FPGA Based Selective Harmonic Elimination Technique for Multilevel Inverter

T. Porselvi¹, K. Deepa², R. Muthu³

¹Department of Electrical and Electronics Engineering, Sri Sai Ram Engineering College, Sai Leo Nagar, Chennai, India ²Department of Electrical and Electronics Engineering, Amrita Vishwa Vidyapeetham, Amrita School of Engineering, Bengaluru, India

³Department of Electrical and Electronics Engineering, SSN College of Engineering, Kalavakkam, Chennai, India

Article Info

Article history:

Received Nov 13, 2017 Revised Dec 18, 2017 Accepted Jan 4, 2018

Keyword:

Field programmable gate array Multilevel inverter Selective harmonic elimination technique Total harmonic distortion

ABSTRACT

Harmonic elimination at the fundamental frequency is very much appropriate for high and medium range of power generation and applications. This paper considers a new technique for selective harmonic elimination (SHE), in which the total harmonic distortion (THD) is minimized when compared with that of the conventional one. With this technique, the harmonics at lower order are eliminated, which are more predominant than the higher ones. Cascaded H-Bridge inverter fed by a single DC is considered which is simulated with the switching angles generated by both the conventional method of SHE and the new method of SHE. The simulated results of the load voltage and the waveforms of the harmonic analysis are shown. The THD values are compared for the two techniques. The experimental results are also shown for the new technique. The switching angles are generated with the help of field programmable gated array (FPGA) in the hardware. The value of experimental THD of voltage is compared with that of simulated THD and the comparison prove that the results are satisfactory.

> Copyright © 2018 Institute of Advanced Engineering and Science. All rights reserved.

Corresponding Author:

Porselvi.T, Department of Electrical and Electronics Engineering, Sri Sai Ram Engineering College, Sai Leo Nagar, Chennai-44 Email: porselvithayumanavan@gmail.com

1. INTRODUCTION

Multilevel inverters are very famous in applications employing high and medium power applications, because of their favourable characteristics like good quality output voltage and output current waveforms, less stress on the switches stress, and less EMI [1-4]. The main classification of multilevel inverter being the neutral point clamped inverter(diode clamped), cascaded H-bridge inverter, flying capacitor inverter [5] and the modular multilevel converters (MMCs) [6-8], [25 - 27]. There are many control techniques available for the multilevel inverter, the most popular and simple technique is the multi-carrier PWM technique. However, this technique is carried out with a high frequency carrier signal that increases the switching losses. Hence, the switching at the fundamental frequency, SHE produces the fundamental at the desired value by eliminating the dominant lower order harmonics [9-11]. In selective harmonic elimination technique, the angles for switching are found by solving non-linear transcendental equation set [12-13].

This paper proposes a SHE technique for the cascaded inverter which employs a single source of DC. The selective harmonic elimination technique further reduces the harmonic distortion of the voltage output of the multilevel inverter. The arrangement of the paper goes like this, Section 2 deals with the

multilevel inverter employing single source of DC, Section 3 deals with selective harmonic elimination technique while section 4 brings out the new harmonic elimination, Section 5 brings out the simulation and experimental results and Section 6 concludes the paper.

2. MULTILEVEL INVERTER EMPLOYING SINGLE SOURCE OF DC

The cascaded Inverters are usually preferred to other configurations of the inverters as they do not require clamping diodes and capacitors. The only drawback of the cascaded inverter is that it uses separate DC sources. An m-level inverter uses $\left(\frac{m-1}{2}\right)$ DC sources, resulting in increased cost. The configuration proposed in this paper eliminates this disadvantage of the conventional cascaded multilevel

proposed in this paper eliminates this disadvantage of the conventional cascaded multilevel inverter [14] [25 - 29].

The configuration requires only one DC source irrespective of levels, resulting in reduced cost. The proposed five-level cascaded inverter employing a single source of DC shown in Figure 1(a). The inverter uses only one DC source irrespective of the number of levels. An m-level inverter of the proposed inverter uses $\left(\frac{m-1}{2}\right)$ transformers. The output of the inverter is connected to the load through the

transformers. The primary of the transformers are connected to the DC source through the bridges. The secondary transformer windings are connected in series aiding to the load [15-16].

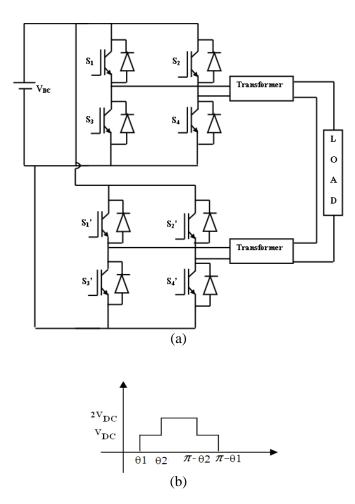


Figure 1. Five-level cascaded multilevel inverter with a single DC source (a) Circuit diagram (b) Waveform of voltage against the switching angles.

Modelling of five level inverter is done using the binary factors of each leg of the H bridges and are

$$H_{11} = \begin{cases} 0, S_1 = OFF, S_3 = ON \\ 1, S_1 = ON, S_3 = OFF \end{cases} H_{21} = \begin{cases} 0, S_2 = OFF, S_4 = ON \\ 1, S_2 = ON, S_4 = OFF \end{cases}$$
$$H_{12} = \begin{cases} 0, S_1' = OFF, S_3' = ON \\ 1, S_1' = ON, S_3' = OFF \end{cases} H_{22} = \begin{cases} 0, S_2' = OFF, S_4' = ON \\ 1, S_2' = ON, S_4' = OFF \end{cases}$$

Where, H_{11} and H_{21} are the binary states of the first and second leg of the first H Bridge respectively. H_{12} and H_{22} are the binary factors of the first and second leg of the second H Bridge respectively. Possible switching configurations of the CHB inverter are shown in the Table 1.

		0	0	
H11	H21	H12	H22	Vo
0	0	0	0	0
0	0	0	1	$-V_{DC}$
0	0	1	0	V _{DC}
0	0	1	1	0
0	1	0	0	-V _{DC}
0	1	0	1	$-2V_{DC}$
0	1	1	0	0
0	1	1	1	-V _{DC}
1	0	0	0	V _{DC}
1	0	0	1	0
1	0	1	0	$2V_{DC}$
1	0	1	1	V _{DC}
1	1	0	0	0
1	1	0	1	$-V_{DC}$
1	1	1	0	V _{DC}
1	1	1	1	0

Table 1. Possible switching configurations of the CHB inverter

3. SELECTIVE HARMONIC ELLIMINATION

Selective harmonic elimination (SHE) technique aims at switching ON and OFF the semiconductor switches in such a way that the desired value of voltage or current fundamental is obtained with less distortion. The angles for switching the devices at the fundamental frequency are calculated by solving the transcendental equation set that characterize the harmonics [17]. For a five-level inverter, two switching angles are to be generated by solving two equations. These equations are solved using the Newton-Raphson (N-R) method that solves the nonlinear equations with initial approximate values is the one among the fastest methods of iteration [18].

Figure 1(b) shows the waveform of voltage for the five-level inverter against the switching angles for a half cycle. Expressing this waveform in Eqn. (1) with the help of Fourier series.

$$v_a(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{DC}}{n\pi} (\cos\theta_1 + \cos\theta_2) \sin(n\omega t)$$
(1)

 θ_1 and θ_2 are the switching angles, where $0 < \theta_1 < \theta_2 < \pi/2$. From Equation 1, fundamental voltage is given by Equation 2 [19-21].

$$V_1 = \frac{4V_{DC}}{\pi} (\cos\theta_1 + \cos\theta_2) \tag{2}$$

The peak fundamental voltage is $V_{m1} = \frac{4V_{DC}}{\pi}$, i.e., it is the value of the fundamental voltage with all the switching angles equated to zero. Modulation index (M_I) is defined as the ratio between the voltage fundamental and the peak voltage fundamental, $M_I = \frac{V_1}{V_{m1}}$. For eliminating the desired harmonic, say the third harmonic, n=3 is substituted in Equation 1 and is equated to zero. The angles for the conventional SHE

$$\cos\theta_1 + \cos\theta_2 = \frac{\pi V_1}{4V_{DC}} \tag{3}$$

$$\cos\left(3\theta_{1}\right) + \cos(3\theta_{2}) = 0 \tag{4}$$

Solving (3) and (4) by Newton-Raphson method, the angles are calculated as $\theta_1 = 0.179$ radians and $\theta_2 = 0.87$ radians. Hence, the third harmonic is eliminated but the other harmonics like fifth, seventh, etc are present.

4. NEW HARMONIC ELLIMINATION

A new SHE technique to minimize the fifth harmonic, along with the elimination of the third order harmonic is considered in this paper. This is achieved by using the equation of fifth order harmonic along with equation of the third order harmonic and leaving the fundamental equation. Fifth harmonic is not completely eliminated but is reduced to a small value by equating the fifth harmonic equation to a minimum value, say 0.0001, as given by Equation 5.

$$\cos(5\theta_1) + \cos(5\theta_2) = 0.0001 \tag{5}$$

By solving Equations. (4 & 5) by N-R method [22], the θ_1 and θ_2 values are found to as θ_1 = 0.2094 rad and θ_2 = 0.8378 rad.

The new selective harmonic elimination reduces one more additional harmonic. For a five level inverter, the technique mitigates the fifth order harmonics in addition to the third order harmonics. For a seven-level inverter, the technique mitigates the seventh order harmonics alongwith the elimination of the third and fifth order harmonics and so on. Hence, the THD value is further reduced. The THD is one among the various performance parameters of inverter circuit and it can be found using Fourier series [23]. THD is the ratio between the sum of all the harmonic components and the fundamental component of the voltage or current.

5. RESULTS AND ANALYSIS

5.1. Simulation results

Simulation work of the five-level inverter is done using MATLAB/ Simulink with the conventional SHE and the new SHE techniques. Waveforms of the simulated output voltage, harmonic analysis and the PWM pattern for both the techniques are obtained.

Figure 2(a-c) respectively shows the simulated output voltage of the MLI, the harmonic analysis and the PWM pattern for the conventional SHE. Figure 3(a- c) respectively shows the wave forms of output voltage of the MLI, harmonic analysis and PWM pattern for the new SHE. From the Figures. 2(b) and 3(b), it is evident that the THD value of the voltage output is 18.46 % with the conventional SHE technique while it is 17.4 % with the new SHE method. Hence, it is clear that the proposed SHE method results in the lesser value of voltage THD as compared to that of the conventional SHE method. The Table 2 compares the THDs of the voltages of the MLI for the two SHE techniques.

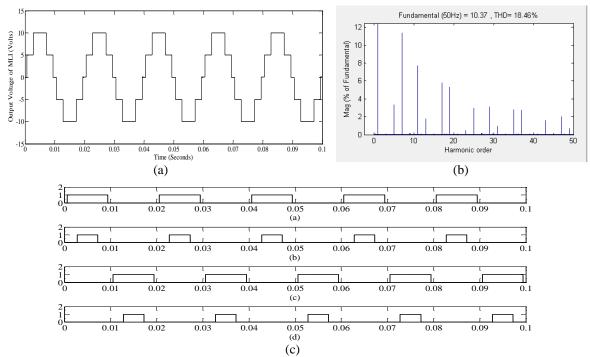


Figure 2. (a) Output voltage of the MLI, (b) Harmonic Analysis, and (c) PWM pattern for the conventional SHE.

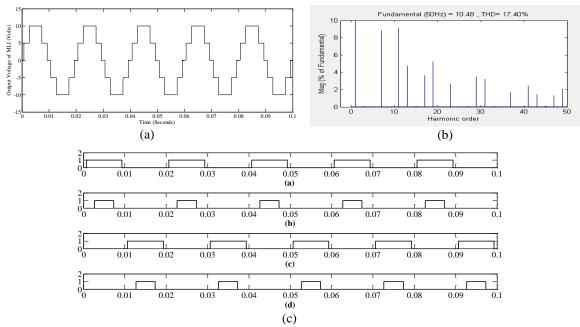


Figure 3. (a) Output voltage waveform of MLI, (b) waveform of Harmonic Analysis, (c) waveform of PWM Pattern for new SHE

Table 2. Voltage THD comparison				
Voltage THD with the conventional SHE technique	Voltage THD with the new SHE technique			
18.46% 17.40%	6			

-

5.2. Experimental results

The proposed five-level CHB inverter is developed in hardware and is experimentally verified. In the hardware, MOSFET switches are used. The switches are fired with the switching angles obtained with the new SHE technique. The switching angles are produced with the FPGA SPARTAN 3E board. Spartan-3 FPGAs are perfectly suited to all type of electronics applications due to its low cost. FPGA realizes high speed switching and attains a high over sampling rate [24]. Figure 4(a) and 4(b) show the snapshot of hardware setup and the output voltage respectively.

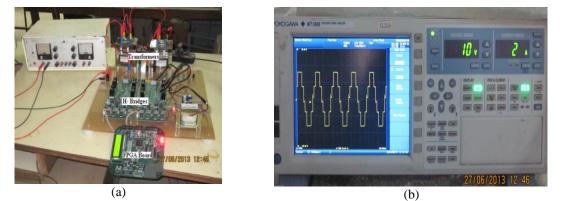
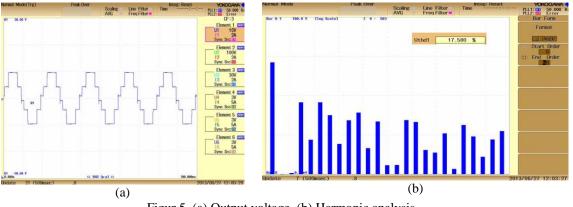


Figure 4. (a) Snapshot of the hardware setup, (b) Snapshot of the output voltage waveform



Figur 5. (a) Output voltage, (b) Harmonic analysis.

It is seen from the Figure 5(b), that the third harmonic is removed and the fifth harmonic is reduced to a low value. It is also seen from the same figure that the voltage THD for experimental output voltage with new SHE is 17.58% considering the maximum of fifty harmonic order. Table 3 shows the comparison of voltage THDs

Table 3. Comparison of the Voltage THDs of the simulated and experimental values

Voltage THD with the new SHE technique for simulated voltage	Voltage THD with the new SHE technique for experimental voltage
17.40%	17.58%

6. CONCLUSION

A new SHE method is proposed and implemented for the five-level inverter. The new method has the advantage of eliminating one more harmonic when compared to the conventional one. Simulation has been carried out for the inverter with the conventional and the new SHE techniques. The simulated waveforms of output voltage, THD analysis and the PWM pattern are obtained. It is found from the simulated harmonic analysis waveform that the voltage THD is 18.46% for conventional SHE while it is 17.40% for the new SHE. Hence, the proposed SHE method has lesser THD value when compared to that of

the conventional SHE method. The five level inverter with single source of DC is developed and verified with the new SHE experimentally. The experimental results of output voltage and harmonic analysis are obtained. The THD value for the new SHE is verified experimentally verified. The THD for the hardware output voltage is 17.58 %, which almost close to the simulated value.

REFERENCES

- [1] L.Tolbert, F-Z. Peng, and T. Habetler, "Multilevel converters for large electric drives", *IEEE Trans. Ind Applications*, vol. 35, pp. 36-44, 1999.
- [2] J.Rodriguez, J-S. Lai, F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications", *IEEE Transaction on Industrial Electronics*, vol. 49, No. 4, pp. 724-738, August 2002.
- [3] Jing Ning Yuyao He Xi'an, Shaanxi, "*Phase-Shifted Suboptimal Pulse- width modulation strategy for multilevel inverter*", Proceedings of IEEE conference on Industrial Electronics and Applications, pp.-1-5, 2006.
- [4] Bum-Seok Suh, Sinha G., Manjrekar M.D., Lipo T.A., "Power Conversion: An Overview of Topologie and Modulation Strategies", Proceedings of 6th International Conference on Optimization of Electrical and Electronic Equipments, vol.2, pp. AD-11-AD-24, 1998.
- [5] T. Meynard and H. Foch, "Multi-level conversion: "*High voltage choppers and voltage-source inverters*," Proc. 23rd Annu. Power Electron. Spec. Conf., Jun. 1992, vol. 1, pp. 397–403.
- [6] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," Proc. IEEE Power Electron. Spec. Conf., Jun. 2008, pp. 174–179.
- [7] A. Antonopoulos, L. Angquist, S. Norrga, K. Ilves, L. Harnefors, and "H. P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1982– 1993, May 2014.
- [8] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.
- [9] J. N. Chaisson, L. M. Tolbert, K. J. Mckenzie, and Z. Du, "A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters", *IEEE Transactions on Power Electronics*, vol. 19, no. 2, March 2004,pp. 478-490.
- [10] S. Sirisukprasert, J. S. Lai, and T. H. Liu, "Optimum Harmonic Reduction with a Wide Range of Modulation Indexes for Multilevel Converters", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, August 2002, pp. 875-881.
- [11] O. Bouhali, E. M. Berkouk, C. Saudemont, and B. François, "A Five level Diode Clamped Inverter with selfstabilization of the DC-Link Voltage for Grid Connection of Distributed Generators", IEEE International Symposium on Industrial Electronics : ISIE 2004, May 3-7, 2004.
- [12] Iwaszkiewicz Jan and Perz Jacek, "Fourier Series and Wavelet Transform Applied to Stepped Waveforms Synthesis in Multilevel Convertors", Proceedings of Electro technical Institute, 2006, pp. 59-74.
- [13] J.Wang, Y. Huang, and F. Z. Peng, "A practical harmonics elimination method for multilevel inverters", *IEEE IAS Annual Meeting*, 2005, pp. 1665-1670.
- [14] T Porselvi, R Muthu, "Sevenlevel three phase cascaded hbridge inverter with a single dc source", ARPN Journal of Engineering and Applied Sciences, vol.7, no.12, pp.1546-1554.
- [15] Sung Geun Song, Feel Soon Kang, Sung-Jun Park, "Cascaded Multilevel Inverter Employing Three-Phase Transformers and Single DC Input", *IEEE Transaction on Industrial Electronics*, Vol. 56, No. 6, pp. 2005-2014, 2009.
- [16] Y. Suresh, A. K. Panda, "Performance of Cascade Multilevel H- Bridge Inverter with Single DC Source by Employing Low Frequency Three Phase Transformers", IECON- 36th Annual Conference of IEEE Industrial Electronics Society, Pheonix, AZ, USA, pp.1981-1986, 2010.
- [17] Fang Zheng Peng, Jih-Sheng Lai, J. McKeever and J. VanCoevering, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation", *IEEE Transactions on Industry Applications*, vol. 32, No. 5, pp. 1130-1138, September/ October 1996.
- [18] C. Woodford and C. Phillips, "Numerical Methods with Worked Examples", Chapman and Hall, pp. 45-57, First edition 1997.
- [19] Jagdish Kumar and Biswarup Das, "Selective Harmonic Elimination Technique for a Multilevel Inverter", Fifteenth National Power Systems Conference (NPSC), IIT Bombay, pp. 608-61, 2008.
- [20] Ali Ajami, Mohammad Reza Jannati Oskuee, and Ata OllahMokhberdoran, "Implementation of Novel Technique for Selective Harmonic Elimination in Multilevel Inverters Based on ICA", Advances in Power Electronics, 2013, pp 1-11.
- [21] D. Ahmadi, K. Zou, C. Li, Y. Huang, and J. Wang, "A universal selective harmonic elimination method for highpower inverters", *IEEE Transaction on Power Electronics*, vol. 26, no. 10, pp.2743–2752, 2011.
- [22] T.Porselvi & R.Muthu, "Modeling and Control of the PMSG for the Wind Energy Conversion System with the CHB Inverter with the New Selective Harmonic Elimination Technique", *International Review on Modelling and Simulation*, vol. 6, no. 3, pp. 767-773, 2013.
- [23] Hussain Bassi, "A Modulation Scheme for Floating Source Multilevel Inverter Topology with Increased Number of Output Levels", *International Journal of Electrical and Computer Engineering (IJECE)*, Vol. 6, No. 5, October 2016, pp. 1985-1993.

- [24]Hiroki Kurumatani, "FPGA-based voltage control with PDM inverter for wideband drive system using T-type neutral-point-clamped topology", EEE International Conference on Mechatronics (ICM), 2017, pp. 1-5.
- [25]Athira S, Deepa K, "Modified Bidirectional Converter with Current Fed Inverter", International Journal of Power Electronics and Drive Systems (IJPEDS), vol.6, No 2, pp.396 – 410, June 2015.
- [26]R. Nair, Mahalakshmi R and Sindhu Thampatty K. C., "Performance of three phase 11-level inverter with reduced number of switches using different PWM techniques," International Conference on Technological Advancements in Power and Energy (TAP Energy), Kollam, pp. 375-380, 2015.
- [27]K. Deepa, Savitha. Pb, and Vinodhini. Bb, "*Harmonic analysis of a modified cascaded multilevel inverter*", 2011 1st International Conference on Electrical Energy Systems, 2011, pp. 92-97.
- [28]R. Mahalakshmi and Thampatty, K. C. Sindhu, "Implementation of Grid Connected PV array using Quadratic DC-DC Converter and Single Phase Multi Level Inverter", *Indian Journal of Science and Technology*, vol. 8, 2015.
- [29] Parvati Nair, Deepa. K, "Two-port DC-DC converter with flyback inverter for rural lighting applications", Proceedings of IEEE International Conference on Technological Advancements in Power and Energy, TAP Energy 2015, pp. 249-253, 2015.

BIOGRAPHIES OF AUTHORS



Dr. T. Porselvi, Associate Professor in the Department of Electrical & Electronics Engineering has 19 years of teaching experience. She received her B.E. degree in Electrical and Electronics Engineering from Madras University, M.E. degree in Power Electronics and Drives from Anna University and Ph.D degree from Anna University. She is a life member of IETE and ISTE. Her areas of interest include Power Electronics, Wind Energy Systems, Electrical Machines, Control Systems, and Network Theory. She has authored 2 textbooks on "Electrical Machines" and "Control Systems". She has published 15 international journal papers, 9 papers in international conference and 9 papers in national conference



Dr. K.Deepa graduated from Alagappa chettiar college of engineering and Technoilogy, T.N, India in 1998. She obtained M.Tech degree from Anna University, Guindy campus, T.N, India in 2005. She received Doctoral degree from Jawaharlal Nehru Technological University, Anantapur, A.P, India in 2017. Currently she is working as Assistant professor in Electrical and Electronics Engineering Department, Amrita School of Engineering, Amrita Vishwa Vidyapeetham University, Bangalore, Karnataka, India. She has 19 years of teaching experience. She is a life Member of IETE and ISTE, India and a professional member of IEEE. She has authored 2 textbooks on "Electrical Machines" and "Control Systems". She has published 17 international journal paper, 2 national journal papers, 25 papers in international conference and 6 papers in national conference. 15 M.Tech Degrees were awarded under her guidance. Her areas of interests include Power electronics, Renewable energy technologies and Control Engineering.



Dr. Ranganath Muthu, Professor in the Department of Electrical & Electronics Engineering has 27 years of teaching and 2 years of industrial experience in the field of Instrumentation, Control and Power Electronics. He has been awarded the Young Scientist Fellowship for the year 1994-1995 by the Tamil Nadu State Council for Science & Technology. He has published 40 papers in International Journals and 53 papers in the proceedings of International/ National Conferences.