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A Novel Low Power-Application UPS Consisting of an APF - Correction Circuit & Integrated Battery-Management System

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ABSTRACT

For the up-coming generations of power-supply systems, the load located area power-supply sources are an effective one, in terms of our requirements: simplicity, integrity, battery-backup, etc. This could follow the Normalization of power factor & Reducing THD% values on input current, which makes us to add an essential to include a power-factor correction unit at supply side in these new typical topologies. This Proposed architecture presents an integrated battery manage system which can also offers PF correction along with Galvanic-Isolation of battery in a humble single structure. [3] The proposed scheme has the reliable characters like increased efficiency, compact circuit and reduced costs associated with a traditional standalone multiple-stages UPS with PFC. This paper addresses the UPS action, the analysis and simulation results of Proposed UPS scheme.

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1. INTRODUCTION

From the past improvements in this research now some more features are necessary to maintain. (1) Power factor correction (PFC) because of its compulsory benefits, this enhancement signifies to a conventional UPS; above and beyond, the world-wide rules make it compulsory. Then, in the way to get this capability, this is essential to add an additional power processing stage. (2) These days, this not sufficient towards rise the density of power in converters capabilities, supplementary this indicates use of high switching frequency converting strategies for bringing compactness & simple constructional techniques, etc., To acquire the requirements of individuality, idleness, and battery back-up unit, all of these appears to be essential for the up-coming trends in power supplies. Integrated planning in power suppliers' systems solves the major issue of our problem, there presents new innovations with doors opened necessary research fields.

The greatest exciting task in the primary stage of a power supply is perhaps power factor correction (PFC) [1], along with this isolation from source to load. Battery galvanic isolation to the whole system is needed. In few situations, a sinusoidal nature output voltage is compulsory, and in those situations the inverter stage is employed based on the boost inverter characteristics especially full-bridge inverter (FB-BI). Boost inverter is used because of the limitations of the normal inverter topologies.

2. PROPOSED SCHEME

The architecture of the Proposed power supply system is shown in Figure 1. The topology works all together with, APFC with the Battery Management system and UPS operations on the primary side of the main converter. On secondary side of the Proposed UPS scheme we perform only inverting action with mandatory options like boosting voltages. The Main converter in its normal mode operation of UPS is capable of carrying out the battery charging along with power factor correcting functioning. Then followed by inverter stage [2]. The Main/Primary converter has Normal, Backup/Discharging & Charging operative modes, which will be described in the following sections.

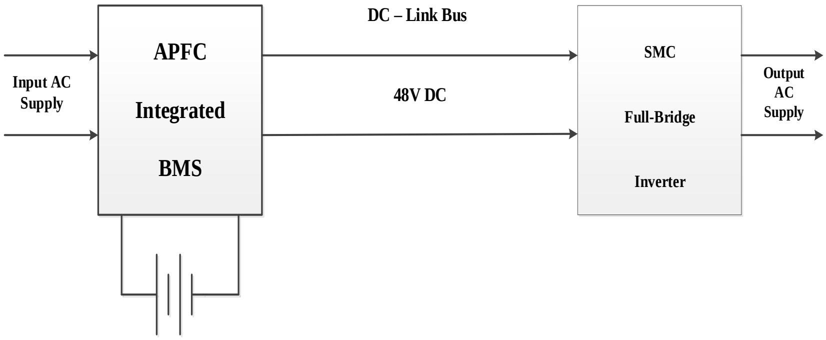

Figure. 1 Proposed UPS Converter with in-built APFC, integrated BMS

2.1. APFC circuit with Integrated BMS:

This APFC Circuit with integrated BMS will works up-on a simple logic-gate based driver circuit. As of this integrated battery charger is incorporated with BMS we came to know that it is a DC-DC power converter, here we used a flyback converter as supply side main power converter.

Throughout the UPS process this flyback converter will works on Discontinuous Conduction Mode (DCM). For making the UPS a very simple operation is needed for that necessity the conduction mode will be stick to DCM in-order to avoid extra controlling circuitry. The UPS is consisting of 3-different modes in them 2-modes are similar in terms of power processing while another-one is independently controlled or independent in terms of control. Here the controlling refers to generation of the control signal which we are going to applying them in those modes.

For the autonomous control signal generation in the respected mode of operation by automatically without human interference we needed a little monitoring system and there by Pulse Width Modulated controller is required respectively, those monitoring system will consisting of some voltage sensors; and taken as the reference input to the PWM control signal generator/ driver circuit.

The states of supply and battery will be measured in terms of their voltage magnitude, if the supply voltage magnitude is not as require our UPS will switches the load power from normal mode to back-up mode to acquire safety over high input currents. The exact voltage references how here taken to perform the automatic operation is as follows;

$$Battery = \begin{Bmatrix} 1 \text{ for battery low} \\ 0 \text{ for battery full} \end{Bmatrix}$$

$$Line = \begin{Bmatrix} 1 \text{ for line ok} \\ 0 \text{ for line fail} \end{Bmatrix}$$

There by we will generate control signals by the following K-Maps:

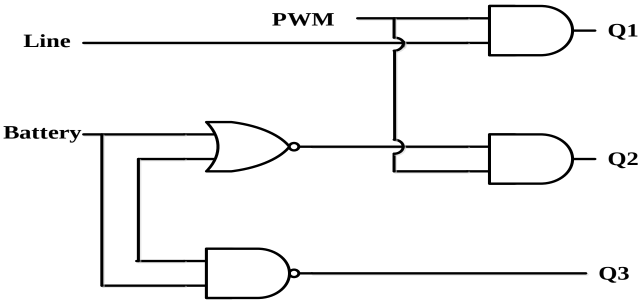

Figure 2. Logic gates with respect to PWM & Status of input parameters

According the instant input-parameters the mode will decided by the Gate-Driver circuit and it is mixed with corresponding PWM signal. The PWM signal will possess pre-defined frequency and duty ratio. Frequency will co-ordinates the converter’s front side filter/correction circuit, the Lf & Cf on the line filter/active power factor correction circuit will works with this switching frequency on the primary converter.

This converter will be looks as shown in the Figure 3. Their duty ratio of PWM signal will helps to control the power transfer from this flyback-converter input to output. In the Normal mode & Charging mode this duty ratio will be useful to control the power follow. Specially in the Normal & Charging modes of operation by selecting the pre-calculated switching frequency of the fly-back converter will affects the “Power Factor” on the supply side, along with input current THD values. As the THD and P.F. are related, by this method the THD & P.F. can be together we can achieve combined control over them. [3]

In the backup/discharging mode the UPS primary converter is a regular fly-back converter, so that simple pre-defined parameters are required like transformer magnetizing inductance, switching frequency and duty ratio all we need to do is to get a 48V output on the end side of the primary converter. Also, in the Normal & Charging mode of the converter also, for a 48V output.

2.2. Inverter Stage

The output of the DC-DC converter is 48V in DC, this should be convert into AC for the multipurpose utility application of the UPS with in the limitations of UPS power capabilities, the inverter stage of this UPS is a Full-Bridge Boost Inverter.

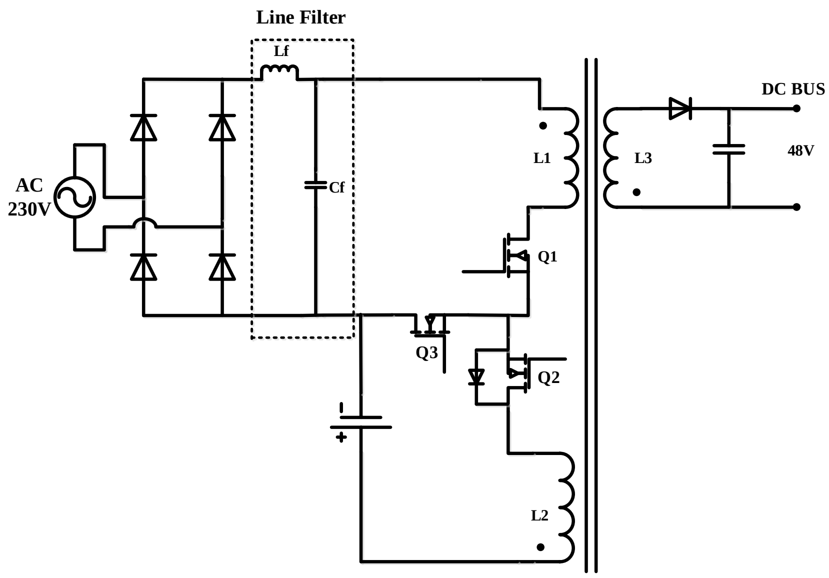

Figure 3. Primary Converter; APFC integrated BMS – UPS Converter

Boost – inverter topology is taken into considered for the voltage fluctuation condition of input, for the regular variation range of the input voltage UPS should be able give the constant output voltage, thus voltage stabilization also achieved from this UPS. For to do this on the inverter side, the SMC (Sliding mode Control) technique is used. To implement this the converter, it is modeled as two dc/ac boost inverters; But one is to be considered as a normal sinusoidal nature voltage source.

How this boost inverter attains DC - AC conversion/inversion is mentioned bellow by step by step; this SMC-FBI is composed by two bi-directional DC to AC boost-converters. This converter produces a DC–Biased sinusoidal output, so that each converter only gives a unipolar voltage. The modulation index of each converter is 180o out of phase with the another one, which can cause the maximization of the voltage over the load [4]. The load is connected differentially across the two single inverters. Thus, where as a DC bias voltage appears at each end of the load with respect to ground. Figure 4 shows the SMC-FB inverter.

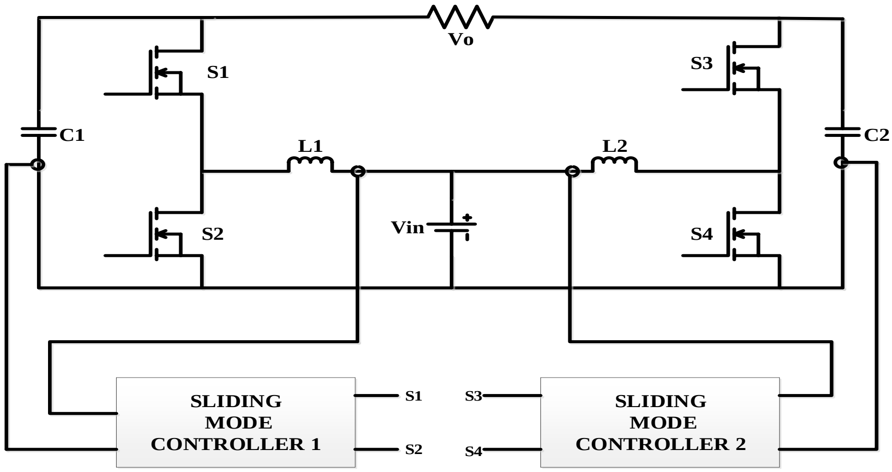

Figure 4. SMC-FB inverter

As we can observe from the above figure the “Vin” here is input to the SMC-FB inverter its input is “Vdc Bus” voltage & “Vo” is UPS output shows across at “R” is load resistor voltage. The following figure Figure 5. Shows the output waveforms of each DC-AC converter as we can see they are exactly 180o phase shift and both are DC-Biased sinusoidal waves in nature [2] [4], the resultant wave Across load will be seen similar to ideal sinusoidal wave alternating between positive and negative amplitudes. The output variation of each converter is 180o out of phase with each other, which make the most of the voltage over the load is as ideal. The following wave forms are shown at 60hertz frequency. They can represent each converter’s output wave forms.

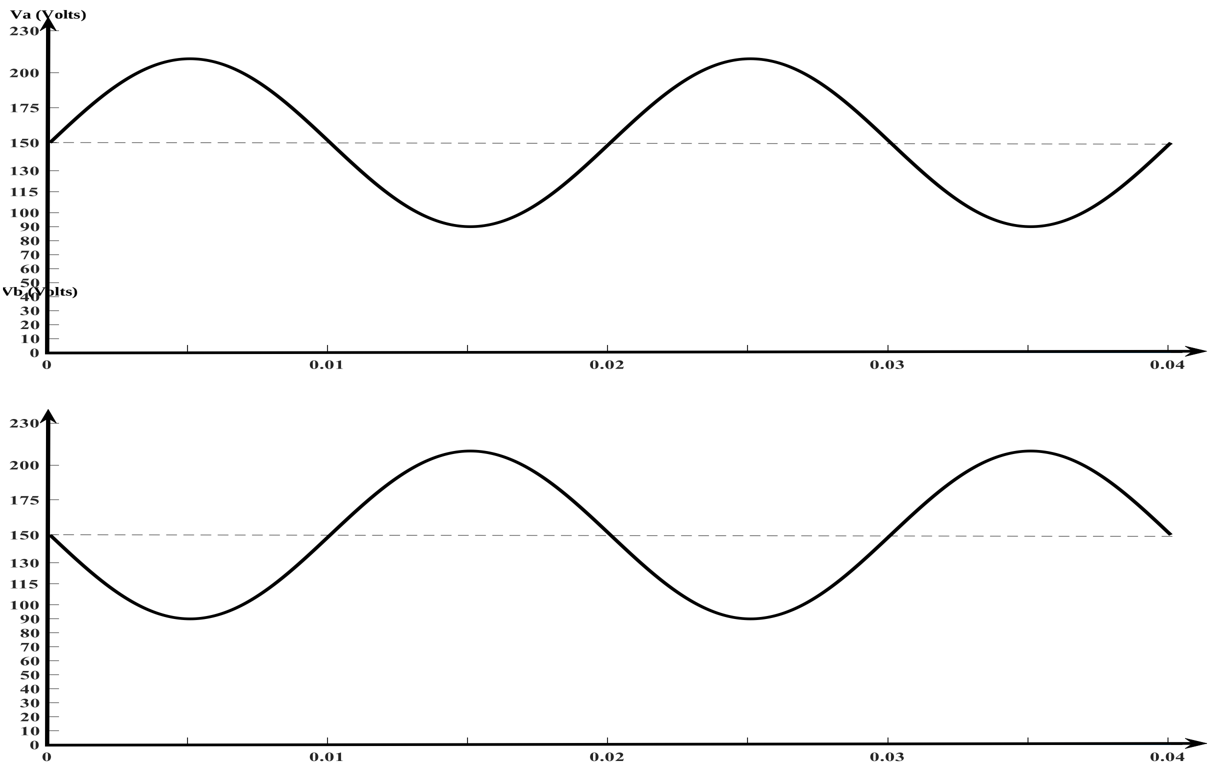

Figure 5. Output voltage for each DC–AC converter

This FB-Inverter works almost similar to that of normal full-bridge inverter apart from boosting terms and switching pulses operation. In the part of the concept of the Proposed converter's operation, from the reference part they are assumed that all the components are ideal and the converter operates in CCM. We have two - topological modes, for a period of operation. The equivalent circuit diagram will be shown in Figure 6.

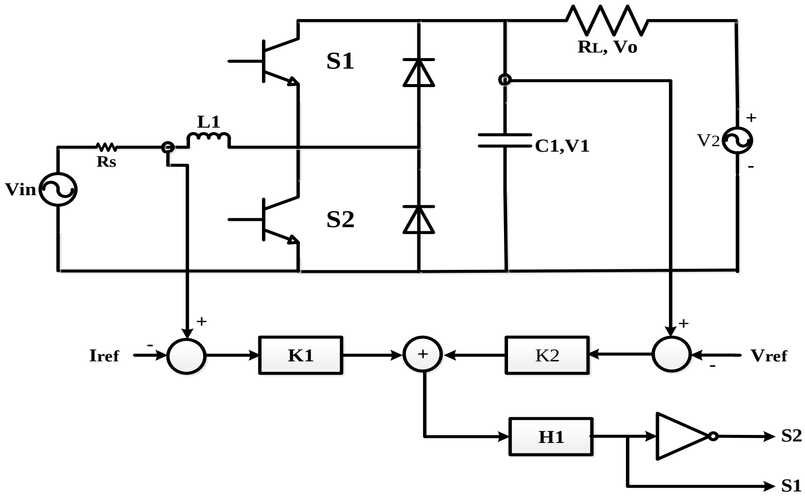

Figure. 6 Sliding Mode Control shows for initial stage of FB inverter

For the Proposed UPS architecture control block scheme is shown in Figure 6. With a suitable adjustment of these constants, we get high control of robustness over the inverter, stability and faster response can be achieved for any operating condition. The system parameter/co-efficient comprises: voltage of DC bus as Vin, receiving side inductors: L1 also with L2, power electronic switches S1, S2, S3, S4 & transfer capacitors: C1 also with C2. Free – wheeling diodes D1 to D4 & load resistance RL. The outputs of capacitor voltage Capacitors: V1 & V2 necessarily follow a sinusoidal nature in wave shape, the furthermost loyally as possible. If the switch S1 is ON and S2 is off, current iL1 goes quite linearly, since the diode D2 is reverse-biased and capacitor C1 supplies energy to the load, decreasing voltage V1. iL1 Current flow through capacitor C1 and the output stage. Figure 7 shows Proposed UPS architecture, with APFC integrated BMS enabled SMC-FB inverter UPS.

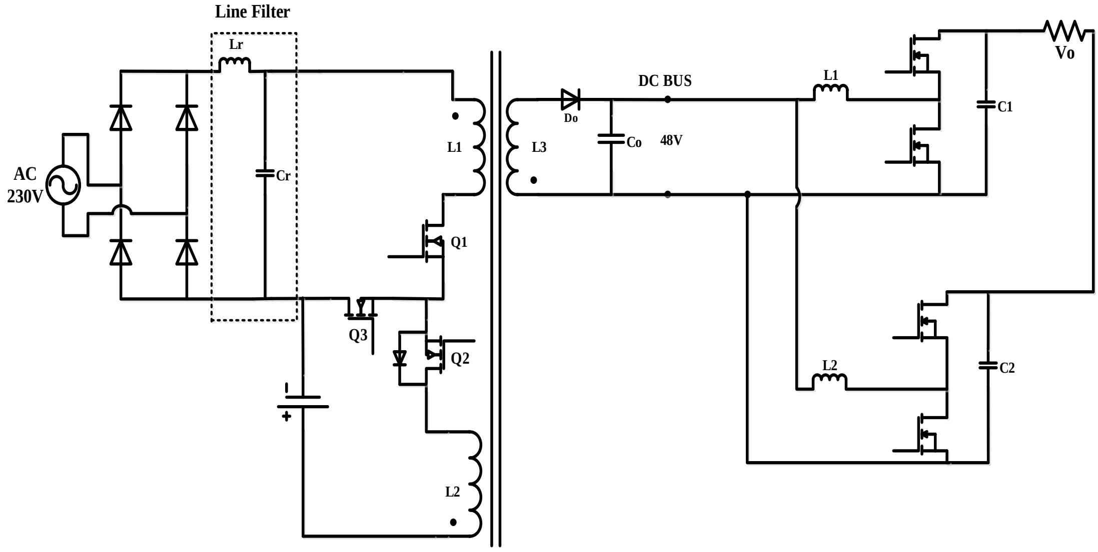

Figure 7. Proposed UPS architecture, with APFC integrated BMS enabled SMC-FB inverter UPS

The current iL1 decreases while capacitor C1 is recharged. Here switches are controlled by hysteresis block H1 generated pulses, so that variable of S (iL1, VI) is gained. The converter's control is done by the circuit parameters and coefficients, here K1, K2.

3. RESULTS & CONCLUSION

The Proposed Isolated UPS Scheem with APF, Integrated BMS & SMC Inverter was simulated in Mat-Lab Simuink and the respected waveforms & Outputs are observerd. The results which I got was shown below with their impartence. Primary Converter's response in all the 3-mode was observed and captured, shown in Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13 in mode by mode wise:

Normal mode: Input Current got 2.33% of THD and PF is 0.89

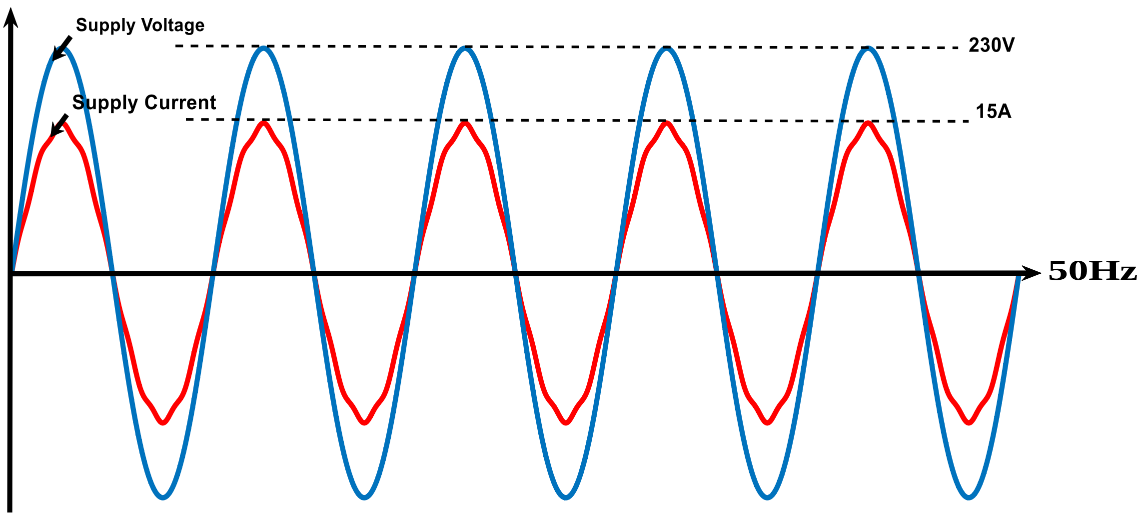

Figure 8 (a). Input Voltage and Current waves in Normal Mod

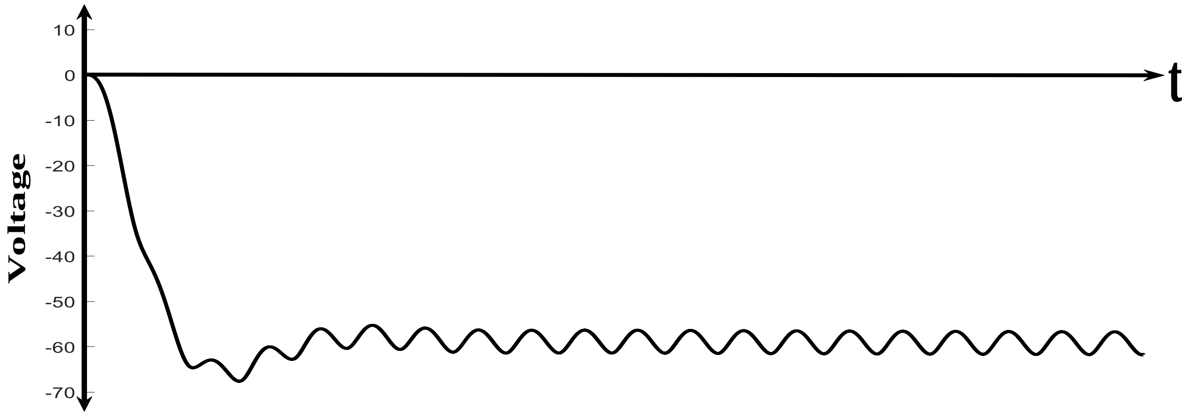

Figure 9. DC Link Voltage wave form

Charging Mode: Input Current got 4.476% of THD and PF is 0.889

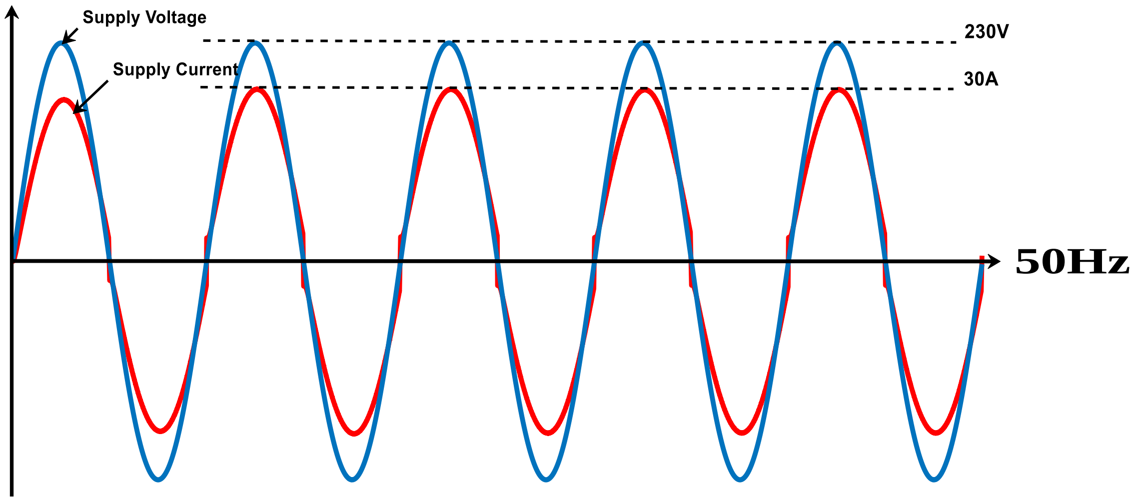

Figure.10 Charging mode supply voltage and current waves in Charging mode

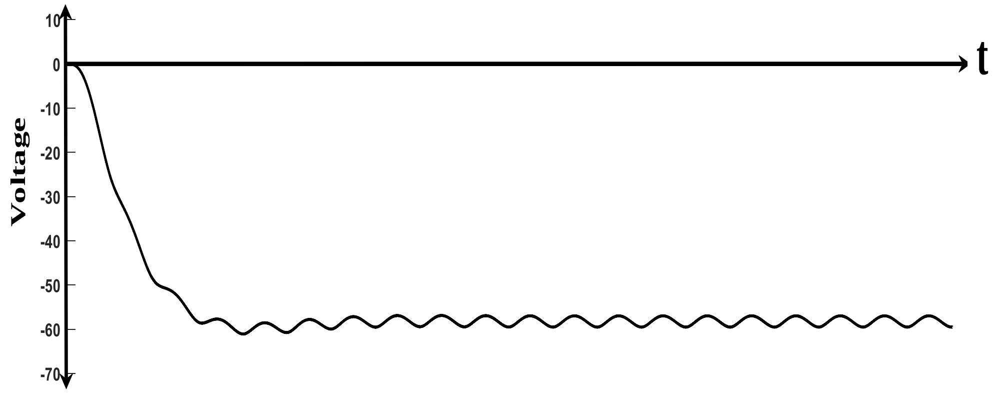

Figure 11. DC Link Voltage wave form

Back-up Mode:

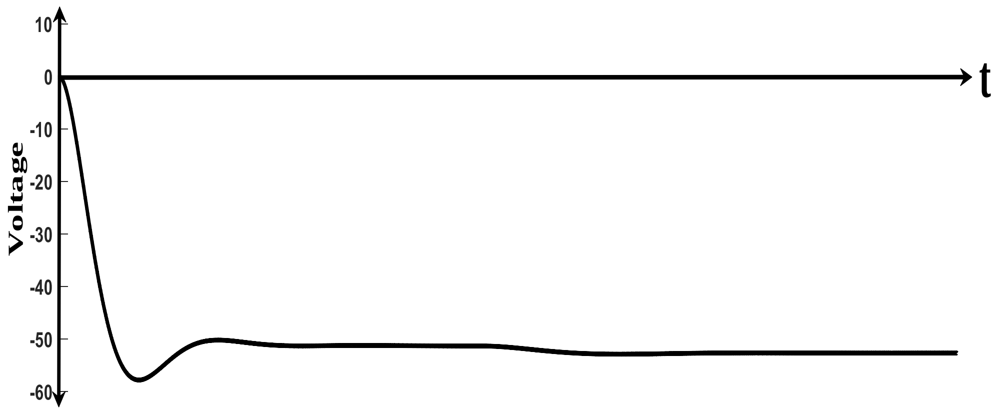

Figure.12. DC Link Voltage wave form

Inverter Output: Output Voltage got 4.23% of THD & also a good PF, not shown in below waveform.

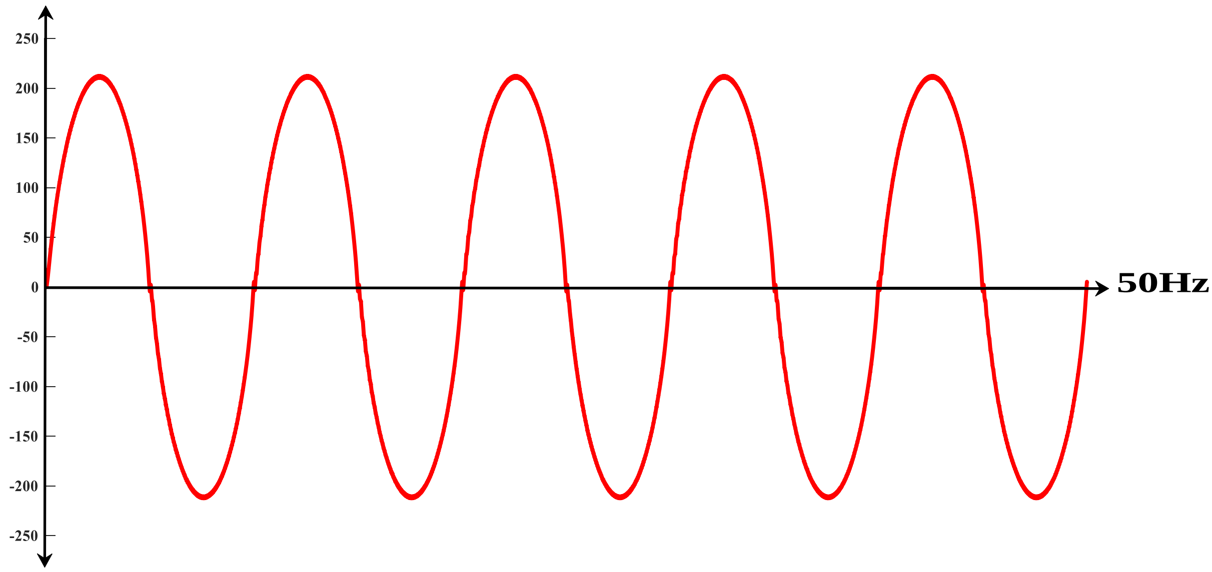

Figure.13. Inverter output waveform

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The results was simulated by me in the part of publishing a technical paper of my post graduation program and proposed theory was porperly adopted as metioned in the refference section. And this paper is the basic paper for my reaserch field UPS.

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