

Fractional PID controlled cascaded flyback switched mode power supply with enhanced time domain response

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ABSTRACT

This work compacts with the modeling, simulation, and application of a Fractional Order Proportional Integral Differential (FOP-I-D) controlled Cascaded Flyback Switched Mode Power Supply (CFSMPS) system. It recommends Parallel cascaded flyback converter for the production of essential DC voltage from the input supply voltage. The output from CFSMPS is regulated by using closed loop configuration. The simulation of Closed-loop Proportional-Integral (PI) and FOP-I-D controlled CFSMPS system has been done and the results of the systems are related. The outcomes signify that the FOP-I-D based system has presented an enhanced response to represent as similar to the PI controlled CFSMPS system. The FOP-I-D controlled CFSMPS system has benefits like decreased steady-state error and enhanced time-domain response.

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1. INTRODUCTION

Saggini et.al presented the simple reference based model to auto tune digitally controlled CFSMPS. A self tuning closed loop technique was amended to digital DC-DC Cascaded Flyback Switch Mode Power Supplies (CFSMPS) in relation to Proportional Integral Derivative (PID) regulators. The tuning method of open loop reference based model was discussed in detail with the digitally disturbed frequency. Then the control loop was inserted for obtaining a closed loop solution and it was overlapped with the control of a duty cycle [1]. An adaptive tuning system with a plan and execution of digital DC-DC converters along with desired phase margin was suggested by Zane et.al [2]. The prevailing adaptive tuning method of controlled Cascaded Flyback Switched Mode Power Supplies (CFSMPS) was digitally controllable. This tactic was relied on maintaining the path of the system continuously based on the systems intersect frequency and phase margin. To meet the above objectives, compensator parameters were unceasingly tuned by a closed loop Multi-Input-Multi-Output (MIMO). A digital tiny square wave signals was commonly injected into the digital compensator and the Digital Pulse Width Modulator (DPWM). The stability margin can be achieved and also continuously monitored. The compensator parameters were adjusted by the MIMO loop for reducing the error among the required and estimated phase margin and intersect frequency.

Morroni et.al has stated that the existing stability margin reserved a path of a digital Switched-Mode Power Supplies. A feasible method has been suggested for reserving a path of the phase margin and cross over frequency of the digital Cascaded Flyback Switch Mode Power Supplies (CFSMPS). From loop-gain measurement technique given by Middlebrook et.al, the proposed concept was recommended for the implementation of digitally controlled SMPS. A Process of injecting the digital square wave signal to its source or to a preceding stage was regulated with its signal frequency. Simultaneously, the system online

phased margin and crossover frequency were obtained by monitoring loop signals, i.e., under normal operation of closed loop CFSMPS [3]. Jeffery et.al has presented the operating modes in Continuous and Discontinuous for SMPS in an adaptive Tuning method. They have suggested the concept of digitally controlled voltage-mode for Switched-Mode Power Supplies from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM) and stated vice versa with the existence of a large signal change. This process has the ability of retaining high-performance control loop associated with CCM to DCM mode transitions to the stability problems [4]. Hellany et.al has suggested resolution of issues in Cascaded Flyback Switched Mode Power Supplies (CFSMPS) by EMI/EMC. Power supplies play a significant role in causing deterioration of the electromagnetic environment. He has also examined Electro Magnetic Interference (EMI) issues in Cascaded Flyback Switch Mode Power Supply (CFSMPS), including fundamental concepts and classifications of Electromagnetic Compatibility. They have also referred to the root cause of the conducted emission from CFSMPS and the role of freeloading elements in the propagation of EMI [5].

Ferreria et.al has provided the Sources, route and drawbacks of conducted EMI in the SMPS circuits the production and propagation of electromagnetic noise obtained in the formal circuit investigation due to the complexity involved in the freeloading in the circuit. The mystery behind the high-frequency features of materials and components are unpredictable for the designer. Similarly the designer is unaware of the freeloading that occurred owing to complicated 3D shapes [6].

Isolated Switch Mode Power Supply for LED Application was presented with design and implementation by Reshma et.al [7]. A New Fly-Back Converter's design using PID Controller has been proposed by Modak et.al [8]. Reliability Measures for Switched-Mode Power Supplies (CFSMPS) with Redundant Flyback Transformer was the product of Pankaj et.al [9]. Improved Power Quality CFSMPS for Computers Using Bridgeless PFC Converter at Front End owes it to Singh et.al [10]. A novel method of Switched mode power conversion design has been suggested by Middlebrook et.al. The excellent design circuitry, palpable efficiency and good flexibility and utmost simplicity of the design provided the capability for substituting the prevailing conventional electrical power processing methods. The system invoked an in-depth discussion on itself and the working of the Ćuk converter; this was followed by its various extensions. A coupled-inductor technique helped achievement of improved efficiency and reduction in size and weight [11]. A detailed discussion on AC to DC converters with rectified power factor and HF transformer insulation was suggested by Singh et.al. A Switched mode solid stated AC-DC converter results transformer isolation (high-frequency) was designed with buck-boost, boost and buck topology. It had the enhanced power quality in addition to Power Factor Correction at AC supply; reduction in the input current's Total Harmonic Distortion (THD) and exact regulation and isolation of the DC output voltage.

An in depth knowledge of power factor correction was done by Singh et.al [12]. Design, Simulation and Implementation Techniques of High-Performance GAN SMPS were presented by Bhavya et.al [13]. It was suggested by Halder et.al to use Flyback Converters, Spacecraft Electrical Power Systems (EPS) [14]. Design and implementation of a new FPIDF-II controller for a widely accepted two-area nonreheat thermal AGC system employing ICA optimization technique was done by Y.Arya [15]. A Multilevel Quasi Matrix Converter Design for SRM Drives in EV Applications was suggested by Syeda [16]. Open Loop and Closed Loop Performance of Switched Reluctance Motor with Various Converter Topologies has been presented by Kirankumar [17]. Impact of freeloading Components on EMI Generated by SMPS has been explained by Milind [18]. Interleaved boost converter fed with PV for Induction motor / agricultural applications was presented by Adireddy [19]. An optimal fuzzy classical controller for Automatic generation control of two-area electrical power systems was suggested by Y.Arya [20]. There has been no reference in literature relating to the cascaded flyback converter system. This investigation suggests a cascaded flyback converter among AC source and load to enable reduction in input current ripple. The papers reported in the literature relating to the above referred subject do not provide any comparison between PI and FOP-I-D controlled CFSMPS systems. The proposed FOP-I-D controller regulates the output of CFSMPS system. The dynamic response of closed loop system is improved through the use of FOPID controller.

2. SYSTEM DESCRIPTION

The conventional flyback converter system is shown in Figure 1. An uncontrolled rectifier converts AC to DC. Using flyback inverter the DC from the rectifier is converted into high frequency AC and its output is converted back into DC using a rectifier. The proposed system of flyback converter for a closed loop is shown in a schematic form in Figure 2. The FOP-I-D controller is proposed for the improvement of the time response of the closed-loop system. The output voltage V_o is compared with respect to the reference voltage V_r and an error signal e_s is given to FOP-I-D. The FOP-I-D output is provided to a comparator, where the sawtooth is compared with the FOP-I-D output. The FOP-I-D system updates the width of the pulse applied to the MOSFET.

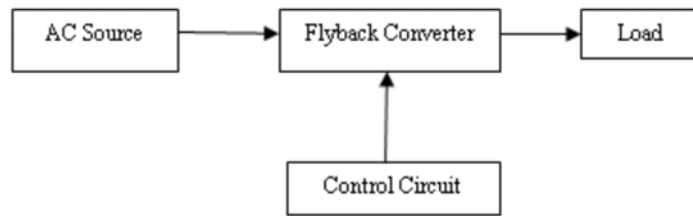


Figure 1. A Schematic form of Conventional flyback converter

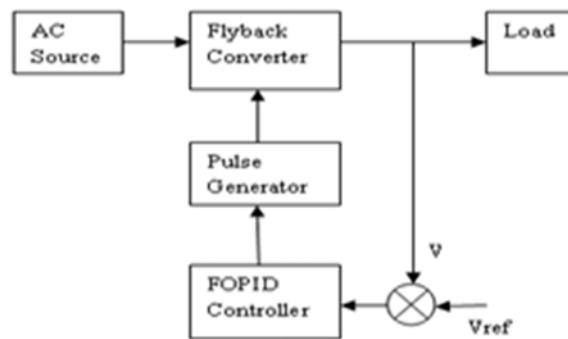


Figure 2. A schematic form of the proposed flyback converter

3. ANALYSIS

A model of FOP-I-D was developed from fractional differentiation. The response obtained with FOP-I-D controller is quite faster than PI controlled system. Figure.2 shows the FOP-I-D control structure. The transfer function of an FOP-I-D controller is given by $C_{FOPID}(s) = K_p + K_i/s^\lambda + K_D s^\mu$ where λ and μ are the order of the integral part derivative part respectively. K_p , K_i and K_D denote the controller constants as in a conventional PID-controller.

4. SIMULATION RESULTS

Figure 2(a) is the circuit diagram of the open loop CFSMPS system. The input voltage to the rectifier is seen as 440V in Figure 2(b). The output voltage is shown with the value of 180 V in the Figure 2(c). The output current along with the value of 2A is shown in Figure 2(d). The Figure 2(e) displays the output power with the value of 190 watts. A small disturbance created is seen at the input at about 0.5 secs which results in a change in output voltage and current. Since open loop configuration is used, the output voltage cannot be regulated.

A closed loop CFSMPS with PI controller is shown in Figure 2(f). The input voltage at its value of 440V is presented in Figure 2(g). The Figure 2(h) represents the output voltage at the value of 90V. Similarly the output current is represented in Figure 2(i) at the value of 1.9A. Figure 2(j) displays the output power at value of 175 watts. As the disturbance is created at 0.5secs, its consequence in the output voltage is seen at 0.5 secs. The use of PI controller helps to increase in the output voltage which gets regulated at 0.9 secs. The rise time, peak time and settling time for PI Controlled CFSMPS are observed as 0.54 secs, 0.7 secs and 0.9 secs respectively.

The circuit diagram of the closed loop CFSMPS with FOP-I-D controller is presented in Figure 3(a). The input voltage is presented in Figure 3(b) with the values of 440V. The Figure 3(c) and 3(d) represents the output voltage and output current with the value of 90V and 1.9A respectively. The Figure 3(e) displays the output power at the value of 180 watts. As the disturbance is created at 0.5 secs, its consequence in the output voltage is seen at 0.5 secs. The use of FOP-I-D controller helps to increase in the output voltage that gets regulated at 0.6 secs. The rise time, peak time and settling time for FOP-I-D Controlled CFSMPS are observed as 0.53 secs, 0.56 secs and 0.6 secs respectively.

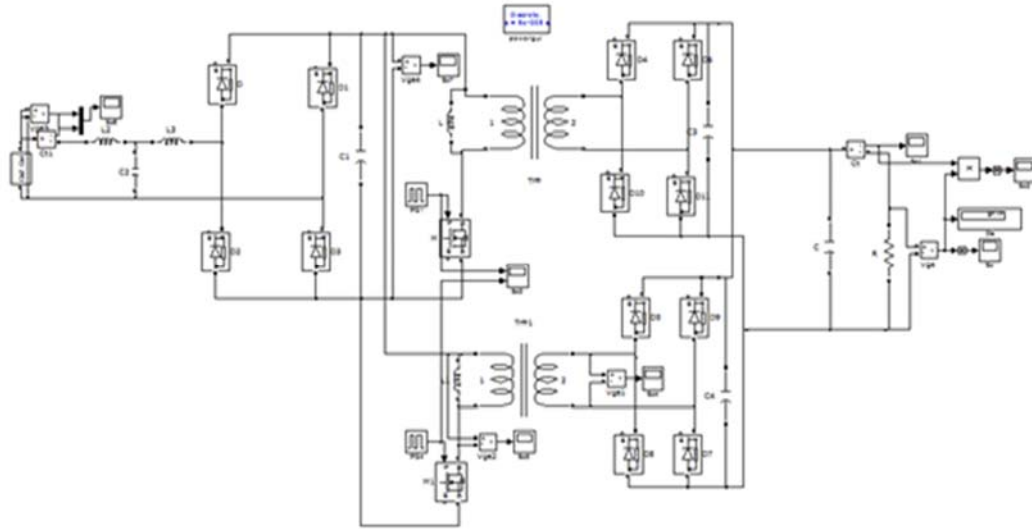


Figure 2(a). Simulation diagram of open loop CFSMPS

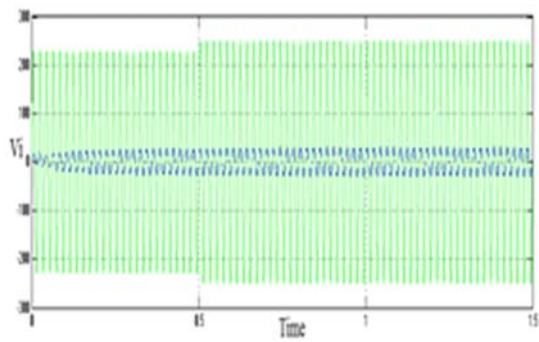


Figure 2(b). Input voltage

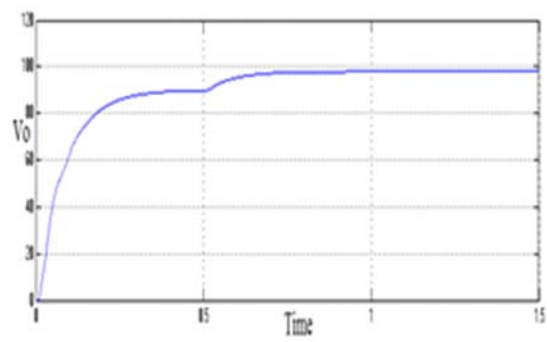


Figure 2(c). Output voltage

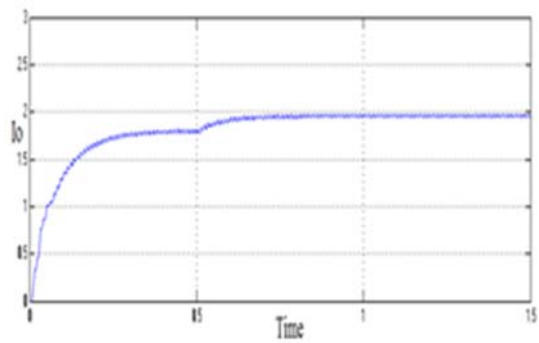


Figure 2(d). Output current

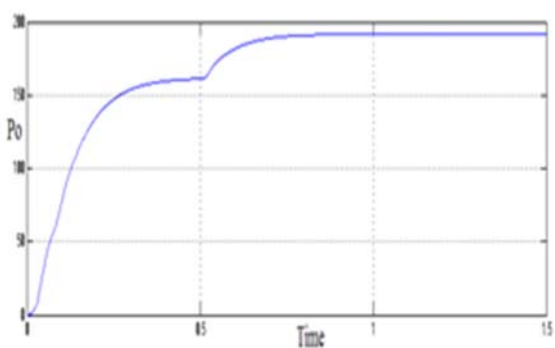


Figure 2(e). Output power

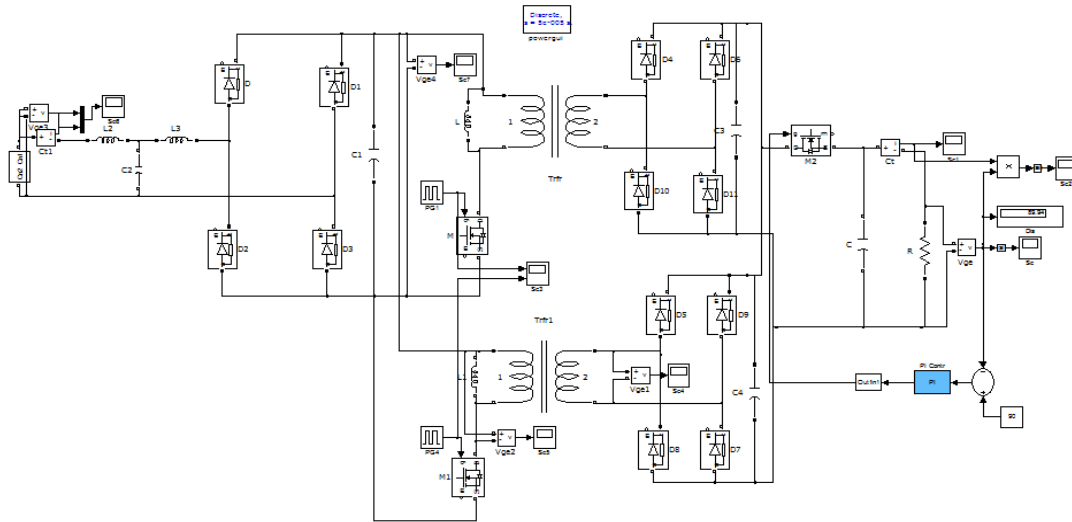


Figure 2(f). Simulation diagram of the closed loop CFSMPS with PI controller

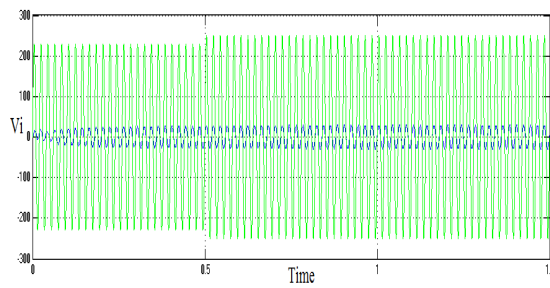


Figure 2(g). Input voltage

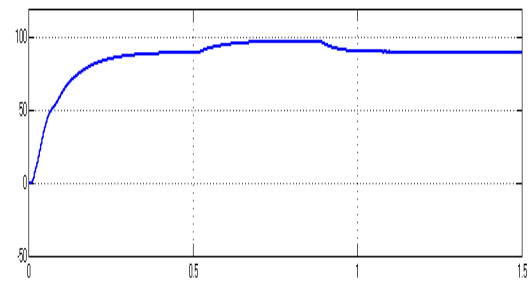


Figure 2(h). Output voltage

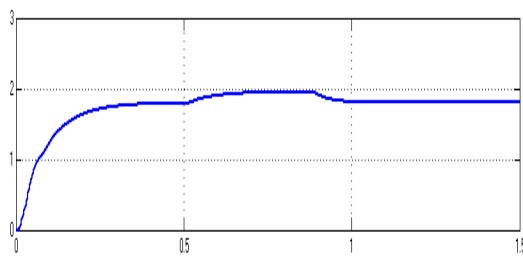


Figure 2(i). Output current

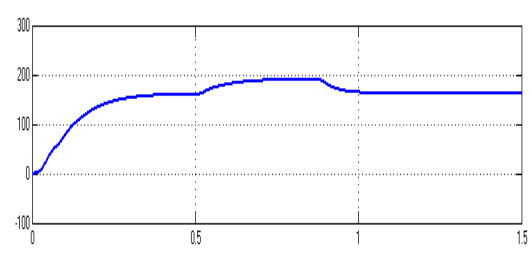


Figure 2(j). Output power

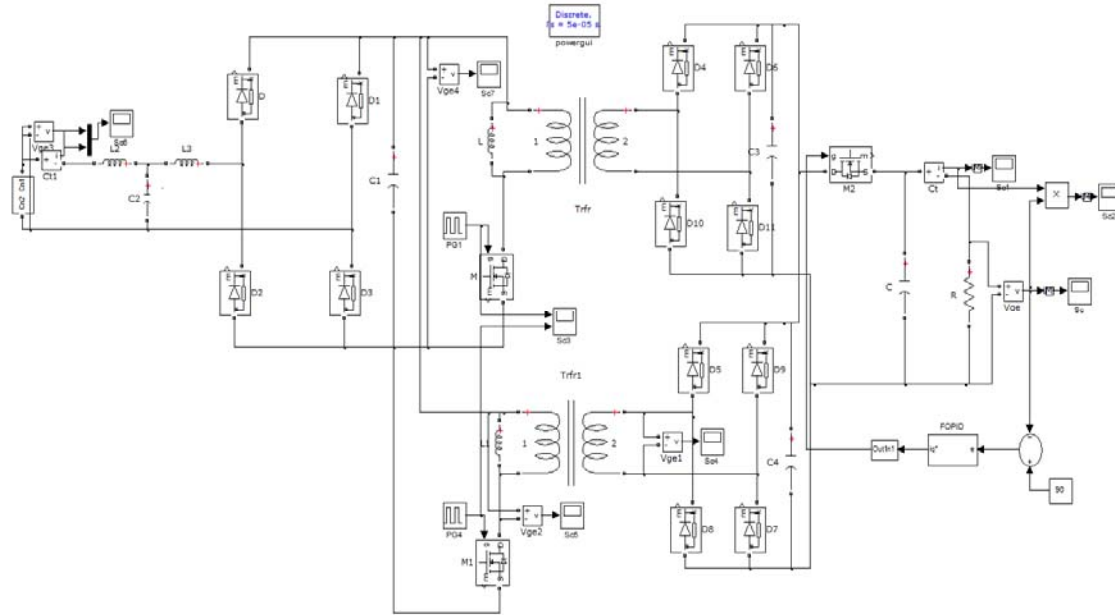


Figure 3(a). Simulation diagram of the closed loop CFSMPS with FOPID controller

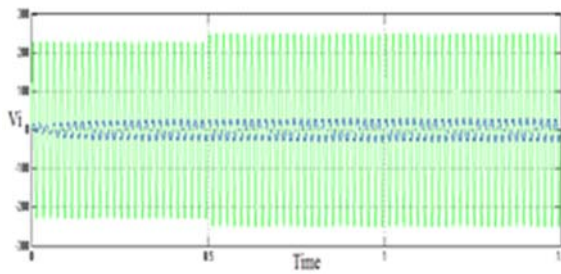


Figure 3(b). Input voltage

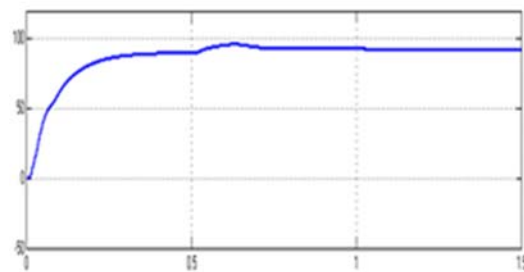


Figure 3(c). Output voltage

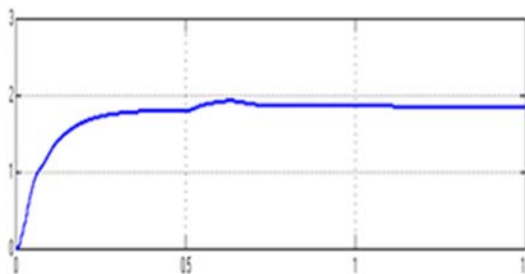


Figure 3(d). Output current

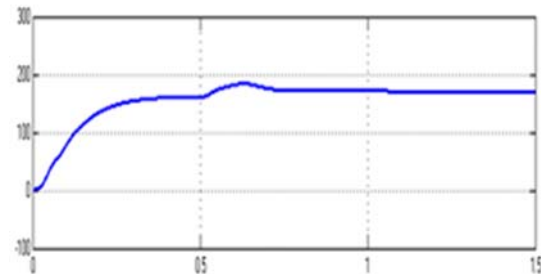


Figure 3(e). Output power

A comparison of time domain parameters is shown in Table-I. The abridgement of the settling-time t_s from 0.9 to 0.6 sec can be seen. The rise time t_r is reduced from 0.54 to 0.53 secs and the peak time t_p from 0.7 to 0.56 seconds respectively. The steady state error e_{ss} in the output voltage is abridged from 2.4V to 1.3 V. Therefore, the response with FO-P-I-D-controller is better than that of the P-I-controlled CFSMPS system.

Table 1. Comparison of Time Domain Parameters

Types of controller	t_r (sec)	t_p (sec)	t_s (sec)	e_{ss} (sec)
PI	0.54	0.70	0.9	2.4
FOP-I-D	0.53	0.56	0.6	1.3

5. CONCLUSION

A study of Simulation for open and closed-loop CFSMPS systems with PI and FOP-I-D controllers has been made. The experimental studies are done centered on Simulink models for CFSMPS systems. The findings connote that the FOP-I-D system having an enhanced response when compared to the PI controlled CFSMPS system. The benefits of the recommended CFSMPS system are low input current ripple, reduced settling time and a steady-state error. The reduction in current ripple is due to the cascading of flyback converters. The improvement in dynamic response is due to the use of FOPID controller. The drawback of CFSMPS is the increase in hardware count due to cascading. The scope of the current work is a comparison of FOP-I-D and PI controlled closed loop CFSMPS systems. A comparison of the response of CFSMPS with proportional resonant and Fuzzy logic controllers will be taken up as the work for the future.

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