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Dead time influence on operating modes of transistor resonant inverter with pulse frequency modulation (PFM)

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ABSTRACT

This study explores the impact of dead-time on the transistor resonant inverter operating modes depending on the ratio of the transistor switching frequency and the resonant frequency of the series-resonance circuit in the diagonal of the transistor bridge. On the basis of theoretical data and experimental results, a dead-time limitation relation has been offered - besides for a minimum value but for a maximum value. This provides extension of the operating mode range in zero voltage switching (ZVS).

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1. INTRODUCTION

The need to introduce dead-time in the controlling of single leg transistors in the schemes of the power electronic converters is known. This is the time, which the signal for switching on of each of the transistors delays with respect to the shutoff signal of the other. In some articles, the necessity of such a time is only mentioned [1], while in others are researched the processes related to it in voltage source inverters, resonant inverters and DC/DC converters, as different ways for its definition and implementation are offered. In [2] the time is recorded on the graphical time diagrams, but the processes are not studied. In [3] is considered a DC/DC converter with a zero voltage switching (ZVS) algorithm, as the dead-time calculation is based on the input capacitance of the MOSFET and the processes associated with the gate charge during switching. With regard to transistor resonant inverters, one of which is explored in this article, the following systemization can be done. Some companies recommend fixed set-up by external resistor in the integrated control circuit, providing the corresponding graphical dependencies [4, 5]. In [6] a fixed value equal to $330nS$ is set. In most studies, dead-time is determined based on the recharging of the output capacitances of the single leg MOSFETs, as the offered formulas for calculating its minimum value are almost identical [7-10]. A similar formula is offered in [11], as the delay time in the drivers is added. When examining a transistor resonant inverter for induction heating in [12], Pulse Frequency Modulation (PFM) is used and dead-time is introduced, but the processes in it are not researched. In [13] this time is optimized based on the ratio between the resonance capacity and the transistor drain-source capacitance, taking in mind the maximum switching frequency. Manual tuning based on the experimental loss measurement in the converter is suggested in [14]. The article [15] is interesting, as besides the minimum value limitation, it offers maximum value limitation as well. There are adaptive dead-time definitions, for example [16], presenting an

adaptive adjustment scheme in the range of $0 \div 3.5\mu S$, suitable for high voltage applications. In [17] is presented a method for compensating dead time, based on a complex form of the modulation signal .As a summary of all the described can be concluded that the studies consider the development of the processes in the power scheme when the dead-time is insufficient in value.

Quite often, however, the designers choose a higher value than needed, to be secured in case of load and power transistor parameters changes. No publications are known on how the operation modes change in case the dead-time has much greater value. The problem is: if this time is much greater, the zero voltage switching mode of the resonant inverters changes. This increases the losses on the transistors and reduces the efficiency. The aim of this study is to present a research of the impact on dead-time operating modes with significant (2 to 3 times) higher value than the needed one. This is done with a transistor bridge resonant inverter, for induction heating application for example. Based on the analysis, the authors propose a new solution: except for a minimum value, dead time should be limited to a maximum value, and mathematical dependence is derived.

Part 2 presents general theoretical information. Part 3 - the results of experimental researches, done in a slightly more unusual approach - the theoretical time diagrams and experiment oscillograms are shown next to each other. On the basis of the experimental results in Part 3, theoretical conclusions and recommendations for the choice of dead-time are made in Part 4.

2. THEORETICAL DATA

Figure 1 shows a power circuit diagram of a bridge transistor resonant inverter designed for induction heating, with constant voltage $U_d$supply. Depending on the load, by equivalent transformations the diagram in the diagonal of the bridge can be turned into a series-resonance circuit for which the following resonance condition is fulfilled.

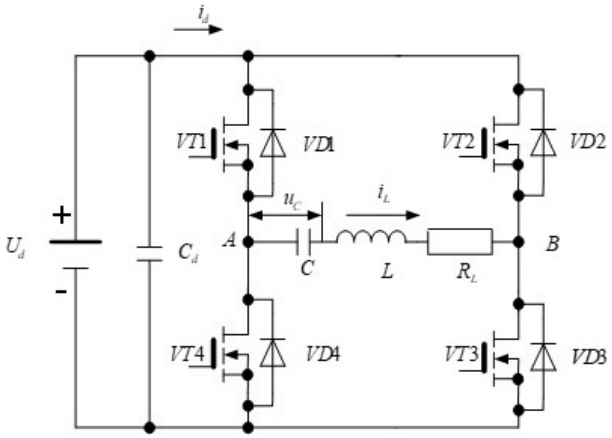


Figure 1. Bridge transistor resonant inverter scheme

$$R_L < 2.\sqrt{\frac{L}{C}}, \quad (1)$$

It is known that the own resonance frequency of the circle is determined by the dependence

$$\omega_0 = \sqrt{\frac{1}{L.C} - \delta^2} \quad (2)$$

where

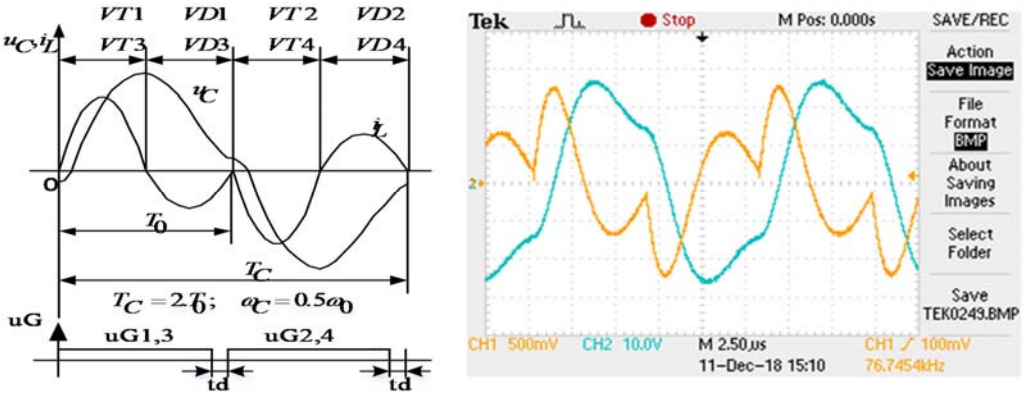
$$\delta = \frac{R}{2.L} \quad (3)$$

is the damping ratio. There is another frequency for the inverter ω_C - switching frequency of the transistors set by the inverter control system. The adjusting of the output power is via Pulse Frequency Modulation (PFM) - change of the switching frequency while maintaining symmetric control of the diagonally connected transistors - 50% duty cycle if dead-time is neglected.

Depending on the ratio between the actual resonance frequency of the circle ω_0 and the switching frequency ω_C, different operation modes are known - with a frequency below or above the resonance, in resonance mode, in which the current through the diagonal can be interrupted or continuous. By mathematical analysis, respective mathematical dependencies can be obtained and can be drawn graphical dependencies for the conduction times of transistors and diodes in the scheme, as it is done in [18], not taking in mind the dead-time. The theoretical information presented here is completed in Part4 with theoretical conclusions based on experimental research. Deliberately, the recharging of the output capacitances of the single leg transistors is ignored, which as is known happens at the beginning of the dead-time. This is done to differentiate the regimes in terms of the conductivity range of the semiconductor devices in the circuit.

3. EXPERIMENTAL RESEARCHES

The oscillograms presented here are from experiments under the following conditions: inverter supply voltage $U_d = 200V$, used transistors - IRF450. The capacitances of these transistors are as follows: output capacitance - $C_{OSS} = 600pF$, feedback capacitance - $C_{RSS} = 240pF$. The maximum value of drain current in the design and implementation of the resonant inverter is $I_{DSM} = 1.5A$. At load changing, this maximum value is $I_{DSM} = 15A$, but at the design the smaller value is taken, as dead-time is inversely proportional to the maximum current value. The calculations based on this data, using the formulas from page 18 of [11] and formula (7) of [7] give approximately the same result for the minimum dead-time value by calculation$t_{dcalc} \approx 200nS$. In the practical implementation, the dead-time value is firmly established $t_d = 600nS > t_{dcalc}$. For all the oscillograms shown below, the CH1 current is monitored with a current probe with 1:1 ratio and the voltage of CH2 with voltage probe with 10:1 ratio.



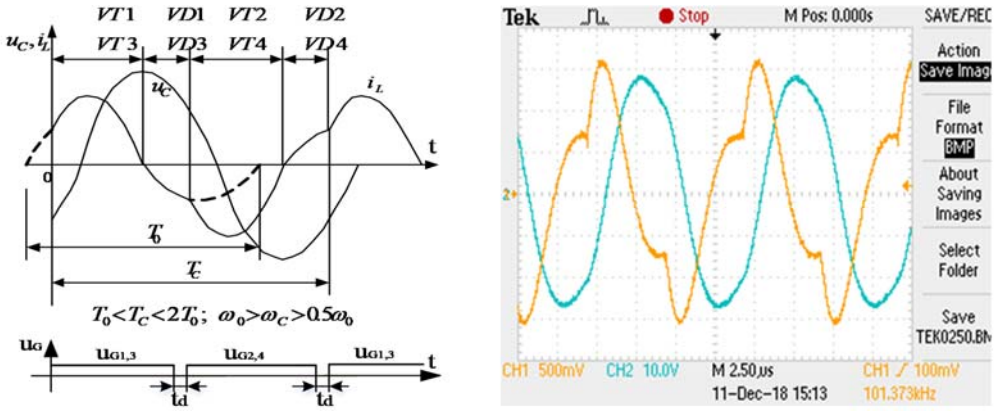
(a) (b)

Figure 2. Operating mode at $\omega_C = 0.5\omega_0$ with dead-time consideration. (a) theoretical time diagrams of the current through the series-resonance circuit i_L and the voltage of the resonant capacitor u_C; (b) oscillograms of the current through the series-resonance circuit i_L - ch1 and the voltage of the resonant capacitor u_C - ch2

Figure 2(a) shows that during the dead-time t_d for the consecutive pair of diagonally connected transistors the conduction is done by the reverse diode of the other pair of transistors. This does not affect the mode of operation of the resonant inverter – Figure 2(b). The same is the case at $0.5\omega_0 < \omega_C < \omega_0$ Figure 3(a) and Figure 3(b).

The theoretical mode of resonance $\omega_C = \omega_0$, ideally, without dead-time consideration, is illustrated with the time diagrams in Figure 4. It can be seen that the reverse diodes do not conduct, i.e. there is no return of energy from the load circuit back to the power supply. If the control system supports this theoretical mode, it would provide maximum energy efficiency. When entering the dead-time in the resonance mode,

immediately after switching off the consecutive pair of diagonally connected transistors, their reverse diodes conduct – Figure 5(a) and Figure 5(b). It turns out that this mode is similar to that shown in Figure 3, regardless of the difference in ratio of the frequencies ω_0 and ω_C .



(a) (b)

Figure 3. Operating mode at $0.5\omega_0 < \omega_C < \omega_0$ with dead-time consideration. (a) theoretical time diagrams of the current through the series-resonance circuit i_L and the voltage of the resonant capacitor u_C; (b) oscillograms of the current through the series-resonance circuit i_L - ch1 and the voltage of the resonant capacitor u_C - ch2

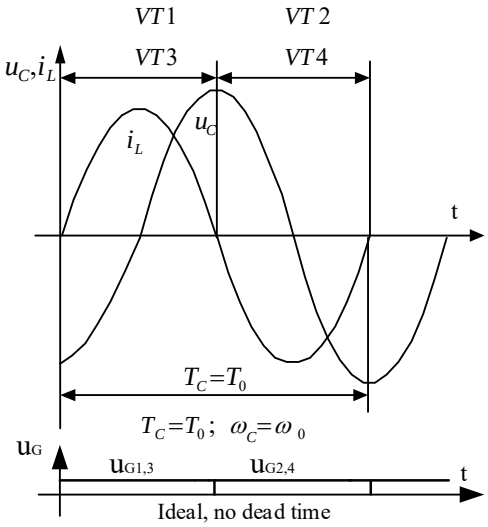
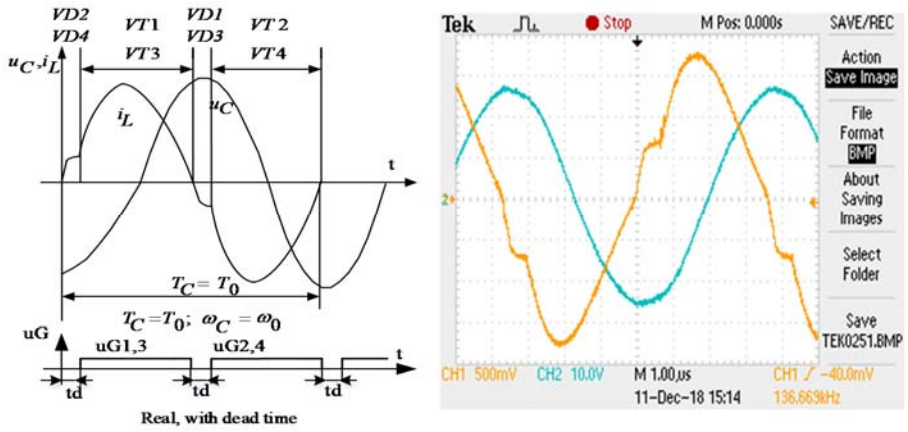
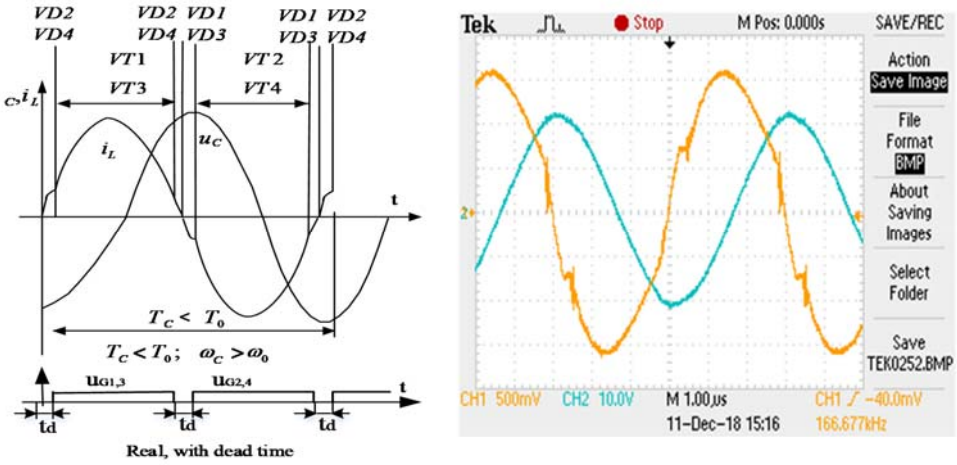


Figure 4. Operating mode at $\omega_C = \omega_0$ without dead-time consideration. Theoretical time diagrams of the current through the series- resonance circuit i_L and the voltage of the resonant capacitor u_C



(a) (b)

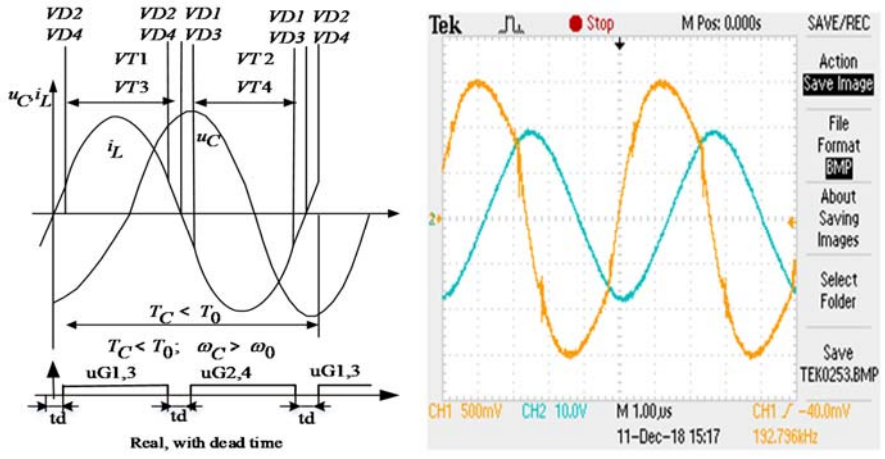
Figure 5. Operating mode at $\omega_C = \omega_0$ with dead-time consideration (the start of this time is after the current has passed through zero value). (a) theoretical time diagrams of the current through the series resonance circuit i_L and the resonant capacitor voltage u_C; (b) oscillograms of the current through the series resonance circuit i_L- ch1 and the voltage of the resonant capacitor u_C - ch2



(a) (b)

Figure 6. Operating mode at $\omega_0 < \omega_C$ with dead-time consideration (the beginning of the time is before the current has passed through zero value). (a) theoretical time diagrams of the current through the series-resonance circuit i_L and the resonant capacitor voltage u_C; (b) oscillograms of the current through the series- resonance circuit i_L - ch1 and the voltage of the resonant capacitor u_C - ch2

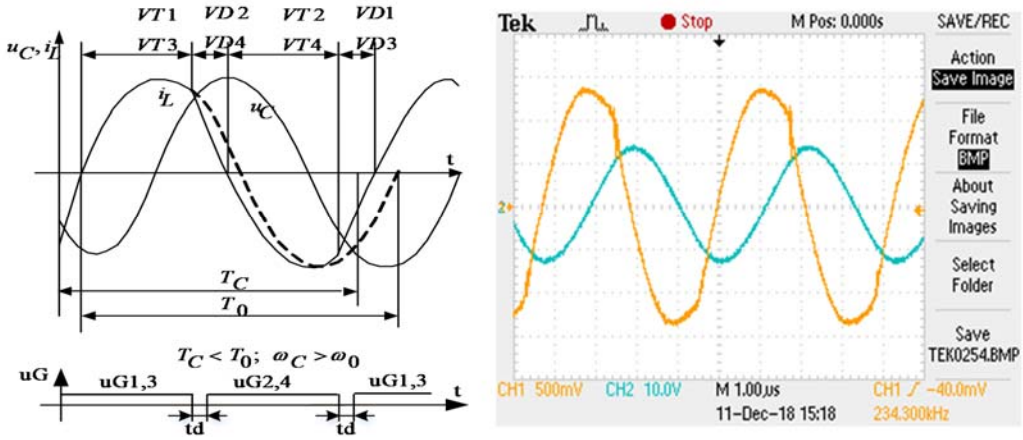
The operating modes shown in Figure 6 and Figure 7 are not described in the literature and are due only to dead-time, although the switching frequency is higher than the resonance frequency. Typically, this mode of operation in the absence of dead-time, is expected to provide ZVS. The interesting in both modes is the alternation of conduction intervals of one pair of diagonally connected diodes with the other pair of diagonally connected diodes. In Figure 7, the duration of the two intervals is the same. As you can see, both of the modes do not provide ZVS. In the case shown in Figure 8, when the dead-time coincides in duration with the conduction interval of a pair of reverse diodes before the switching of their respective transistors, ZVS is provided.



(a) (b)

Figure 7. Operating mode at $\omega_0 < \omega_C$ with dead-time consideration (the beginning and the end of this time are symmetrically spaced to the current flow through zero value). (a) theoretical time diagrams of the current through the series- resonance circuit i_L and the resonant capacitor voltage u_C; (b) oscillograms of the current through the series- resonance circuit i_L- ch1 and the voltage of the resonant capacitor u_C - ch2

Namely this borderline case is used below to set the maximum dead-time limitation. This case is taken in mind, because at the further increase of the frequency of switching during dead-time always the reverse diode of the respective transistor conducts and ZVS is implemented.



(a) (b)

Figure 8. Operating mode at $\omega_0 < \omega_C$ with dead-time consideration (the end of this time is before the current has passed through zero value). (a) theoretical time diagrams of the current through the series- resonance circuit i_L and the resonant capacitor voltage u_C; (b) oscillograms of the current through the series- resonance circuit i_L - ch1 and the voltage of the resonant capacitor u_C - ch2

4. THEORETICAL CONCLUSIONS

From the shown in Part 3 can be concluded that apart from the minimum limit the dead-time must have maximum limit to provide a ZVS mode in a wider interval of frequency variation around the resonance value. It is sufficient to the recharging time of the output capacitances of the transistors [7, 11] t_{dcalc} to add the time for switching on the reverse diodes, i.e. to ensure

$$t_{dcalc} < t_d < t_{dcalc} + t_{ON} \quad (4)$$

The question is what is the value of time t_{ON}. Regarding the switching time of the diodes used in the DC/DC converters, there is a detailed study [19] showing that for the different types it ranges from 2 to 15 nS. In this case, however, it is about the reverse diode of MOSFET, which is actu ally a parasitic transistor in the structure. At the gate of the transistor there is no switch-on signal as it is in the synchronous rectifiers so this signal will be provided after dead-time. In this case, the published studies on synchronous rectifiers can not be used. From this point of view, it can be said that in the manufacturers' documentation there is no precise data on the time of switching on t_{ON} of the reverse diode. For example, with regard to the used here IRF450 transistors in [20] it is said: "Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD". Also for the sum of the inductances of the two terminals of the transistor, $LS + LD$ the value is 6.1 nH.

Taking in mind the above, the authors offers the following way of determining the time t_{ON}: Before starting the switch on of the MOSFET reverse diode, the capacity of the drain-source transistor needs to be current discharged through the diagonal of the inverter bridge to a voltage of approximately 0.6V. Therefore, it can be assumed that on the sum of the inductances $LS + LD$ is applied voltage with such value. Then the rate of current change through them and the reverse diode will be:

$$S = \frac{di_{ON}}{dt_{ON}} \approx \frac{0.6}{LS+LD} \quad (5)$$

Or in the described case

$$S = \frac{di_{ON}}{dt_{ON}} \approx \frac{0.6}{6.1nH} \approx 0.1\frac{A}{nS} \quad (6)$$

Therefore, at known value of the current $i_L(t_{ON})$ which must be reached through the reverse diode

$$t_{ON} = S.i_L(t_{ON}) \quad (7)$$

For example, for the case shown in Figure 8(b) for $i_L(t_{ON}) \approx 1A, t_{ON} = 10nS$. At current value 10A the time would be 100nS.

5. CONCLUSIONS

As a result of this study for the dead-time impact on the operating modes of bridge transistor resonant inverter, is established an operating mode around the resonance frequency with consecutive conduction of the pairs diagonally connected reverse MOSFET diodes, which has not been described till now. Here is offered a formula for the maximum limitation of dead-time value besides the known so far minimum value limitation. An example of how to use it is shown as well.

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