Asymmetric hybrid multilevel inverter with reduced harmonic using hybrid modulation technique

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ABSTRACT

This paper studies the Asymmetric cascaded three phase multilevel inverter developed with hybrid modulation technique applied for an industrial application. The aim of this paper to reduce the Total harmonics distortion in the cascaded multi level inverter by introducing the new concept to develop the three phase CMLI. This inverter has two segments, one segment has H-bridge inverter and another segment has sequential arrangement of power semiconductor switches with asymmetrical voltage source in the ratio of 1:2. Similarly develop the segments for other phases. This new topology is called as Hybrid MLI. This hybrid MLI is used to reduce the no of semiconductor device requirement and the Total harmonics distortion. The inverter is controlled by Phase disposition (PD) and alternative phase opposition disposition PWM technique (APOD). This control technique is used to minimize the current harmonic and increase the system performance. The circuit is simulated using Matlab circuit and its performance is compared using PD and APOD PWM techniques and verified with simulation results.

Keywords:
Alternative phase opposition disposition
Cascaded multi level inverter
Phase disposition
Pulse width modulation
Total harmonic distortion

1. INTRODUCTION

Power electronics converters are mostly used to convert low voltage DC into high voltage DC conversion and other conversion (AC to DC) applications due to their advancements. Many industries are required good quality and high power for running the equipment. Due to industry requirements many research works are going in the field of increasing power handling capacity and improve the power quality. In this paper discuss about reduce the harmonic using hybrid modulation technique and improve the power handling capacity of the inverter. MLI is used to improve the power quality and high-power applications [1-6]. Cascaded multi level inverter is discussed in [7-11] and it is superior compare than other multi level inverter topologies [7-11]. Cascaded multi level inverter is also further classified symmetrical and asymmetrical type. The symmetrical topology has equal voltage source and required more DC source and H-bridge inverter. Asymmetrical topology has unequal voltage source and less no of DC sources and H-bridge compare than symmetrical method [12-18].

The combination of two other inverter topologies is called as Hybrid topology. Hybrid topology has proposed further reduced the component and harmonics [19]. Many modulation techniques are developed for control the inverter and reduced the harmonic [20-25]. Each method has some advantage and disadvantages. The combination of neutral clamped three level inverter with H-bridge based three phases asymmetrical VSI fed three phase induction motor circuit is proposed in this paper. The proposed hybrid inverter is used to
reduce the harmonic and power handling capACity. This inverter is controlled by using hybrid modulation technique. The circuit operation and simulation results will be discussed in the following section.

2. CIRCUIT DESCRIPTION

The proposed three phase hybrid MLI which combines the asymmetrical neutral point diode clamped three level inverters with integrated h-bridge inverter fed induction motor circuit diagram is as shown in figure 1. This proposed circuit has asymmetrical input source, three level and H-bridge combination and motor load. The three-level inverter is used to distribute the power and increase the power handling capACity. This inverter switches are controlled by multi carrier PWM technique. The switching table is as shown in table 1 for single leg. Similarly, other two legs switches are triggered with 120-degree Phase shift from eACh phase. Table 1 shows the switching state of HMLI. The output voltage level is produced based on the voltage level required. For generating +3 VDC switch S1, S4, S5 and S8 are turned ON. Similarly, other voltage levels are also AChieved.

![Proposed 3 phase HMLI circuit diagram](image)

![Figure 1. Proposed 3 phase HMLI circuit diagram](image)

Table 1. Switching states of HMLI topology

<table>
<thead>
<tr>
<th>Level</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
<th>S8</th>
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<td>1</td>
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<td>0</td>
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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>-2V</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>-1V</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0V</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1V</td>
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<td>3V</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

3. CONTROL TECHNIQUE:

Multi carrier Sine PWM technique is applied for control the proposed inverter. In this method sine reference signal is compared with multiple triangle carriers with different voltage level. EACh carrier produces different voltage level of the inverter. PD and APOD method were generated for control the proposed inverter output. When eACh carrier signal is generated in opposite phase is called as phase opposite disposition PWM technique. This pulse generation method is as shown in Figure 2 (a) and Figure (b).
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4. SIMULATION RESULTS:

The simulation diagram has been developed for the proposed inverter. This inverter output voltage is controlled by multi carrier PWM technique. PDPWM method and APODPWM method are developed for determine the inverter performance. Figure 3(a) and Figure 3(b) shows the output phase voltage HMLI for resistive load. It has almost sinusoidal waveform the output phase voltage for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition as shown Figure 3(a) and Figure 3(b)

Figure 3. Output phase voltage for HMLI using a) PD b) APOD method (R LOAD)

Figure 4(a) and Figure 4(b) shows the output line voltage HMLI for motor load. It has approximately sinusoidal waveform The output line voltage for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown Figure 4(a) and Figure 4(b).

Figure 4. Output line voltage for HMLI using a) PD b) Figure 4. APOD method (motor LOAD)
Figure 5(a) and Figure 5(b) shows the load current HMLI for motor load. The load current for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown in Figure 5(a) and Figure 5(b).

![Load current HMLI for motor load](image)

(a) ![Load current HMLI for motor load](image)

(b) Figure 5. Load current for HMLI using a) PD, b) APOD method (motor LOAD)

Figure 6 shows the load current FFT analysis for HMLI. As a result this current output has less current harmonic. The load current FFT analysis for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown in Figure 6(a) and Figure 6(b). Figure 7 shows the rotor speed of motor connected with HMLI. The rotor speed for 7 level hybrid multi level inverter using phase opposition, phase disposition and Alternative phase opposition and disposition are as shown in Figure 7(a) and Figure 7(b). Figure 8 shows the rotor torque in HMLI. The rotor torque for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown in Figure 8(a) and Figure 8(b).

![FFT Analysis for output current (m=1) using, a) PD, b) APOD method (motor LOAD)](image)

(a) ![FFT Analysis for output current (m=1) using, a) PD, b) APOD method (motor LOAD)](image)

(b) Figure 6. FFT Analysis for output current (m=1) using, a) PD, b) APOD method (motor LOAD)

![Rotor speed in rpm, a) PD b) APOD method (motor LOAD)](image)

(a) ![Rotor speed in rpm, a) PD b) APOD method (motor LOAD)](image)

(b) Figure 7. Rotor speed in rpm, a) PD b) APOD method (motor LOAD)
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5. COMPARATIVE ANALYSIS:
Both PDPWM and APODPWM methods are used to determine the proposed inverter performance. PD method has less harmonic compare than APOD technique by varying modulation index from 0.7 to 1. It is shown from Table 2 and Figure 9. Inverter output voltage has more distortion in APOD PWM method compare than PDPWM method.

<table>
<thead>
<tr>
<th>Modulation index</th>
<th>% of THD in PD technique</th>
<th>% of THD in APOD technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>4.3</td>
<td>4.28</td>
</tr>
<tr>
<td>.8</td>
<td>3.59</td>
<td>3.57</td>
</tr>
<tr>
<td>.9</td>
<td>2.62</td>
<td>2.70</td>
</tr>
<tr>
<td>1</td>
<td>1.75</td>
<td>1.79</td>
</tr>
</tbody>
</table>

6. CONCLUSION
The asymmetric cascade three phase multilevel inverter-based power supply proposed for AC motor application. This circuit is simulated using PDPWM and APODPWM method for compare the system performance. PD method has less current harmonic of 1.75% compare than APOD technique current harmonic of 1.79% by modulation index 1. Inverter output voltage has more distortion in APODPWM method compare than PDPWM method. PDPWM method gives better performance compare than APODPWM method. It is proved from simulation results. This proposed hybrid multilevel inverter has less components count compare than other multilevel inverter topology.

REFERENCES


