

Harmonic minimization of a single-phase asymmetrical TCHB multilevel inverter based on nearest level control method

Wail Ali Ali Saleh, Nurul Ain Mohd Said, Wahidah Abd Halim

Faculty of Electrical Engineering, Universiti Teknikal Malaysia Melaka, Malaysia

Center for Robotics & Industrial Automation, Universiti Teknikal Malaysia Melaka, Malaysia

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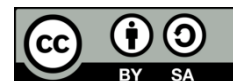
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ABSTRACT

Multilevel inverters are gaining special interest among researchers and in the industry due to their widespread applications and numerous merits. Obtaining high quality, more reliable output while using a reduced number of electronic components is the main purpose of most of the research conducted in this area of study. The purpose of this study is to apply the nearest level control (NLC) method to a 13-level transistor-clamped H-bridge (TCHB) inverter with unequal DC voltage supplies. The NLC method operates at the fundamental frequency, thus reducing switching losses, and can reduce the harmonic content significantly. The adopted multilevel inverter consists of two TCHB cells supplied with two asymmetrical DC input sources with a voltage ratio of 1:2. This structure reduces the number of electronic components, and the asymmetry in the DC input voltages results in a higher number of levels. The adopted topology and its proposed control method were simulated in Matlab/Simulink, and the simulation results were verified through experiments using an Altera field-programmable gate array (FPGA) board. The results showed that the topology and its control method are efficient in obtaining a high-quality output with an improved total harmonic distortion (THD).

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Corresponding Author:

Nurul Ain Mohd Said,

Faculty of Electrical Engineering,

Universiti Teknikal Malaysia Melaka,

Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.

Email: nurulain@utem.edu.my

1. INTRODUCTION

Multilevel inverters (MLIs) have become widely used in the industry, especially in medium/high voltage high power applications. Electric and hybrid vehicles, photovoltaic energy conversion and uninterruptable power supply (UPS) are just a few of the many applications available in the industry [1]. Researchers are exerting great efforts to develop better topologies of MLIs and better modulation methods and/or control strategies in terms of cost, size, efficiency and reliability. There are three main topologies of MLIs: Neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [1-3]. Many other topologies have been thoroughly investigated in the literature, such as the modular multilevel converter (MMC) [4] and the transistor-clamped H-bridge (TCHB) MLI [5, 6]. The TCHB MLI uses a reduced number of DC power supplies and switches to produce the same number of levels as compared with the conventional CHB MLI. Moreover, the TCHB inverter responds more effectively in reducing the harmonic content of output voltage and load current. According to the values of DC power supplies, some topologies of MLIs are classified into either symmetrical if these values are equal, or asymmetrical if they are unequal.

Asymmetrical topologies of MLIs [7, 8] produce a higher number of output levels while using fewer components as compared with the symmetrical ones.

High-switching frequency modulation techniques, such as multicarrier/multireference PWM [9-11] and space vector PWM [12] are efficient in obtaining a high-quality output; however, switching losses are dominant in such techniques. Low-frequency modulations are more efficient for high-power applications since they minimize switching losses. Selective harmonic elimination (SHE) [13-16], nearest vector control (NVC) [17], and nearest level control (NLC) [18-20] are the most commonly used low-frequency modulations in MLIs. The SHE method requires the solution of some nonlinear transcendental equations. However, as the number of levels increases, more equations exist whose solutions become more complicated and time-consuming. The working principles of NVC and NLC are approximately the same, except that the NVC considers the voltage vector nearest to the reference instead of the nearest voltage level in the case of the NLC [3]. Although the NVC is simple, it requires additional computational resources [21]. The NLC method is simple and more suitable for MLIs with a high number of levels. The NLC method is applied to asymmetrical CHB MLIs in [7] and [21]. The results show that the THD is reduced dramatically without the need for filtration. Switching losses are significantly reduced using the NLC method, especially in asymmetrical topologies with a high number of levels, since most of the power is delivered by the high power cell which commutates at the fundamental frequency [21]. The NLC method is also applied to a 21 level asymmetrical TCHB (A-TCHB) inverter in [8] with a DC link ratio of 1: 4 between two TCHB cells. The results show a significantly improved THD, however, the study does not discuss applying the method to a reduced number of levels (less than 21). After a precise review of the literature, it was found that few studies have been conducted on the NLC method applied to the TCHB inverter compared to MMC [22-25] and asymmetrical CHB MLI [7, 21]; Therefore, this paper focuses on applying the NLC method to a 13 level A-TCHB inverter with a DC voltage ratio 1: 2 between two TCHB cells. The method operates at the fundamental frequency and can be extended to any number of levels. The proposed NLC method is performed through simulation in Matlab/Simulink and the simulation results are verified through experiments using an Altera FPGA board.

2. THE ADOPTED 13-LEVEL A-TCHB INVERTER

The circuit diagram of the 13-level A-TCHB inverter is shown in Figure 1. The configuration consists of two TCHB cells supplied with unequal DC input voltages. The low-voltage cell (*cell 1*) is supplied with V_{DC} , and the high-voltage cell (*cell 2*) is supplied with $2V_{DC}$. The switching states of each TCHB cell individually are shown in Table 1. The 1: 2 voltage ratio was chosen since it is the smallest integer ratio for the two-cell configuration; hence any higher integer ratio can be assumed. The 13-level output is synthesized by adding the voltages of the two cascaded cells. Detailed voltage waveforms for each cell as well as for the inverter output are illustrated in Figure 2. Unlike the high-voltage cell, the low-voltage cell has many commutations per cycle. However, most of the power is delivered by the high-voltage cell which commutates at the fundamental frequency; thus, the switching losses are significantly reduced.

Table 1. Switching states of the TCHB cells

No	ON switches cell 1 (v_1)	Voltage level	ON switches cell 2 (v_2)	Voltage level
1	S_{11}, S_{41}	$+v_{dc}$	S_{12}, S_{42}	$+2v_{dc}$
2	S_{41}, S_{51}	$+\frac{1}{2}v_{dc}$	S_{42}, S_{52}	$+v_{dc}$
3	S_{11}, S_{21} (or S_{31}, S_{41})	0	S_{12}, S_{22} (or S_{32}, S_{42})	0
4	S_{21}, S_{51}	$-\frac{1}{2}v_{dc}$	S_{22}, S_{52}	$-v_{dc}$
5	S_{21}, S_{31}	$-v_{dc}$	S_{22}, S_{32}	$-2v_{dc}$

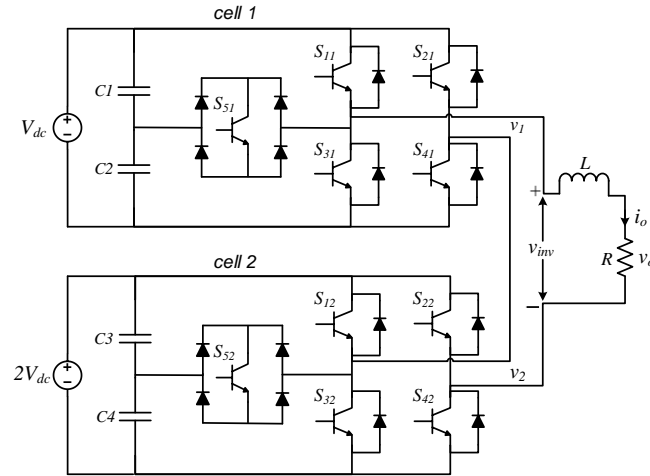


Figure 1. The 13-level asymmetrical TCHB inverter

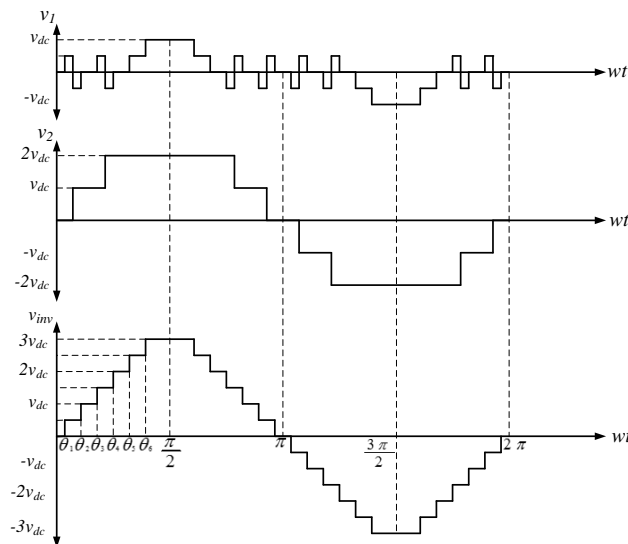


Figure 2. Low-voltage cell, high-voltage cell, and resultant 13-level output voltages, respectively

3. THE PROPOSED NLC METHOD

The proposed control strategy applied to the adopted inverter is called the nearest level control (NLC) method. The method is simple in its concept in which the output voltage level nearest to the reference is selected and gating signals are generated to the corresponding switches [7]. For A-TCHB MLI, the modulation index, M is generally defined as:

$$M = \frac{V_{ref}}{V_m} \quad (1)$$

where V_{ref} is the amplitude of the reference, and V_m is the total DC link voltage for i cells. V_m is calculated by:

$$V_m = \sum_{n=1}^i v_{dc,n} \quad (2)$$

For the 13-level A-TCHB inverter, since the voltage ratio between the two cells is 1: 2, according to (2), $V_m = v_{dc,1} + v_{dc,2} = v_{dc} + 2v_{dc} = 3v_{dc}$. Therefore M is directly proportional to V_{ref} . As an example:

To set M to 1, the value of v_{dc} is chosen to be $\frac{1}{3} V_{ref}$. So, $v_{dc,1} = \frac{1}{3} V_{ref}$ and $v_{dc,2} = \frac{2}{3} V_{ref}$. The implementation of the NLC method for the A-TCHB inverter by a comparison algorithm is shown in Figure 3. A sinusoidal reference, v^* is first fed to the high-voltage cell (*cell 2*). When the reference reaches certain voltage levels, $\pm h_{L,2}$, *cell 2* produces $\pm \frac{1}{2} v_{dc,2}$. Whereas, when the reference reaches $\pm h_{H,2}$, *cell 2* produces $\pm v_{dc,2}$. The unmodulated portion left by the five-level waveform of *cell 2* is then used as the reference and fed to the lower voltage cell (*cell 1*). Again, based on the voltage levels $\pm h_{L,1}$ and $\pm h_{H,1}$, *cell 1* produces $\pm \frac{1}{2} v_{dc,1}$ and $\pm v_{dc,1}$, respectively. The values of $h_{L,n}$ and $h_{H,n}$ are determined by:

$$h_{L,n} = \frac{1}{4} v_{dc,n}, \quad h_{H,n} = \frac{3}{4} v_{dc,n} \quad (3)$$

For mathematical analysis, the reference for the high-voltage cell is defined as:

$$v^* = v_2^* = V_{ref} \sin(\omega t) \quad (4)$$

This voltage reference is compared with the two constants $h_{L,2}$ and $h_{H,2}$. Then the gating signals are generated to the switches of the high-voltage cell using logic gates.

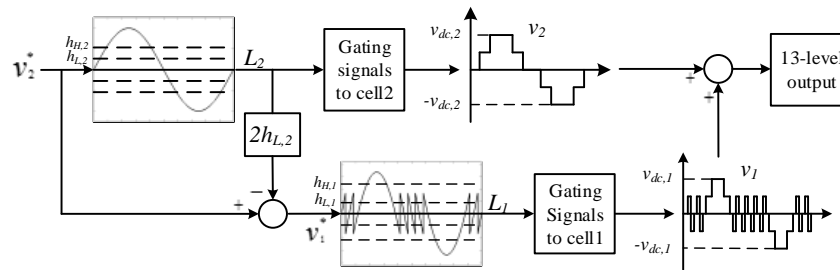


Figure 3. Implementation of the nearest level control method

The reference for the low-voltage cell is given by:

$$v_1^* = v_2^* - 2h_{L,2} * L_2 \quad (5)$$

where L_2 is the switching pattern resulting from the high-voltage cell after comparison and is given by:

$$L_2 = [(v_2^* > h_{L,2}) + (v_2^* > h_{H,2})] - [(v_2^* < -h_{L,2}) + (v_2^* < -h_{H,2})] \quad (6)$$

where the result of each comparison is 1 if true, or 0 if not. In the same way, the reference for the low-voltage cell is compared with $h_{L,1}$ and $h_{H,1}$. Then the gating signals are generated using logic gates to the corresponding switches of the low-voltage cell. The switching pattern resulting from the low-voltage cell is L_1 and is calculated in the same way as (6), considering the reference and constant values for the low-voltage cell.

4. ANALYSIS OF THE INVERTER OUTPUT VOLTAGE

The output waveform of the TCHB inverter is a quarter-wave symmetry; therefore, the output voltage can be represented using the Fourier series as:

$$V_{inv}(\omega t) = \sum_{n=1}^{\infty} b_n \sin(n\omega t) \quad (7)$$

where b_n is the Fourier coefficient. It equals zero for even n ; however, for odd n it is given by:

$$b_n = \frac{2v_{dc}}{n\pi} \sum_{i=1,3,5,\dots}^s \cos n\theta_i \quad (8)$$

where s is the number of switching angles in a quarter-wave and θ_i are the switching angles which should be within $[0, \pi/2]$. Table 2 shows the number of angles and voltage levels for a range of the modulation index. The number of levels reduces significantly as the modulation index decreases. The maximum number of levels achieved using the adopted configuration is 13 levels. The switching angles for the 13-level A-TCHB inverter at $M \geq 0.917$ depend only on $h_{L,1}$, since the output voltage remains the same when the inverter switches at $h_{H,1}$, as can be seen in Figure 2. Therefore, The switching angles can be calculated as follows:

$$\begin{aligned} \theta_1 &= \sin^{-1}\left(\frac{h_{L,1}}{M}\right), & \theta_2 &= \sin^{-1}\left(\frac{3h_{L,1}}{M}\right), & \theta_3 &= \sin^{-1}\left(\frac{5h_{L,1}}{M}\right) \\ \theta_4 &= \sin^{-1}\left(\frac{7h_{L,1}}{M}\right), & \theta_5 &= \sin^{-1}\left(\frac{9h_{L,1}}{M}\right), & \theta_6 &= \sin^{-1}\left(\frac{11h_{L,1}}{M}\right) \end{aligned} \quad (9)$$

The total harmonic distortion (THD) is given by:

$$\text{THD} = \frac{1}{Y_1} \sqrt{\sum_{n=2}^{\infty} Y_n^2} \quad (10)$$

where Y could be the voltage (V) or the current (I). The fundamental voltage V_1 , which is equal to b_1 , can be calculated at any value of M using (8) and (9).

5. RESULTS AND DISCUSSION

5.1. Simulation results

The simulation of the 13-level A-TCHB inverter and the applied NLC method is carried out in Matlab/Simulink. The simulation parameters were selected to match those of the experimental setup as shown in Table 3 to facilitate analysis and comparison of the results. The voltage THD evaluated throughout a range of M is shown in Figure 4. It is observed that the minimum voltage THD is achieved at $M = 1.044$ and is 5.18%. It can also be noticed that as M increases, the THD decreases. However, after $M = 1.044$, the THD increases with the increase in M . It can be inferred from Figure 4 that the NLC method presents high THD for inverters with a reduced number of levels and with low modulation indices [3], and this is the main drawback of the NLC method.

Table 2. Number of angles and voltage levels according to the modulation index

Modulation index (M)	Number of Angles	Voltage levels
$M \geq 0.917$	6	13
$0.75 \leq M \leq 0.916$	5	11
$0.584 \leq M \leq 0.749$	4	9
$0.417 \leq M \leq 0.583$	3	7
$0.25 \leq M \leq 0.416$	2	5

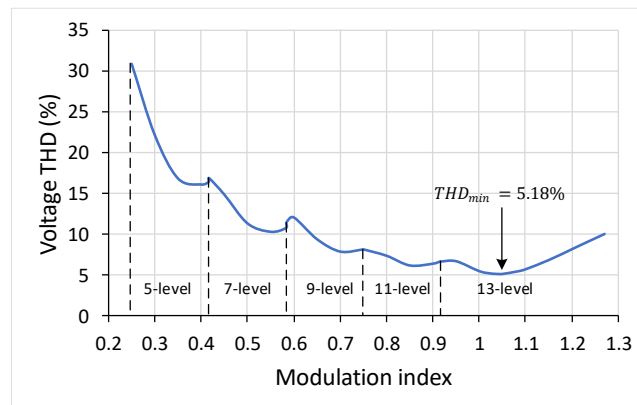


Figure 4. THD versus modulation index using NLC

The simulation results of the inverter output voltage and current using RL load at $M = 1$ are shown in Figures 5 (a) and (b), respectively. The THDs for both voltage and current are shown in Figures 5 (c) and (d), respectively. The voltage THD is 5.53%, and the current THD is 3.69% at $R = 100 \Omega$ and $L = 15\text{mH}$. If a bigger inductance is used, the current THD will reduce, and its waveform will be more close to sinusoidal.

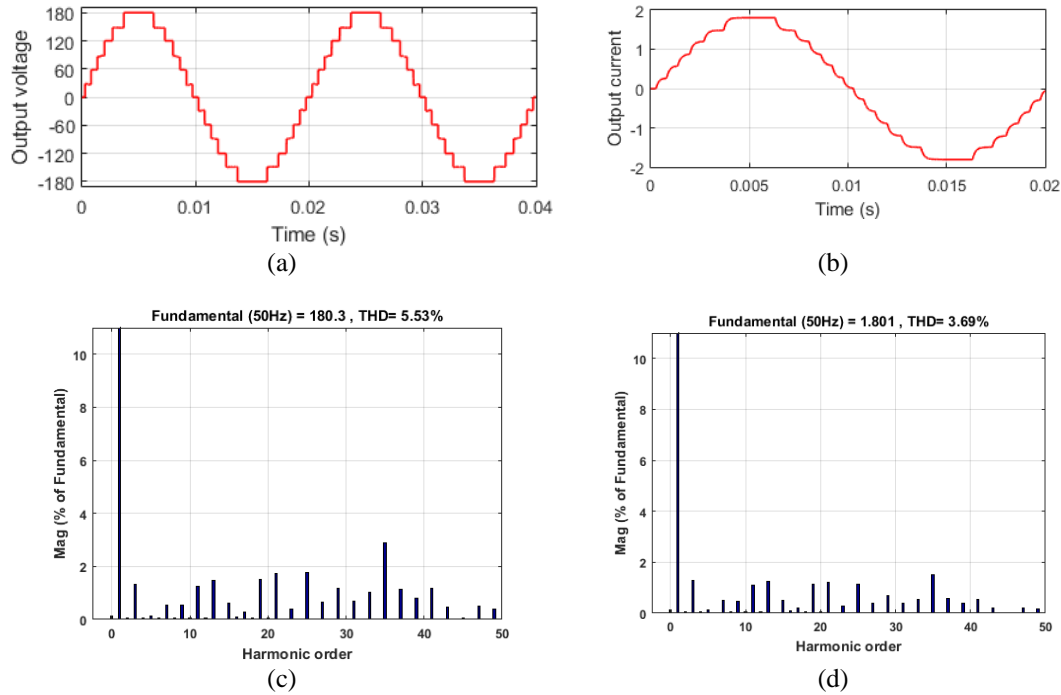


Figure 5. Simulation results using RL load at $M = 1$ (a) output voltage waveform, (b) load current waveform, (c) output voltage THD and (d) current THD

By comparing the results with those obtained in [26] using the SHE method for the same number of levels, it was noted that the minimum voltage THD using the SHE method is 6.70%, while in the case of the proposed NLC method, the minimum achieved voltage THD is 5.18%, as shown in Figure 5, which indicates a significant improvement in the voltage THD. Another comparison is made with [19] for the same control method, the same number of levels, but with different asymmetrical MLI topology. It was noted that at $M = 1$, the THD values of voltage and current in [19] are 6.30% and 0.35%, respectively, which are very close to the results obtained in this study (5.51% and 0.70% for the voltage and current THDs, respectively), considering similar values of R and L in both studies. However, the number of DC sources is higher in [19].

5.2. Experimental validation

To test the functionality of the inverter and its control method, a prototype was built in the laboratory. The control algorithm and the generation of gating signals were carried out using an FPGA board (Cyclone IV EP4CE22F17C6N). The experimental setup is shown in Figure 6, and the detailed system parameters are listed in Table 3. Another low-cost FPGA (Cyclone IV EP4CE6E22C8) is used to provide a dead time of $2 \mu\text{s}$ for the switching signals to prevent the switches from having a shoot-through fault. The FPGAs were processed using Quartus II software and programmed in the VHDL language. The output voltage and current of the inverter are displayed on the Tektronix TDS 2024C oscilloscope. The voltage and current THDs are measured using the Fluke 435 power quality analyzer.

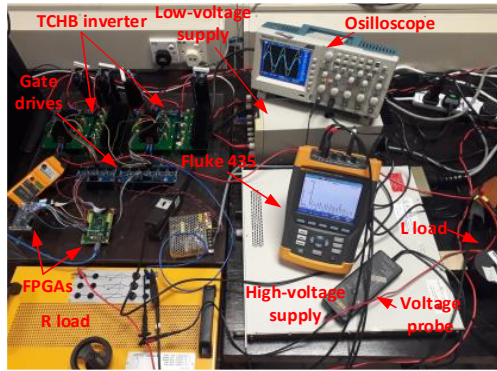
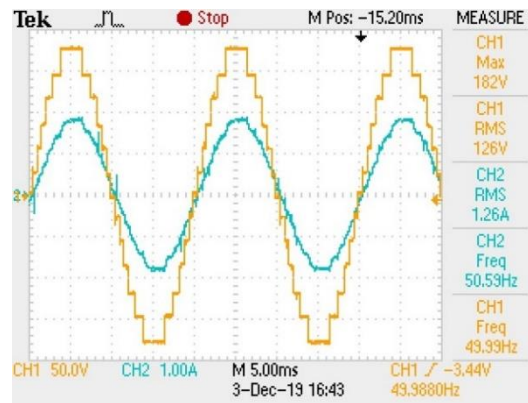
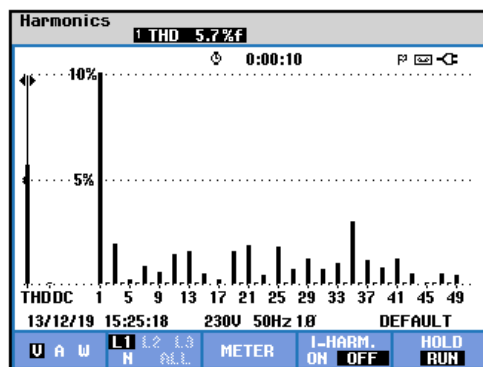


Figure 6. The experimental setup

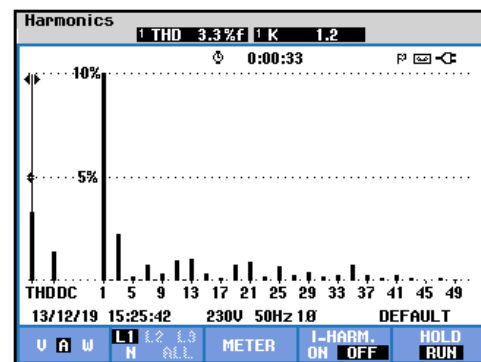
Table 3. System parameters for experimental tests

Parameter	Value
DC voltage for cell 1	60 V
DC voltage for cell 2	120 V
IGBT	IRG4PC50UD
Power diodes	RHRG30120
DC-link capacitors	2200 μ F
Load resistance	100 Ω
Load inductance	15 mH
Fundamental frequency	50 Hz

The experimental results for the output voltage and current of the inverter at $M = 1$ using RL load are shown in Figure 7. It can be seen that 13 voltage levels appear at the output and the current approaches a sinusoidal shape. The THDs of both voltage and current are 5.7% and 3.3%, as shown in Figures 8 (a) and (b), respectively. It was observed from the experiments that the minimum voltage and current THDs were recorded at $M = 1.044$ to be 5.2% and 2.7%, respectively.

Figure 7. Experimental results of output voltage and current at $M = 1$ using RL load

(a)



(b)

Figure 8. Measured results using RL load at $M = 1$ (a) Voltage THD and (b) Current THD

It should be noted that the NLC method does not eliminate specific harmonics like the SHE method, which eliminates some low-order harmonics; rather, it minimizes the overall THD of the inverter output. The simulation and experimental results of the voltage THD were compared at different values of M using R load as shown in Figure 9. It is noted that the simulation and experimental results are in close agreement with each other.

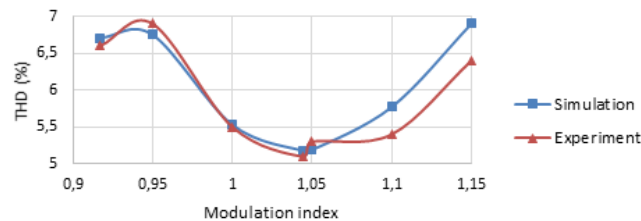


Figure 9. Total harmonic distortion versus modulation index

6. CONCLUSION

In this paper, the NLC method was applied to a 13-level A-TCHB inverter. The asymmetry in the DC supplies of the TCHB cells results in an increased number of output levels and therefore less THD. The asymmetrical topologies utilize a reduced number of DC power supplies and switches to produce the same number of levels compared to symmetrical ones. The NLC method is conceptual and simple to be implemented. The 13-level output starts at $M = 0.917$. A minimum voltage THD of 5.18% is achieved at $M = 1.044$. The simulation results indicate the efficiency of this method for obtaining high-quality output. The THD is calculated and analyzed at different values of the modulation index. The experimental results are in close agreement with the simulation results. The NLC method obtains a lower voltage THD compared to other low-switching frequency modulation methods, even though the required modulation index to produce the 13-level output is considered high ($M \geq 0.917$). Due to that, the NLC method is better suited for a high number of levels and high modulation indices. Further studies are needed to investigate the performance of the method in closed-loop applications.

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