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# Real time simulation of reduced switch multilevel inverter with PWM switching sequence control

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**ABSTRACT**

Reduction of switch count in symmetrical and asymmetrical reduced switch multilevel inverter designs has been proposed regularly with operation of conventional carrier-based pulse width modulation technique. In this study, a novel structure of symmetrical Hexa shaped model reduced switch seven level output inverter is proposed without any auxiliary switch and H-bridge. Proposed structure offers a smaller number of switch count and voltage sources which results in the cost and complexity reduction of its implementation. To operate the switching sequence of inverter from carrier based alternative phase opposition disposition (APOD), phase opposition disposition (POD), and phase disposition (PD) methods, suitable logical expression to be realize which gained more prominence. Active utilization of two voltage sources in each mode of operation results in significant reduction of voltage stress across each switch is achieved. A comparative study of proposed multilevel inverters (MLI) with various reduced switch MLIs has been presented. Initially, simulation model implementation has been carried out with MATLAB/Simulink and observed the performance parameters and total harmonic distortion (THD). Simulation results are carried for the comparison of the results obtained in the real time work performed on OPAL-RT 5700 simulator.



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## 1. INTRODUCTION

Various applications in electrical energy systems like electric vehicles, low power applications, high voltage DC transmission, flexible AC transmission, motor drives, uninterrupted power supplies, switch mode power supplies and integration and usage of various renewable energy sources are working with the crucial support of multilevel inverters (MLI) [1]–[6]. Various MLIs are proposed for the conversion of DC to AC in different voltage ranges with popular control topologies, well maintained power quality, low total harmonic distortion (THD) with unequal and equal DC link output voltage levels [7]–[9]. Conventional MLIs are classified as cascaded H -bridge, flying capacitor and neutral point clamped are absolutely advantages as multilevel output voltage. But these classic designs have cost complexity and more component count in their design and operation. To overcome the complexities of classic MLIs, reduced switch multilevel inverters (RSMLI) are proposed with various pulse width modulation (PWM) techniques for their switch controls. Symmetric and asymmetric MLIs are two types defined by the magnitudes of voltage sources used for the design of various RSMLIs [10].

Deep research studies are presented with various PWM methods for the RSMLI operated with different renewable energy sources. Literature study on various RSMLI is observed for 5, 7 and 9 level output voltages. To perform the mode of operations for different level in their proposed designs, various PWM techniques are used and proper methodology is used to generate the switching sequence pulse pattern [5], [11]. Brief observation and comparative study with switch count, number of capacitors, diodes and voltage sources as well as methodology used for the operation is given in Table 1. In proposed RSMLI, only two voltage sources and six active power switches are used without capacitors. Basic logic gates are used for the operation of switching sequence. Based on the comparative survey, proposed RSMLI is the total least count of elements with symmetrical operation of MLI.

Table 1. RSMLI comparison study with proposed Hexa MLI

| References | DC Voltages | MOSFET / IGBT | Diodes | Capacitors | Total elements | Output voltage level | PWM Technique | Methodology |
|---|---|---|---|---|---|---|---|---|
| [2], [12] | 4 | 5 | 0 | 0 | 9 | 7 | Bipolar (APOD, POD, PD) | Logic gates |
| [13] | 4 | 11 | 0 | 0 | 15 | 9 | Unipolar (APOD, POD, PD) | - |
| [14] | 2 | 7 | 4 | 2 | 15 | 9 | Bipolar (POD) | Logic gates |
| [1] | 2 | 8 | 0 | 0 | 10 | 7 | Bipolar (APOD) | Logic gates |
| [15] | 4 | 12 | 0 | 0 | 16 | 9 | Unipolar (APOD, POD, PD) | Logic gates |
| [16] | 3 | 7 | 3 | 0 | 13 | 7 | - | Fuzzy logic |
| [17] | 1 | 6 | 2 | 2 | 11 | 5 | Unipolar (PD) | K Map |
| Hexa MLI | 2 | 6 | 0 | 0 | 8 | 7 | Bipolar (APOD, POD, PD) | Logic gates |

In design and operation of reduced switch multilevel inverter, control of each switch with required pulse sequence is difficult. Comparing the number of pulse sequences produced from PWM method and the number of switches in RSMLI are not equal. Depends on the control strategy of each switch in RSMLI, problem statement of the proposed research work is on the generation of pulse sequences to the noval Hexa MLI. Organization of this article is presented in five sections. Section one presents the need and study of various reduced switch MLI. PWM strategy of proposed Hexa MLI for switching operations is explained in section two. Operation of proposed Hexa MLI and its various modes for the output level generations is provided in section three. Obtained results and discussion with RT-lab is given in section four. Proposed MLI with control technique and its comparison of THD is concluded in final section.

## 2. PWM STRATEGY FOR HEXA MLI

Different modulation strategies are analyzed and utilizing for the operation of conventional multilevel inverters and RSMLI. Considering for RSMLI, carrier based pulse width modulation techniques are preferable with "per carrier cycle" of multilevel inverter output voltage [18], [19]. Space vector modulation technique is direct method of carrier based PWM technique with pre-defined inverter state, carrier signal time length and modulation cycle [20]–[22]. In indirect method, low frequency modulation signal is intersection with high frequency carrier waves and results in pulse generation required for the operation of switching sequence [1], [23], [24]. Indirect method is easy to implement with intersection technique of carrier and modulation signal for the operation of reduced switch MLI. Saw tooth wave, trapezoidal wave, unipolar and bipolar sinusoidal waves are preferable for the modulation wave. Triangular waves are used as carrier waves based on the output voltage level of the proposed model [15], [25]. Multi carrier triangular waves are used for the generation of five level and more level output. Phase shift and level shift are the two methods of multi carrier PWM technique with the arrangement of carrier signals [17], [26]. In proposed model, level shift PWM with alternative phase opposition disposition (APOD), phase opposition disposition (POD), and phase disposition (PD) are used.

In APOD, each carrier triangular wave is in opposition with displacement of $180^0$ to phase of its alternative carrier wave. In POD, carrier waves on positive half side are in phase and carrier waves on negative half are in opposition displacement of $180^0$ with positive half carrier waves. In PD, all carrier waves are in phase without any phase opposition[27]. Variations of carrier arrangement in APOD, POD and PD are shown in Figure 1. Proposed Hexa MLI is operated for seven level output voltage. Based on the output voltage, count of carrier signals (C), amplitude of each carrier wave, amplitude of modulation wave ($A_m$) is considered for the multi carrier PWM operation to generate pulses as given in (1) and (2). Comparative intersection technique for

the generation of gating signals is shown in Figure 2. Generated pulses $P_1$, $P_2$, $P_3$, $N_1$, $N_2$ and $N_3$ are represented in binary sequence for the comparative algorithm with switching sequence of MLI.

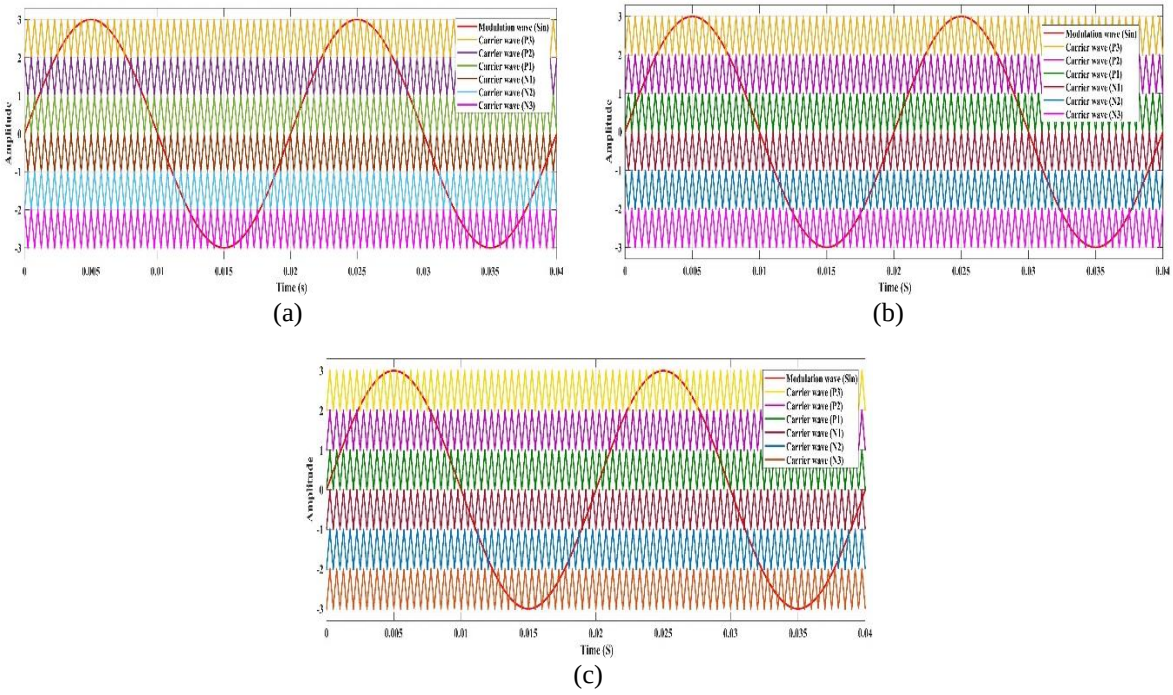


Figure 1. Multi carrier Pulse width modulation technique of; (a) alternate phase opposition disposition (APOD), (b) phase opposition disposition (POD), (c) phase disposition (PD)

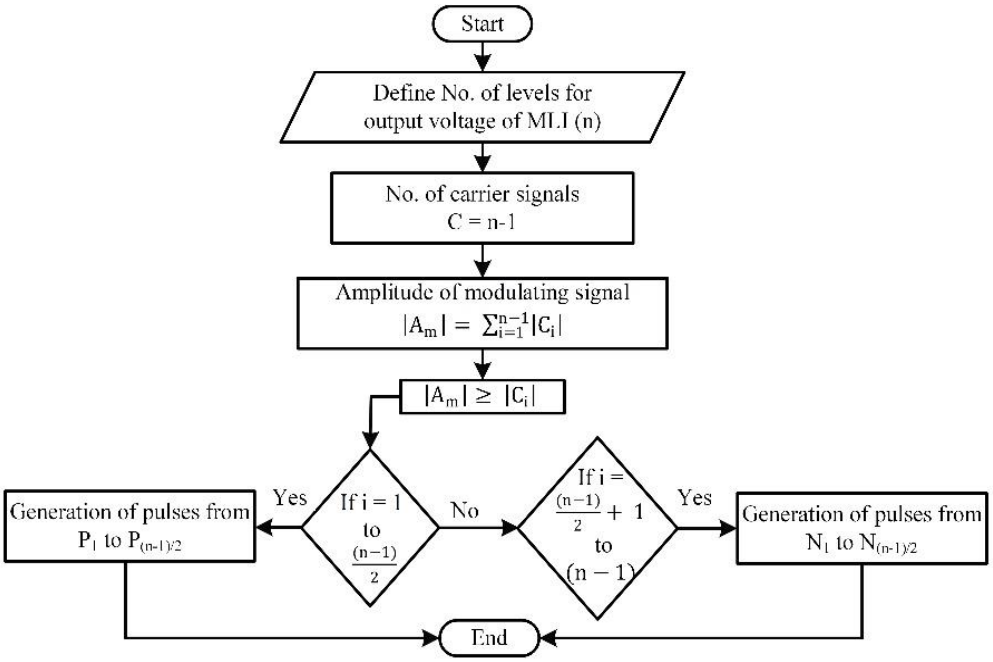


Figure 2. Flowchart of multi carrier PWM technique for reduced switch MLI

Amplitude of modulation wave,

$$|A_m| = \sum_{i=1}^{n-1}|C_i| \quad (1)$$

$$P_1 \text{ to } P_{\frac{(n-1)}{2}} \text{, If i= 1 to } \frac{(n-1)}{2} \quad |A_m| \geq |C_i| \quad \Rightarrow \left\{ N_1 \text{ to } N_{\frac{(n-1)}{2}} \text{, If i= } \frac{(n-1)}{2} + 1 \text{ to (n-1)} \right\} \tag{2}$$

By using bipolar modulation wave, n-1 carrier signals are used for 'n' level output voltage[28]. The switching sequence order of Hexa MLI is given in Table 2. Modulating frequency of 50Hz and switching frequency of 5 KHz is used for the entire operation of proposed model of PWM and inverter. A noval switching sequence comparative algorithm is performed for the generation of gating signal which is required for the operation of each switch and is presented in Figure 3. Variable 'K' represents the switch number of Hexa MLI and 'J' is the total number of switches in RSMLI.

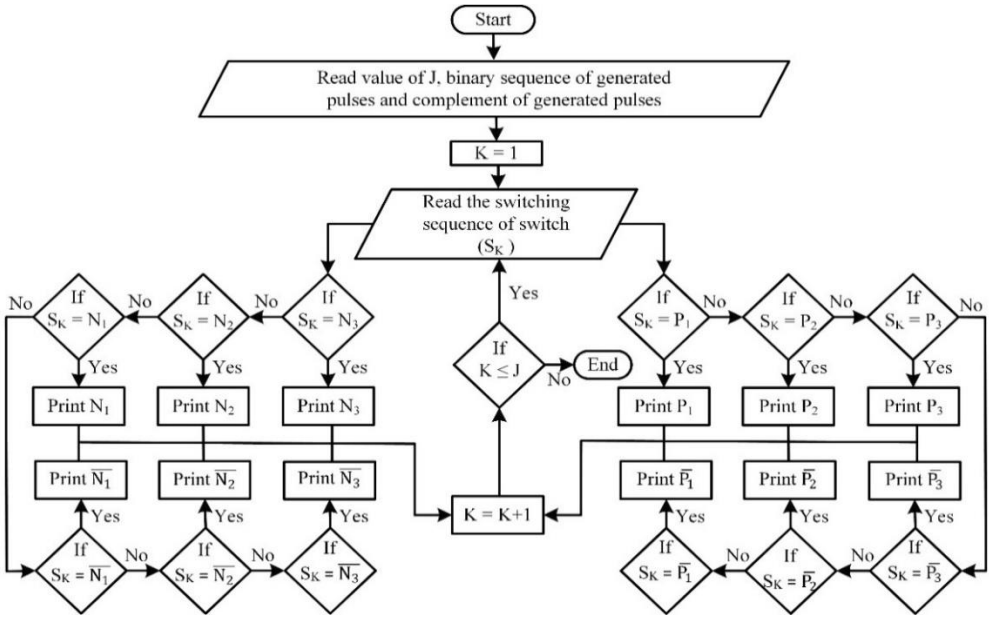


Figure 3. Flow chart of switching scheme for seven level Hexa MLI

Table 2. Switching sequence to control seven level Hexa MLI

| Mode of operation | Voltage level | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
|---|---|---|---|---|---|---|---|
| 1 | 2V | 1 | 0 | 0 | 1 | 1 | 0 |
| 2 | +1.5V | 1 | 0 | 0 | 1 | 1 | 1 |
| 3 | +1V | 1 | 1 | 0 | 1 | 1 | 1 |
| 4 | -1V | 1 | 1 | 1 | 0 | 1 | 1 |
| 5 | -1.5V | 1 | 1 | 1 | 0 | 0 | 1 |
| 6 | -2V | 0 | 1 | 1 | 0 | 0 | 1 |

## 3. HEXA MULTILEVEL INVERTER

Hexa MLI is the compact design of reduced switch multilevel inverter. It is operated with 6 power switches with anti-parallel power diodes to generate seven level output voltage. Auxiliary power switches are not used for the operation of level generation. Two symmetrical DC voltage sources ($V_{DC}$) are used for the unequal DC level output voltage of the Hexa MLI. Proposed Hexa MLI design is shown in Figure 4. Switches $S_1$, $S_2$, $S_5$, $S_6$ are used for the level generation and switches $S_3$, $S_4$ are for the polarity generation of output levels. Operation of each switch is explained in the various mode of operations. Unequal DC level outputs are $2V_{DC}$, $1.5V_{DC}$, $V_{DC}$, $0V_{DC}$, $-V_{DC}$, $-1.5V_{DC}$, $-2V_{DC}$. By excluding $0V_{DC}$, remaining output voltage levels are presented in six different modes of operations with resistive load.

- Mode 1: Three power switches are triggered with the support of PWM method. $S_1$ and $S_5$ are conducted for the level generation of $2V_{DC}$ and switch $S_4$ is operated for positive polarity. With the operation of single loop with two DC voltage sources, resultant voltage is the summation of voltages across the load. Flow of current through load and switches conducted in mode 1 is shown in Figure 5 (a).

- Mode 2: Switches $S_1$, $S_5$, $S_6$ are conducted for the level generation of $1.5V_{DC}$ and switch $S_4$ is for positive polarity generation. This mode is of two loops and an output voltage of one and half times of total voltage is obtained at load. Four conducted switches and current flow is shown in Figure 5 (b).
- Mode 3: $V_{DC}$ output voltage level is generated with the conduction of five switches and three loops are formed in Hexa MLI as shown in Figure 5 (c). Switches $S_1$, $S_5$, $S_6$ and $S_2$ are conducted for the level generation and $S_4$ is for polarity generation.
- Mode 4: Switches $S_6$, $S_2$, $S_1$ and $S_5$ are conducted for the output level generation of $-V_{DC}$. $S_3$ is conducted for the negative polarity generation. Current flow through the resistive load is reversed when compared to above three modes. Conducted switches and flow of current is shown in Figure 5 (d).
- Mode 5: $-1.5V_{DC}$ output voltage is generated by switching ON, $S_6$, $S_2$, $S_1$ with pulse sequence generated by PWM method. $S_3$ is conducted for negative polarity generation. One and half times of output voltage level with two loops formed by conducted switches in proposed Hexa MLI is shown in Figure 5 (e).
- Mode 6: Figure 5 (f) shows the operational mode of $-2V_{DC}$ with conducted switches and current flow direction through load. Switches $S_6$, $S_2$ and $S_3$ are conducted with single loop operation for maximum level of negative polarity generation.

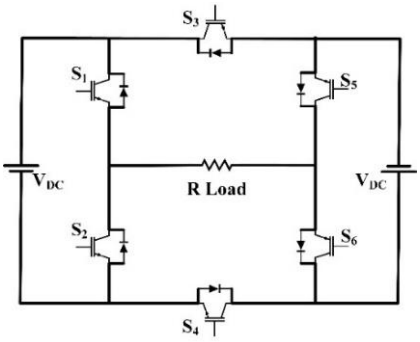


Figure 4. Proposed Hexa multilevel inverter

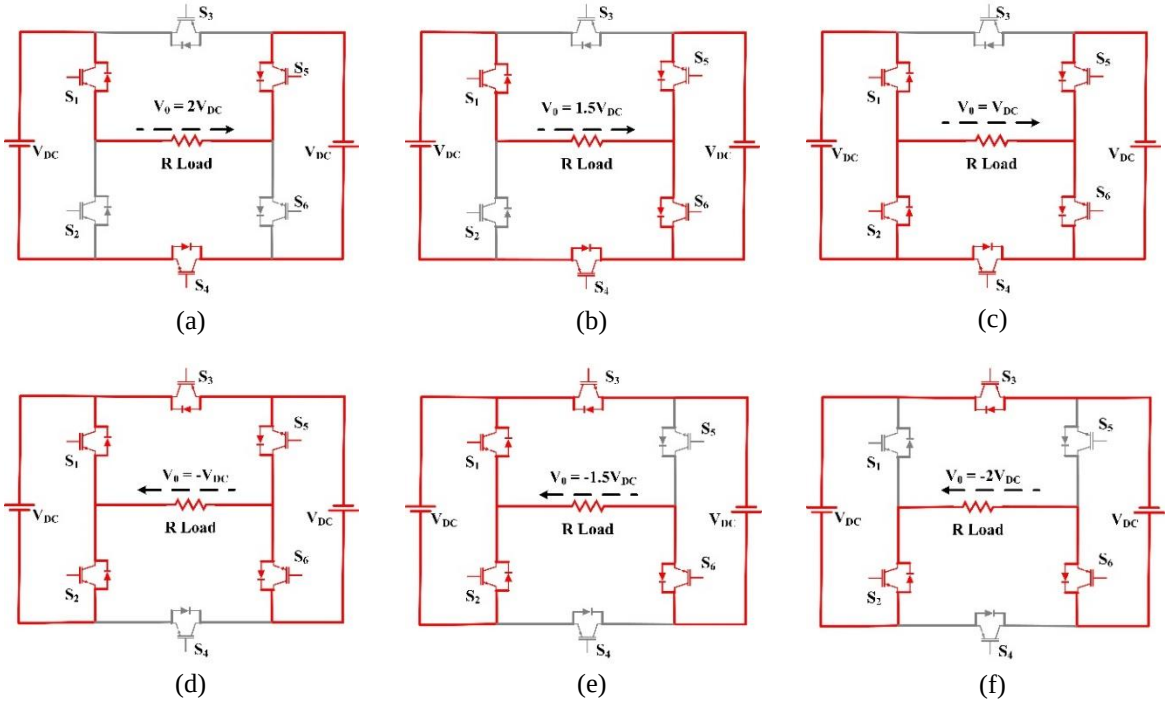


Figure 5. Various operational modes of Hexa MLI; (a) output voltage level of $2V_{DC}$, (b) output voltage level of $1.5V_{DC}$, (c) output voltage level of $V_{DC}$, (d) output voltage level of $-V_{DC}$, (e) output voltage level of $-1.5V_{DC}$, (f) output voltage level of $-2V_{DC}$

## 4. RESULTS AND DISCUSSION

Proposed Hexa MLI is designed and simulated with MATLAB/Simulink. Two symmetrical DC voltage sources of 24 V are connected in the design of Hexa MLI to generate seven level 48V output voltage across resistive load of 50 Ω. Primary criteria of the proposed work is to implement the operation of Hexa MLI with various PWM techniques. APOD, POD, PD are the preferred PWM techniques in the operation of Hexa MLI and the generated output voltage and current are observed with the various modulation index values. As a resultant to find the performance of the output parameters, THD observation of the proposed MLI is analyzed under various PWM techniques in simulation as shown in Figure 6.

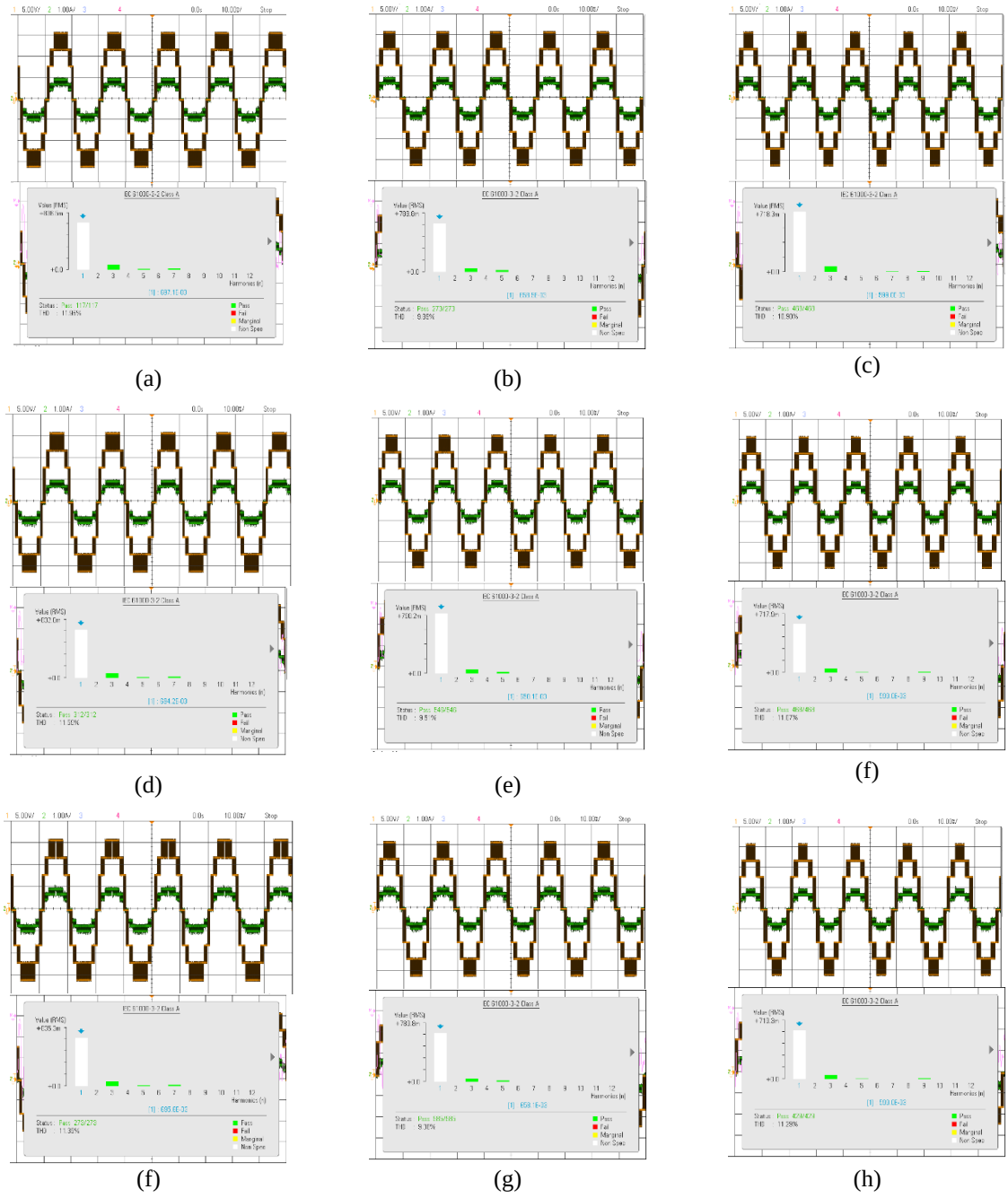


Figure 6. Seven level output voltage, current and their corresponding total harmonic distortion with, (a) APOD, Modulation Index 1, (b) APOD, Modulation Index 0.9, (c) APOD, Modulation Index 0.8, (d) POD, Modulation Index 1, (e) POD, Modulation Index 0.9, (f) POD, Modulation Index 0.8, (g) PD, Modulation Index 1, (h) PD, Modulation index 0.9, (i) PD, Modulation Index 0.8

To verify the obtained output parameters of the Hexa MLI in real time, proposed model is operated by OPAL-RT. Simulink model is built on the RT-LAB and loaded to the real time interface OPAL-RT 5700. Analog outputs of voltage and current of MLI in real time are recorded with digital signal oscilloscope. Maximum output range of OPAL-RT 5700 is from 16V to -16V. Obtained output voltage of 48V is scaled to limit of 16V and shown in Figure 6. Real time THD observation is recorded for the various carrier frequency PWM techniques at different value of modulation indexes from 1.1 to 0.7. Obtained output voltages, currents and their corresponding harmonic analysis are shown in Figure 6 with modulation index of 1, 0.9 and 0.8. Figures 6 (a)-(c) shows the performance parameters and THD analysis of Hexa MLI with APOD PWM technique. Figures 6 (d)-(f) shows the voltage, current and THD values of proposed MLI with POD technique. Figures 6 (g)-(i) shows output parameters of Hexa MLI with PD technique. The real time simulation experimental arrangement is shown in Figure 7.

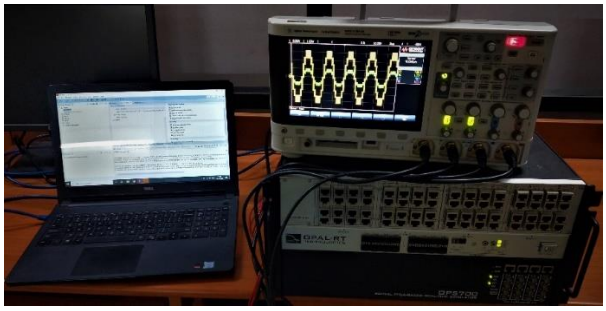

Figure 7. Real time simulation experimental setup with OPAL-RT 5700

Simulation and real time comparative presentation of resultant %THD of Hexa MLI under various carrier frequency PWM techniques at different modulation index values are given in Table 3. Simulation and real time THD values are meet the limits. PD PWM technique gives the better performance among three techniques. An optimal value of modulation index value is suitable for 0.9 based on the THD result analysis in three PWM techniques. Comparative observation between simulated THD and real time THD are shown in Figures 8 and 9 to find the better PWM technique and modulation index.

Table 3. Simulation and Real Time THD Comparison of HEXA MLI

| Modulation Index | Simulation | | | OPAL-RT | | |
|---|---|---|---|---|---|---|
| | APOD | POD | PD | APOD | POD | PD |
| 1.1 | 10.59 | 10.97 | 11.11 | 11.02 | 11.23 | 11.43 |
| 1 | 11.49 | 11.08 | 10.77 | 11.96 | 11.59 | 11.39 |
| 0.9 | 8.76 | 8.54 | 8.31 | 9.89 | 9.51 | 9.38 |
| 0.8 | 9.79 | 10.11 | 10.18 | 10.90 | 11.07 | 11.29 |
| 0.7 | 8.71 | 8.79 | 8.82 | 10.38 | 10.38 | 10.59 |

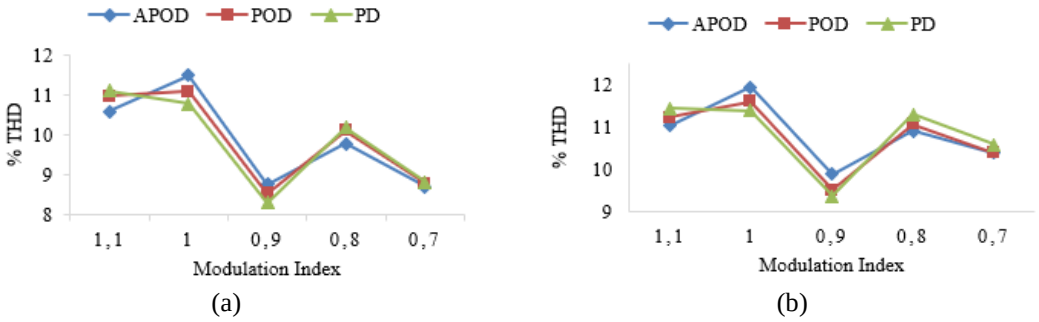


Figure 8. %THD comparison between simulation and OPAL-RT, (a) simulation comparative THD performance with APOD, POD and PD, (b) OPAL-RT comparative THD performance with APOD, POD and PD


Figure 9. %THD comparison between APOD, POD and PD, (a) THD comparision of simulation and OPAL-RT with APOD PWM technique, (b) THD comparision of simulation and OPAL-RT with POD PWM technique, (c) THD comparision of simulation and OPAL-RT with PD PWM technique

## 5. CONCLUSION

Hexa multilevel inverter with reduced switch count is modeled with simulation and real time platforms. Seven level output voltage is obtained across resistive load with only two DC voltage sources. Proposed MLI is validated with the various PWM methods and to find the best performance at different values of modulation index. Multi carrier PWM techniques with proper logical expression for the operation of Hexa MLI switching sequence is performed. Output voltage and output current are observed and recorded at different PWM techniques with their corresponding THD values with the use of OPAL-RT 5700 simulator. Comparative study of THD between simulation and real time of proposed Hexa MLI is performed and the percentage THD of both conditions are within acceptable standards.

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