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Low switching frequency modulation for generalized three-phase multilevel inverters geared toward Grid Codes compliance

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ABSTRACT

In this paper, a generalized three-phase multilevel power inverter (MLI) structure is proposed under asymmetric configurations. The operating mode and the switching combinations are briefly exposed according to the parity of the number of direct current (DC) voltage sources in use. Subsequently, the proposed topology is evaluated in terms of commonly used factors and then benchmarked against some of the state-of-the-art cascaded MLIs featuring multiple DC voltage sources (MDCS-CMLIs) while putting emphasis on the reduction of power switching devices. Moreover, a new nearest level control (NLC)-based modulation technique is designed for the purpose of better comply with some quality grid codes, namely the European EN 50160 and the International IEC 61000-2-12. The identification of the optimal control thresholds is realized by a constrained optimization algorithm (*e.g.*, particle swarm optimization (PSO)) which is implemented in python script and validated through SIMULINK fast fourier transform (FFT) analysis tool. Lastly, the harmonic performance of the proposed technique is compared side-by-side with that of the conventional NLC scheme and exhibits significant reduction in harmonic distortion.

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1. INTRODUCTION

In medium-voltage (MV) and medium-to high-power level conversion field, multilevel inverters (MLIs) are considered to be the flagship solution for grid-related applications including renewable energy sources integration, high voltage DC transmission/flexible AC transmission system (HVDC/FACTS), shunt active power filter (APF), and static synchronous compensator (STATCOM). Moreover, they are renowned as one of the most effective way to synthesize high resolution AC power endowed with attractive features such as low harmonic distortion, high power handling, and best power conversion efficiency to name a few [1]. Despite all of the aforementioned benefits, MLI topologies require a relatively large number of power semiconductor and passive components. To address this issue, a lot of research are led toward the reduction of the power components count so as to enhance both the overall power efficiency and the system reliability [2]-[4].

In practice, cascaded MLI structures with multiple DC sources (MDCS-CMLIs) are regarded to be the most authoritative MLIs since they have been employed in some renewable energy systems for more than a decade. They can be set either in symmetric or in asymmetric configuration [1], [5]. Asymmetric nature of DC

sources would bring more levels to the output waveforms which positively impact their harmonic performance. For this reason, only asymmetric structures are considered throughout this paper.

Low switching frequency modulations (LSFM) found their way in the field of MLI structures with the main objective of alleviating the switching losses incurred by the relative high number of power switches [6], [7]. Nowadays, there is only one well-established LSFM scheme geared toward grid-tied applications known as selective harmonic mitigation (SHM) which in turn is akin to the selective harmonic elimination (SHE) modulation technique [8]-[11]. However, SHE/SHM has some limitations that could be overcome by NLC [5], [12], especially those related to dynamic performance under real-time operation and computational effort required while using lookup tables or curve fitting polynomials or any initial guessing and iterative routines [13], [14].

The next section proposes a generalized three-phase MLI topology under different parity of k DC voltage sources. To evaluate performance, the inverter structure is analyzed in terms of some commonly used factors and compared to other state-of-the-art topologies. Afterwards, in section 3, a new NLC-based modulation is developed for the purpose of better meeting the grid quality requirements of both EN 50160 and IEC 61000-2-12 codes. In order to achieve that, some mathematical formulations based on fourier series expansion are shortly exposed. Next, the formulation of the optimization problem is given as a system of nonlinear inequalities considering each individual harmonic limit L_h and the total harmonic distortion (THD) of a given line-to-line output voltage $v_\ell(\omega t)$. Then, the particle swarm optimization (PSO) algorithm [15] is called to determine the appropriate switching angles θ_i depending on the voltage ratio r and the thresholds λ_i. Finally, the harmonic performance of the proposed control technique is benchmarked side-by-side against that of the conventional NLC scheme. Results and discussion are carried out while relevant conclusions are highlighted at the end of this paper.

2. ASSESSMENT OF THE PROPOSED MLI TOPOLOGY

2.1. Basic unit cell MDCS-CMLI structure

The proposed three-phase MLI topology is depicted by Figure 1 where the basic unit cell is shaded in light color. As it can be seen, each single-phase cell is made up from two voltage sources, four unidirectional ($S_{1,1}$, $S_{1,2}$, $S_{3,1}$, $S_{3,2}$) and two bidirectional power switches ($S^*_{2,1}$, $S^*_{2,2}$). Several unit cells can be strung together in series so as to synthesize high resolution output voltages. A comparative study with detailed operating modes for both 5-level symmetric and 7-level asymmetric configurations has already done in [16], so it will not be discussed further except for some reminiscent results required when designing the generalized structure.

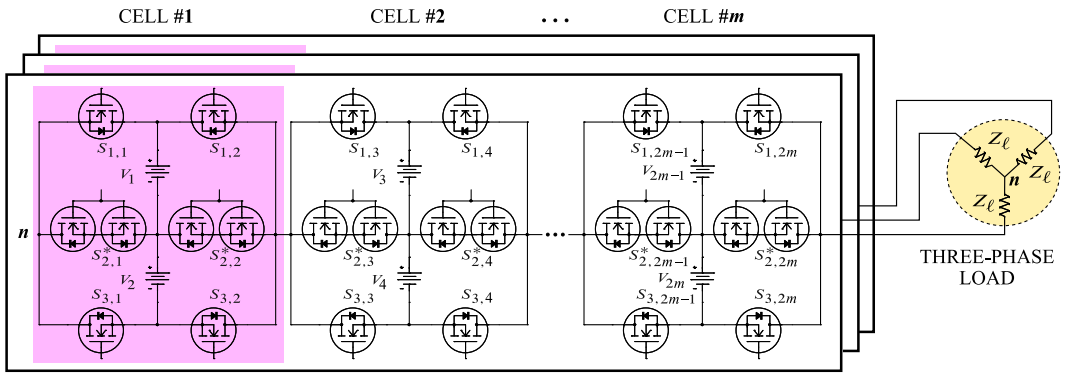

Figure 1. Proposed generalized three-phase multilevel power inverter topology. Basic unit cell is shaded in which bidirectional switches are illustrated by two back-to-back N-channel power MOSFETs

The focus of the present work was mainly driven toward grid-connected MLIs for renewable energy integration. Asymmetric nature of the discrete DC sources would be of great benefit in enhancing power quality required by the grid code. In each cell, a binary voltage ratio was used (*i.e.*, $r = V_2/V_1 = 2$) and for the sake of efficiency, bidirectional switches were made of two back-to-back N-channel power MOSFETs.

Two aspects of importance should be at the forefront when designing MLI topologies: total standing voltage (TSV) and total active switches (TAS). The former is defined as the sum of the highest voltage stress

across each power switch while the latter is the total number of conducting MOSFETs over one time period:

$$\begin{cases} \text{TSV} & = & 4(V_1+V_2)+2V_2=16V_1 \\ \text{TAS} & = & 32 \text{ MOSFETs}. \end{cases} \tag{1}$$

2.2. Extended MDCS-CMLI structure

The basic unit cell within the generalized structure of Figure 1 can be extended in two different ways according to the parity of the k number of DC voltage sources. For each phase, every unit cell is connected together in series so as to generate high-resolution output waveforms by virtue of arithmetic combinations of the DC power sources where their p.u. magnitudes V_k feature *septenary* configurations as follows:

$$\forall m \in \mathbb{N}^*, V_k/V_1 = \begin{cases} 7^{(k-1)/2}, & k=2m-1 \\ 2\,(7^{k/2-1}), & k=2m, \end{cases} \tag{2}$$

where m represents the number of basic unit cells being connected.

In order to build up all the available n levels and guarantee every time that any of the $2m$ DC voltage sources will never be short-circuited, then the following general rule should be applied:

$$S_{i,j} = \{0,1\} \Big| \prod_{j=1}^{2m} \sum_{i=1}^{3} S_{i,j} = 1, \tag{3}$$

$S_{i,j}$ correspond to the enhancement-mode NMOS, so '0' and '1' denote, respectively, the OFF- and ON-state. In addition, the available switch combinations for the generalized single-phase MLI are tabulated in Table 1.

Table 1. Switching combinations of the generalized single-phase MLI under asymmetric operation

	Per-Unit Output Voltage Levels (V_k/V_1)																	
	$\frac{1-7^m}{2}$	$\cdots$	-24	$\cdots$	-10	$\cdots$	-3	-2	-1	0	$+1$	$+2$	$+3$	$\cdots$	$+10$	$\cdots$	$+24$	$\cdots$	$\frac{7^m-1}{2}$
$S_{1,1}$	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON	OFF	ON	ON	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$S_{1,2}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	ON	ON	OFF	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON
$S_{1,3}$	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON	ON	ON	ON	ON	ON	ON	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$S_{1,4}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	ON	ON	ON	ON	ON	ON	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON
$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$
$S_{1,2m-1}$	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON	ON	ON	ON	ON	ON	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	OFF
$S_{1,2m}$	OFF	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON	ON	ON	ON	ON	ON	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON
$S^*_{2,1}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	ON	OFF	OFF	ON	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$S^*_{2,2}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	ON	OFF	OFF	ON	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$S^*_{2,3}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	ON	$\cdots$	OFF	$\cdots$	OFF
$S^*_{2,4}$	OFF	$\cdots$	OFF	$\cdots$	ON	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$
$S^*_{2,2m-1}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$S^*_{2,2m}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$S_{3,1}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	ON	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON
$S_{3,2}$	ON	$\cdots$	ON	$\cdots$	ON	$\cdots$	ON	ON	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$S_{3,3}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	ON	$\cdots$	ON
$S_{3,4}$	ON	$\cdots$	ON	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF
$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$	$\cdots$	$\vdots$
$S_{3,2m-1}$	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	ON
$S_{3,2m}$	ON	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$\cdots$	OFF	$\cdots$	OFF	$\cdots$	OFF

Depending on the parity of k number of DC voltage sources, the equations of the number of switches (N_{sw}), gate drivers (N_{gd}) and total standing voltage (TSV) for the proposed n-level power inverter are given

as shown in:

$$\begin{array}{ll|ll} \forall m \in \mathbb{N}^* \mid k = 2m, & & \forall m \in \mathbb{N}^* \mid k = 2m-1, & \\ n & = 7^{k/2} & n & = 3\,(7^{(k-1)/2}) \\ N_{sw} & = 8\log_7(n) & N_{sw} & = 8\log_7(n/3)+4 \\ N_{gd} & = 6\log_7(n) & N_{gd} & = 6\log_7(n/3)+4 \\ \mathrm{TSV} & = \sum_{i=1}^{k} 16V_i/3 & \mathrm{TSV} & = \sum_{i=1}^{k-1} 16V_i/3 + 4V_k \\ & = 8(n-1)V_1/3. & & = (20n-24)V_1/9. \end{array} \tag{4}$$

It is worth noting that the use of the last two bidirectional power switches (*i.e.*, $S^*_{2,2m-1}$ and $S^*_{2,2m}$, $m \geq 2$) is not justified when k is odd; only unidirectional are needed. Furthermore, and in order to estimate the overall cost-per-level involved in creating an n-level inverter structure, the cost function $\$(n,\beta)$ is taken into consideration with the assumption that all the switches in use share the same power rating [17], [18]. Depending on its values (greater or less than unity), the weight coefficient β is used to emphasize either the TSV_{pu} or the total number of required electric components:

$$\$(n,\beta) = (N_{sw} + N_{gd} + [N_c + N_d] + \beta\,\mathrm{TSV}_{pu})\,n^{-1}\,k, \tag{5}$$

where the per-unit TSV is defined as: $\mathrm{TSV}_{pu} = \mathrm{TSV}/\sum_{i=1}^{k} V_i$. However, topologies with power diodes N_d and/or electrolytic capacitors N_c are not considered here since they are generally lossy and/or bulky.

2.3. Comparative study with recent MDCS-CMLIs

A comparative study of some cutting-edge MDCS-CMLIs is performed in order to show the merits of the proposed structure [19]-[22]. Typically, the n is limited to 50 levels, which would be far enough for any grid-tied applications targeting either single- or three-phase inverters. As can be seen from Figure 2, the proposed topology requires the least number of $k(n)$ DC sources with moderate $N_{sw}(n)$, $N_{gd}(n)$ and p.u. $\mathrm{TSV}(n)$, resulting in the lowest cost function $\$(n,\beta)$ for both cases (*i.e.*, $\beta \leq 1$ and $\beta > 1$) regardless the parity of k.

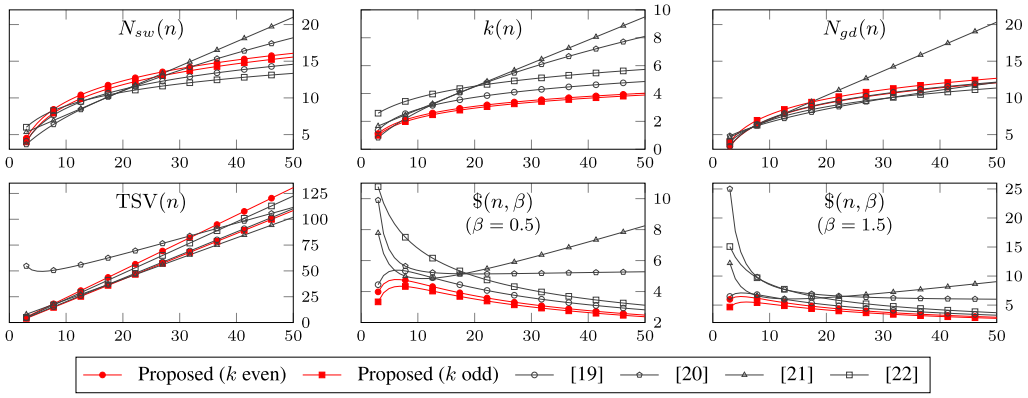

Figure 2. Comparison of the proposed asymmetric topology to some state-of-the-art MDCS-CMLIs

3. PROPOSED CONTROL STRATEGIES FOR GRID-TIED MLI TOPOLOGIES

3.1. Mathematical formulation of the proposed MLI output voltage waveform

The output voltage waveform of the proposed inverter driven by an NLC modulation is similar to a staircase sine wave function with equal riser ($r = 2$), and because of its odd quarter-wave symmetry property, the general form of the Fourier coefficient b_h is simplified as shown in with $a_h = b_{2h} = 0$ for all harmonics h:

$$\begin{aligned} b_h = \frac{4V_1}{\pi}\Bigg(&\int_{\theta_1}^{\theta_2} \sin h\theta\,\mathrm{d}\theta + \int_{\theta_2}^{\theta_3} r\sin h\theta\,\mathrm{d}\theta + \int_{\theta_3}^{\theta_4} (r+1)\sin h\theta\,\mathrm{d}\theta \\ &+ \cdots + \int_{\theta_{\frac{n-1}{2}}}^{\pi/2} (r+1) \sum_{m=2}^{\log_7(n)} (7^{m-1}+1)\sin h\theta\,\mathrm{d}\theta\Bigg) \end{aligned} \tag{6}$$

The fourier series of the phase voltage $v_\phi(\omega t)$ can then be written as a function of the voltage ratio r and the switching angles θ_i:

$$v_\phi(\omega t) = \sum_{h=1}^{\infty} b_h \sin h\omega t = \frac{4V_1}{h\pi} \sum_{h=1}^{\infty} \big[\cos h\theta_1 + (r-1)\cos h\theta_2 + \cos h\theta_3 + (5-2r)\cos h\theta_4 + \cos h\theta_5 + (r-1)\cos h\theta_6 + \cdots + \cos h\theta_{(n-1)/2}\big] \sin h\omega t \qquad (h : \text{odd harmonics}) \tag{7}$$

where θ_i is defined by (8), taking into account the number of available levels n and the thresholds λ_i. The introduction of the latter parameters allows to distinguish two operating modes regarding the symmetry or asymmetry of the thresholds in which the magnitudes of λ_i are, respectively, equal or not *necessarily* equal. Thus, conventional NLC modulation can be re-established simply by setting all symmetrical thresholds to 1.

$$\forall i \in \{1, 2, \ldots, (n-1)/2\}\ \exists \boldsymbol{\lambda} \in \mathbb{R}_+^{(n-1)/2} : \quad 0 \le \theta_1 \le \theta_2, \ldots, \theta_i = \arcsin\left(\frac{2\lambda_i(i-0.5)}{n-1}\right) \le \frac{\pi}{2} \tag{8}$$

The generalized form of the modulation index $m_a(r, \boldsymbol{\lambda})$ is given is being as:

$$m_a(r, \boldsymbol{\lambda}) \triangleq \frac{\hat{v}_{\phi,1}}{\max(\hat{v}_{\phi,1})} = \frac{\pi \hat{v}_{\phi,1}(r, \boldsymbol{\lambda})}{2(n+2r-5)V_1} \tag{9}$$

where $\hat{v}_{\phi,1}(r, \boldsymbol{\lambda})$ and $\max(\hat{v}_{\phi,1})$ represent, respectively, the amplitude of the fundamental component of $v_\phi(\omega t)$ and its maximum by which all θ_i are zeroed out.

3.2. Constrained optimization problem for grid-tied applications

Power quality grid codes usually specify an upper limit L_h for each specific harmonic h and indicate the maximum accepted distortion which, conventionally, considers all harmonics up to the 40th. For instance, the signal quality requirements of both the European and the International grid codes, namely EN 50160 and IEC 61000-2-12, are tabulated in Table 2, where the limited voltage THD is set to 8%. It is worth noting that the maximum harmonic orders required by EN 50160 and IEC 61000-2-12 are 25th and 50th, respectively [23], [24].

Table 2. Individual harmonic limits according to codes EN 50160 and IEC 61000-2-12 in MV networks

EN 50160 ($h \le 25$)						IEC 61000-2-12 ($h \le 50$)					
Odd Harmonics (*Non-multiple of 3*)		Odd Harmonics (*Multiple of 3*)		Even Harmonics		Odd Harmonics (*Non-multiple of 3*)		Odd Harmonics (*Multiple of 3*)		Even Harmonics	
h	L_h (%)	h	L_h (%)	h	L_h (%)	h	L_h (%)	h	L_h (%)	h	L_h (%)
5	6	3	5	2	2	5	6	3	5	2	2
7	5	9	1.5	4	1	7	5	9	1.5	4	1
11	3.5	15	0.5	≥ 6	0.5	11	3.5	15	0.4	6	0.5
13	3	21	0.5			13	3	21	0.3	8	0.5
17	2					17	2	≥ 27	0.2	10	0.5
≥ 19	1.5					≥ 19	$38.59/h - 0.27$			≥ 12	$2.5/h + 0.25$

To seek the appropriate voltage ratio r and all the thresholds λ_i (*i.e.*, the switching angles θ_i) that would have compliance with the aforementioned quality grid regulations, a constrained optimization problem whose cost function $\mathrm{CF}(r, \boldsymbol{\lambda})$ is formulated is being as:

$$\mathrm{CF}(r, \boldsymbol{\lambda}) \equiv \mathrm{CF}(r, \lambda_1, \lambda_2, \lambda_3, \ldots, \lambda_{(n-1)/2}) = \min_{r, \boldsymbol{\lambda}} \mathrm{THD}_{40}\big[v_\ell(\omega t)\big]$$

$$s.t. \quad \begin{cases} \varepsilon_f & \ge & \left|\hat{v}_{\ell,1}(r, \boldsymbol{\lambda}) - \dfrac{2\sqrt{3}V_1}{\pi}(n+2r-5)\, m_a(r, \boldsymbol{\lambda})\right| \\ (1-\delta)L_h & \ge & \dfrac{4\sqrt{3}V_1}{h\pi \hat{v}_{\ell,1}(r, \boldsymbol{\lambda})}\big[\cos h\theta_1 + (r-1)\cos h\theta_2 + \cos h\theta_3 + \cdots + \cos h\theta_{(n-1)/2}\big] \\ 8\% & \ge & \mathrm{THD}_{40}\big[v_\ell(\omega t)\big] = \sqrt{\displaystyle\sum_{h=5,7,\ldots}^{37} \frac{\hat{v}_{\ell,h}^2(r, \boldsymbol{\lambda})}{\hat{v}_{\ell,1}^2(r, \boldsymbol{\lambda})}} \end{cases} \tag{10}$$

where δ is a safety margin; v_ℓ and $v_{\ell,h}$ are, respectively, the line-to-line output voltage and its specific non-triplen odd harmonics under three-phase balanced condition. They are interrelated and can be written as shown in:

$$v_\ell(\omega t) = \sqrt{3}\sum_{h=1}^{\infty} b_h \cos(h\omega t + \varphi_h) = \sum_{h=1}^{\infty} v_{\ell,h}(r, \boldsymbol{\lambda}) \qquad (h : \text{non-triplen odd harmonics}) \tag{11}$$

3.3. Assessment and implementation of the proposed modulation technique

MLIs with higher number of levels are more likely to meet grid quality requirements. However, they significantly suffer from low power efficiency, bulky footprint, high cost and complex design and control. For instance, the proposed inverter structure with 21 levels may be employed, but instead it would be more advisable to use that with 7 levels tuned by a small passive filter since the number of power switches $N_{sw}(n)$, DC sources $k(n)$ and $\mathrm{TSV}(n)$ are reduced by factors of 1.75, 2, and 2.75, respectively. Figure 3 depicts the integration of the proposed 7-level power inverter into the medium-voltage (MV) power distribution system.

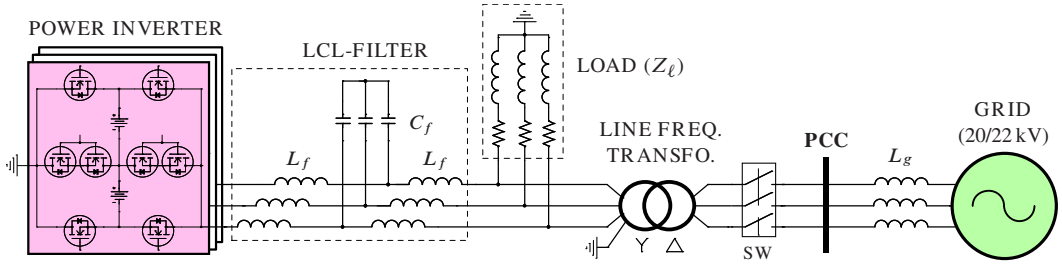

Figure 3. Integration of the proposed 7-level power inverter into medium-voltage power distribution networks

Henceforth, all the above generalized equations are called to deal with only one symmetrical threshold under λ-NLC$_S$ modulation or with three asymmetrical thresholds under λ-NLC$_A$. The domain of each of these thresholds depend upon the definition given by (8), where in the first case $\lambda \in [0, 1.2]$ and in the second case $\lambda_1 \in [0, 6]$, $\lambda_2 \in [0, 2]$ and $\lambda_3 \in [0, 1.2]$ such that $\lambda_1 \leq 3\lambda_2 \leq 5\lambda_3$. The major hindrance of solving the constrained optimization problem arises from the challenge of exploring a wide search space in order to locate feasible solutions $\{\lambda_i^*, r^*\}$ that give best harmonic profiles of the output voltage. So, with the intention to enhance the solutions quality and speed up the processing time of the used evolutionary algorithm, only potential feasible solutions with $\mathrm{THD}_{40} \leq 8\%$ are kept and then plotted in Figures 4 (a) and (b) for both λ-NLC$_S$ and λ-NLC$_A$ modulation strategies, respectively. Moreover, it can be seen in Figure 4 (c) that MLIs driven by conventional NLC ($\lambda = 1$) are out of the allowed range and those with binary configuration ($r = 2$) exhibit the lowest THD. The last result has already been demonstrated in [25].

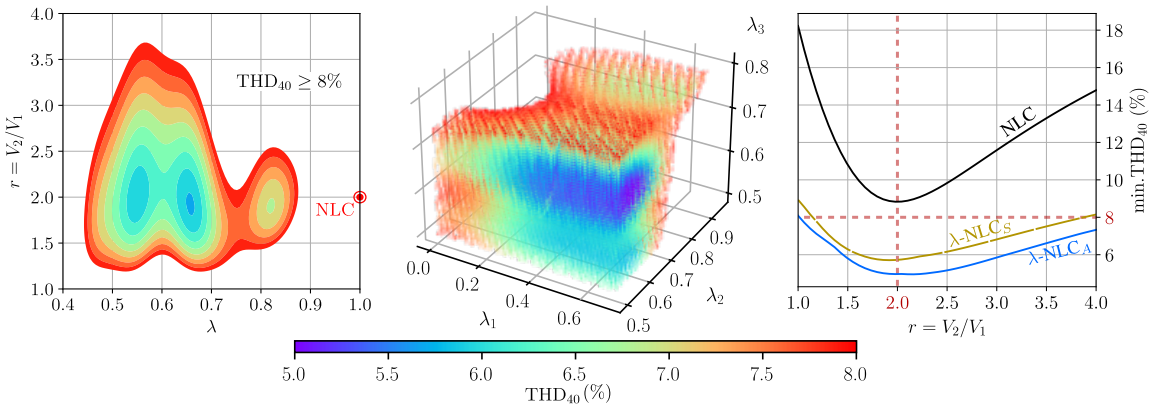

Figure 4. Potential feasible solutions to the constrained optimization problem under: (a) λ-NLC$_S$ and (b) λ-NLC$_A$ (with $r = 2$) modulations. (c) Best harmonic performance with respect to voltage ratio r

In consequence, the binary configuration is chosen which additionally narrow down the search space. The best possible solutions $\{\lambda_i^*\}$ to the non-linear constrained optimization problem of (11) are determined using an implementation of PSO in Python. The validation is done by the algorithm of Figure 5 under SIMULINK. Figure 6 plots the modulating signals, phase- and line-output voltages under conventional, symmetrical and asymmetrical NLC modulations, whereas Figure 7 indicates, side-by-side, the harmonic contents of the respective line-output voltages along with the limits imposed by European and International Grid Codes. Noticeable enhancements in terms of harmonic distortion are directly obtained by the proposed λ-NLC$_S$ and λ-NLC$_A$ modulations, particularly the THD reductions are of about 34% and 43% with respect to the conventional NLC when targeting full EN 50160 compliance with 10% of safety margin, and about 30% and 41% when targeting IEC 61000-2-12 Grid Code. It is worth to mention that all the lower order harmonics are canceled out whereas few of those with higher order can be mitigated by introducing small low-pass filters. These results are summarized within Table 3 in which best feasible solutions are recorded.

IN : Mod. signal $\mathrm{SIG}(t) = (1+r)V_1 \sin(\omega t + \varphi)$
OUT : Gating signals for power switches $S_{i,j}$

if $\mathrm{SIG}(t) \leq \lambda_1 V_1$ *and* $\mathrm{SIG}(t) \geq -\lambda_1 V_1$ **then**
  $\lambda \leftarrow \lambda_1$ **return**
else
  if $\mathrm{SIG}(t) > 2\lambda_2 V_1$ *or* $\mathrm{SIG}(t) < -2\lambda_2 V_1$ **then**
    $\lambda \leftarrow \lambda_3$ **return**
  else
    $\lambda \leftarrow \lambda_2$ **return**

switch $\mathrm{ROUND}(\mathrm{SIG}(t)/(\lambda V_1))$ **do**
  case *equals to* 1
    $S_{i,j} \leftarrow$ switch state #+1 (*cf.* Table 1); **break**
  case *equals to* 2
    $S_{i,j} \leftarrow$ switch state #+2 (*cf.* Table 1); **break**
  ⋮
  otherwise
    if $\mathrm{ROUND}(\mathrm{SIG}(t)/(\lambda V_1)) > +3$ **then**
      $S_{i,j} \leftarrow$ switch state #+3 (*cf.* Table 1)
    if $\mathrm{ROUND}(\mathrm{SIG}(t)/(\lambda V_1)) < -3$ **then**
      $S_{i,j} \leftarrow$ switch state #−3 (*cf.* Table 1)

Figure 5. NLC-based algorithm for the implementation of the proposed 7-level modulation schemes

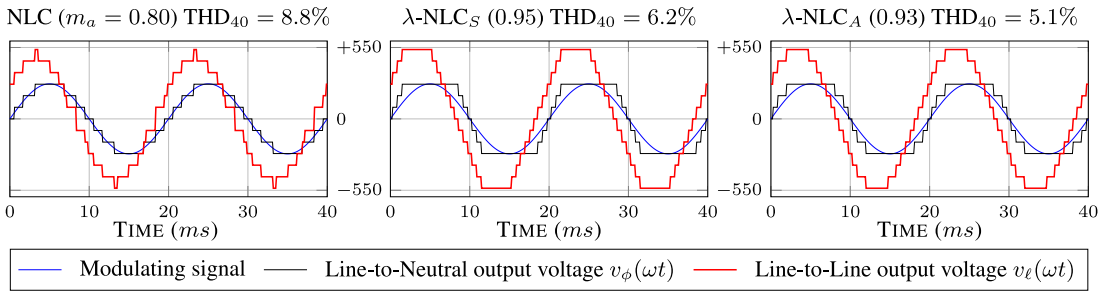

Figure 6. Modulating signals, phase-and line-output voltages using NLC, λ-NLC$_S$ and λ-NLC$_A$ modulations

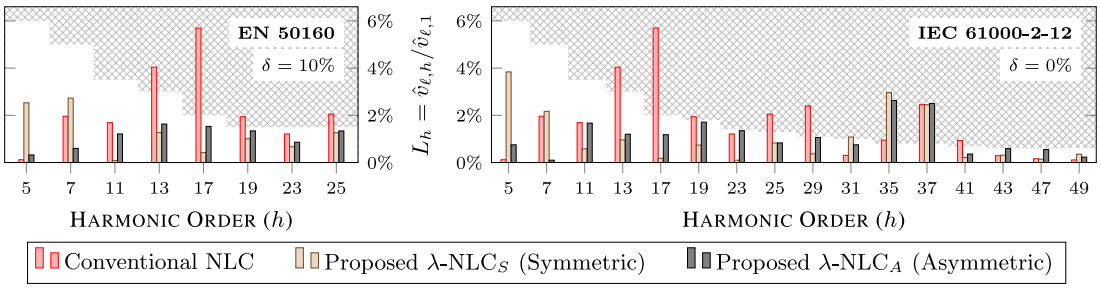

Figure 7. Harmonic contents of the line-output voltages using NLC, λ-NLC$_S$ and λ-NLC$_A$ modulations

Table 3. Salient results of the proposed modulation schemes under some best feasible solutions

MODULATION SCHEME	THRESHOLDS λ_1^*	λ_2^*	λ_3^*	THD (%)	GRID CODE COMPLIANCE EN 50160	IEC 61000-2-12	NOTES (*Remaining harmonics*)
Conv. NLC	1.00	1.00	1.00	8.81	No	No	13th–19th, 25th, 29th, 35th–41st
λ-NLC$_S$	0.55	0.55	0.55	5.83	Yes†	N/A	†Safety margin $\delta = 10\%$
	0.52	0.52	0.52	6.17	Yes	No	31st, 35th and 37th
λ-NLC$_A$	0.61	0.56	0.68	5.01	Yes†	N/A	†Safety margin $\delta = 10\%$
	0.52	0.55	0.68	5.15	Yes	No	35th and 37th

4. CONCLUSION

In this article, a generalized three-phase cascaded multilevel inverter topology with reduced power switching devices was presented. The asymmetric nature of its odd/even DC power sources featuring a septenary relationship in voltage magnitude allows to synthesize high-resolution output waveforms. Subsequently, comparison to some of the cutting-edge MDCS-CMLIs were carried out. It has shown that the proposed structure accomplishes the lowest cost-per-level within all levels regardless the value of the weight coefficient β. Moreover, a new NLC-based modulation strategy was suggested with a twofold aim: firstly, to comply with two European and International power quality grid codes, respectively, EN 50160 and IEC 61000-2-12; and secondly, to provide an alternative pathway to overcome the intrinsic drawbacks inherited from SHE/SHM techniques. The obtained results within SIMULINK FFT analysis tool clearly demonstrated the outperformance of the proposed modulation with (a) symmetrical thresholds λ_i over the conventional NLC, in which the optimal feasible solutions λ_i^* to the constrained optimization problem was determined by a bio-inspired algorithm (*e.g.*, PSO) described in python programming language.

REFERENCES

[1] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel Inverter Topologies With Reduced Device Count: A Review," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135-151, Jan. 2016, doi: 10.1109/TPEL.2015.2405012.

[2] K. P. Panda, S. S. Lee, and G. Panda, "Reduced Switch Cascaded Multilevel Inverter With New Selective Harmonic Elimination Control for Standalone Renewable Energy System," in *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7561-7574, Nov.-Dec. 2019, doi: 10.1109/TIA.2019.2904923.

[3] C. Dhanamjayulu, D. Prasad, S. Padmanaban, P. K. Maroti, J. B. Holm-Nielsen and F. Blaabjerg, "Design and Implementation of Seventeen Level Inverter With Reduced Components," in *IEEE Access*, vol. 9, pp. 16746-16760, 2021, doi: 10.1109/ACCESS.2021.3054001.

[4] A. Chappa, S. Gupta, L. K. Sahu, S. P. Gautam and K. K. Gupta, "Symmetrical and Asymmetrical Reduced Device Multilevel Inverter Topology," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 885-896, Feb. 2021, doi: 10.1109/JESTPE.2019.2955279.

[5] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 1248-1282, September 2017, doi: 10.1016/j.rser.2017.03.121.

[6] M. D. Siddique, *et al.*, "Low Switching Frequency Based Asymmetrical Multilevel Inverter Topology With Reduced Switch Count," in *IEEE Access*, vol. 7, pp. 86374-86383, 2019, doi: 10.1109/ACCESS.2019.2925277.

[7] S. Ahmad, M. Meraj, A. Iqbal, and I. Ashraf, "Selective harmonics elimination in multilevel inverter by a derivative-free iterative method under varying voltage condition," *ISA Transactions*, vol. 92, pp. 241-256, September 2019, doi: 10.1016/j.isatra.2019.02.015.

[8] L. G. Franquelo, J. Nápoles, R. C. P. Guisado, J. I. León, and M. A. Aguirre, "A Flexible Selective Harmonic Mitigation Technique to Meet Grid Codes in Three-Level PWM Converters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3022-3029, Dec. 2007, doi: 10.1109/TIE.2007.907045.

[9] J. Nápoles, J. I. León, R. C. Portillo, L. G. Franquelo, and M. A. Aguirre, "Selective Harmonic Mitigation Technique for High-Power Converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2315-2323, July 2010, doi: 10.1109/TIE.2009.2026759.

[10] A. Moeini, H. Iman-Eini, and M. Najjar, "Non-equal DC link Voltages in a Cascaded H-Bridge with a Selective Harmonic Mitigation-PWM Technique Based on the Fundamental Switching Frequency," *Journal of Power Electronics*, vol. 17, no. 1, pp. 106-114, January 2017, doi: 10.6113/JPE.2017.17.1.106.

[11] S. Kundu and S. Banerjee, "An improved SHM-PWM scheme for three-phase seven-level CHB inverter to improve power quality by fulfilling CIGRE WG 36-05 and EN 50160 and sharing equal power between the H-bridge cells," *Int. Trans. . Elec. Energy Sys.*, vol. 29, no. 9, p. e12040, May 2019, doi: 10.1002/2050-7038.12040.

[12] Y. Jin *et al.*, "A Novel Harmonic Control Method for MMC Combining Improved Nearest Level Control and Selective Harmonic Elimination Method," *IEEE Energy Conversion Congress and Exposition (ECCE)*, September 2019, pp. 6368-6375, doi: 10.1109/ECCE.2019.8912529.

[13] A. Janabi and B. Wang, "Real-time Implementation of Selective Harmonic Elimination with Seamless Dynamic Performance," *IEEE Energy Conversion Congress and Exposition (ECCE)*, September 2018, pp. 3362-3366, doi: 10.1109/ECCE.2018.8557466.

[14] M. Ahmed *et al.*, "Selective harmonic elimination method for unequal DC sources of multilevel inverters," *Journal for Control, Measurement, Electronics, Computing and Communications*, vol. 60, no. 4, pp. 378-384, July 2019, doi: 10.1080/00051144.2019.1621048.

[15] M. A. Memon, S. Mekhilef, M. Mubin, and M. Aamir, "Selective harmonic elimination in inverters using bio-inspired intelligent algorithms for renewable energy conversion applications: A review," *Renewable and Sustainable Energy Reviews*, vol. 82, pp. 2235-2253, February 2018, doi: 10.1016/j.rser.2017.08.068.

[16] M. Setti and M. Cherkaoui, "Design and implementation of an optimized multilevel power inverter structure based on C MEX and PSPICE," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 11, no. 3, pp. 1388-1397, September 2020, doi: 10.11591/ijpeds.v11.i3.pp1388-1397.

[17] R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, M. Kojabadi, and F. Blaabjerg, "A New Boost Switched-Capacitor Multilevel Converter with Reduced Circuit Devices," in *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6738-6754, August 2018, doi: 10.1109/TPEL.2017.2751419.

[18] S. Sabyasachi, V. B. Borghate, and S. K. Maddugari, "A 21-Level Bipolar Single-Phase Modular Multilevel Inverter," *Journal of Circuits, Systems and Computers*, vol. 29, no. 1, p. 2050004, 2020, doi: 10.1142/S0218126620500048.

[19] P. Prem *et al.*, "A novel cross-connected multilevel inverter topology for higher number of voltage levels with reduced switch count," *International Transactions on Electrical Energy Systems*, vol. 30, no. 6, pp. 1-18, June 2020, doi: 10.1002/2050-7038.12381.

[20] A. N. Babadi, O. Salari, M. J. Mojibian, and M. T. Bina, "Modified Multilevel Inverters with Reduced Structures Based on Packed U-Cell," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 874-887, June 2018, doi: 10.1109/JESTPE.2017.2767499.

[21] M. D. Siddique, S. Mekhilef, M. Rawa, A. Wahyudie, B. Chokaev, and I. Salamov, "Extended Multilevel Inverter Topology With Reduced Switch Count and Voltage Stress," in *IEEE Access*, vol. 8, pp. 201835-201846, 2020, doi: 10.1109/ACCESS.2020.3026616.

[22] M. D. Siddique, A. Iqbal, M. A. Memon and S. Mekhilef, "A New Configurable Topology for Multilevel Inverter With Reduced Switching Components," *IEEE Access*, vol. 8, pp. 188726-188741, 2020, doi: 10.1109/ACCESS.2020.3030951.

[23] CENELEC EN 50160, "Voltage characteristics of electricity supplied by public electricity networks," *Orgalim, Europe's Technology Industries*, February 2011.

[24] IEC 61000, "Environment - Compatibility levels for low-frequency conducted disturbances and signalling in public medium-voltage power supply systems," *IEC Standard IEC*, April 2003.

[25] M. Setti, M. Ouassaid, and M. Cherkaoui, "New power efficient seven-level inverter topology controlled by flexible nearest level modulation," *2017 International Conference on Electrical and Information Technologies (ICEIT)*, 2017, pp. 1-6, doi: 10.1109/EITech.2017.8255249.