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A Comparative Studies of Cascaded Multilevel Inverters Having Reduced Number of Switches with R and RL-Load

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ABSTRACT

Multilevel inverter offers many benefits for high power application compavered to conventional cascaded Multilevel Inverter topology.This paper presents Symmetric CMLI using variable frequency carrier based pulse width modulation techniques. The proposed topology reduces total harmonic distortion and reduced switching losses for seven level inverter. The simulation study of the proposed topology has been carried out in MATLAB/SIMULINK. The main objective of this paper is to achieve number of levels of MLI with reduced number of switches and DC power sources compared to conventional topology.

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1. INTRODUCTION

In a multilevel inverter a desired output voltage has been synthesized to several levels from a number of DC sources as inputs. The most attractive applications of multilevel power conversion technology are in the medium to high voltage ranges [1]. A multilevel inverter not only achieves high power ratings but also enables the use of renewable energy sources. Renewable energy soures i.e solar photovoltaic, wind, fuel cells etc. can be easily interfaced to multilevel converter for high power applications [2].

Three different topologies have been proposed for multilevel inverters i.e cascaded MLI, Diode-clamped MLI and capacitor clamped. Each of the topology has a different mechanism to provide voltage levels [3]. These topologies are widely referred to as the 'classical topologies' [4]. One major disadvantage of multilevel power conversion is that great number of power semiconductor switches needed. Another disadvantage of multilevel power converters is that the voltage steps are produced by isolated DC voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available and series capacitors require voltage balance [5].

There are two PWM methods mainly used in multilevel inverter control strategy. One is fundamental switching frequency and another is high switching frequency.for high switching frequency classified as space vector PWM, Selective Harmonic Elemination PWM and SPWM. Among these PWM methods SPWM is the most preferable as it is simple and easy to implement [6]-[7]. In this paper SPWM method with different carrier based disposition as PDPWM and APODPWM have been analyzed.

2. EXISTING TOPOLOGIES

Conventional cascaded seven level multilevel inverter require twelve switches and 3 dc sources separately [4]. To overcome the drawbacks of it next topologies are made with seven level nine switches 3 dc sources, seven level seven switches and 3 dc sources etc [7]. The proposed topologies are designed for seven level, 6 switches with 4 dc and 3 dc sources respectively with bidirectional switches where the harmonics are reduced.

2.1. Proposed Topology-I

The proposed topology is designed with six switches without H-bridge and four dc sources as shown in Figure 1. The proposed topology is simple in design compared to the existing topologies. Switches S6 and S7 are used for generating the pulses in positive and negative sequence and switch S1 is connected to the load. It is used only when all the switches are open to produce zero voltage level. Switch S2, S3, and S4 are used to generate the levels Vdc, 2Vdc, 3Vdc in both positive and negative levels.

The generalized expression for the number of switches and the number of Dc sources are

S=(N+5)/2 and V=(N+1)/2

Where N=Number of levels, S= No. of switches and V=No. of DC sources.

Both the carrier based PWM techniques i.e IPD PWM and APOD PWM methods are analyzed with resistive and RL-type load.

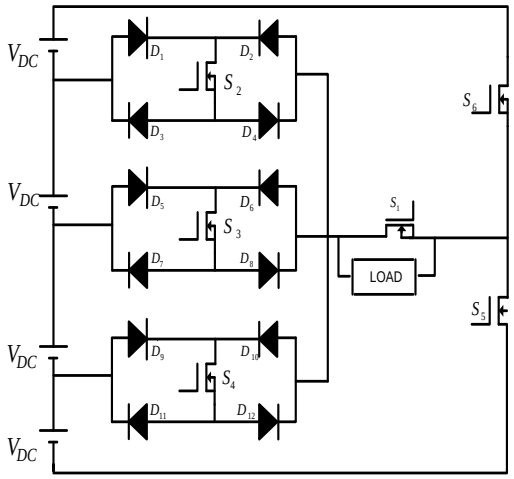


Figure 1. Configuration of seven level six switches with 4 DC sources proposed Topology

Table 1. Switching pattern for seven level six switches 4 Dc sources

SL.No	S1	S2	S3	S4	S5	S6	D1D4	D2D3	D5D8	D6D7	D9D12	Output Voltage
1	Off	Off	Off	On	On	Off	Off	Off	Off	Off	On	V_{dc}
2	Off	Off	On	Off	On	Off	Off	Off	On	Off	Off	$2V_{dc}$
3	Off	On	Off	Off	On	Off	On	Off	Off	Off	Off	$3V_{dc}$
4	On	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	0
5	Off	On	Off	Off	Off	On	Off	On	Off	Off	Off	$-V_{dc}$
6	Off	Off	On	Off	Off	On	Off	Off	Off	On	Off	$-2V_{dc}$
7	Off	Off	Off	On	Off	On	Off	Off	Off	Off	Off	$-3V_{dc}$

2.2. Proposed Topology-II

It is simple in design and compared to other existing topologies. It consists of three DC sources and six switches.the generalized expression for the number of switches ad number of Dc sources for the topology is given by

S=(N+5)/2 and V==(N-1)/2.

Both the carrier based PWM techniques i.e IPD and APOD PWM methods are analyzed with resistive load type.

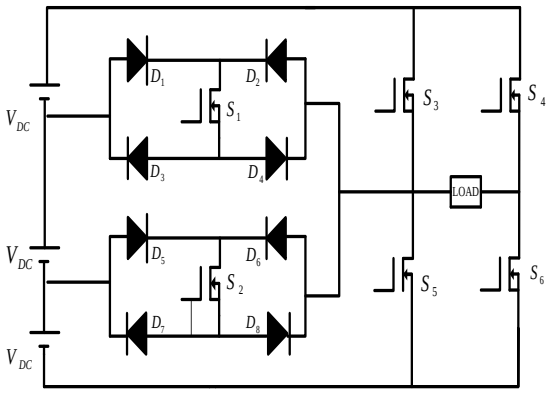


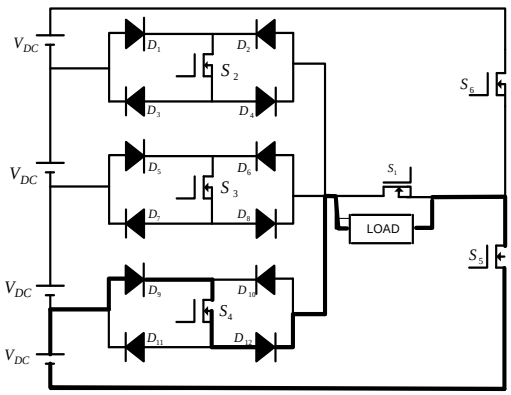
Figure 2. Configuration of seven level six switches with 3 DC sources proposed Topology

Table 2. Configuration of 7 level 6 switches and 3Dc sources

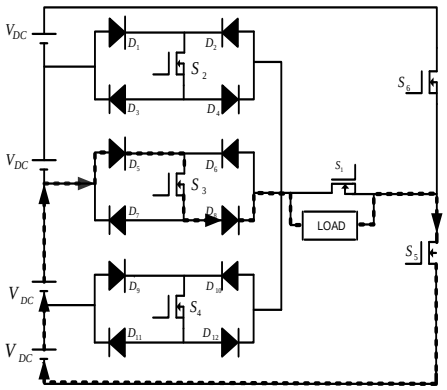
SL.No	S1	S2	S3	S4	S5	S6	D1D4	D2D3	D5D8	D6D7	Output Voltage
1	Off	On	Off	Off	Off	On	Off	Off	On	Off	V_{dc}
2	On	Off	Off	Off	Off	On	On	Off	Off	Off	$2V_{dc}$
3	Off	Off	On	Off	Off	On	Off	Off	Off	Off	$3V_{dc}$
4	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	0
5	On	Off	Off	On	Off	Off	Off	On	Off	Off	$-V_{dc}$
6	Off	On	Off	On	Off	Off	Off	Off	Off	On	$-2V_{dc}$
7	Off	Off	Off	On	On	Off	Off	Off	Off	Off	$-3V_{dc}$

3. MODES OF OPERATION

3.1. Topology -1



Mode 1



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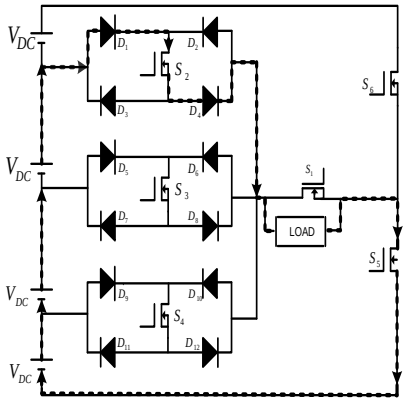

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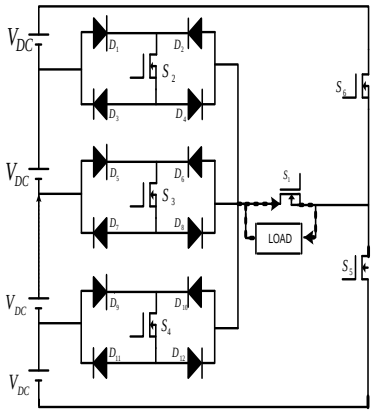

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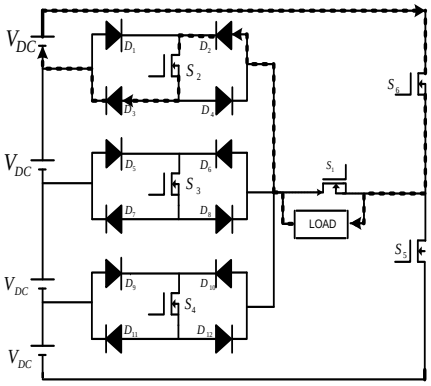

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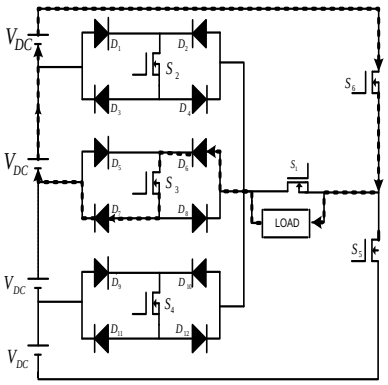
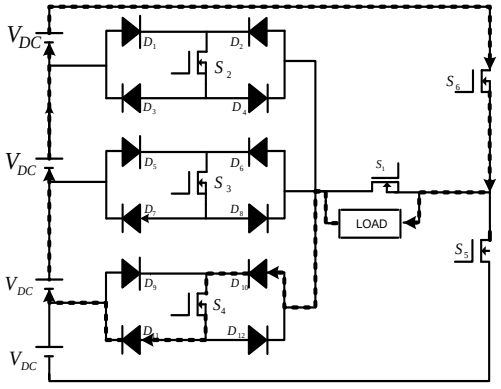


Mode 6



Mode 7

Figure 3. Different modes of operation of 7 levels, 6 switches and 4 DC sources CMLI

3.2. Topology –II

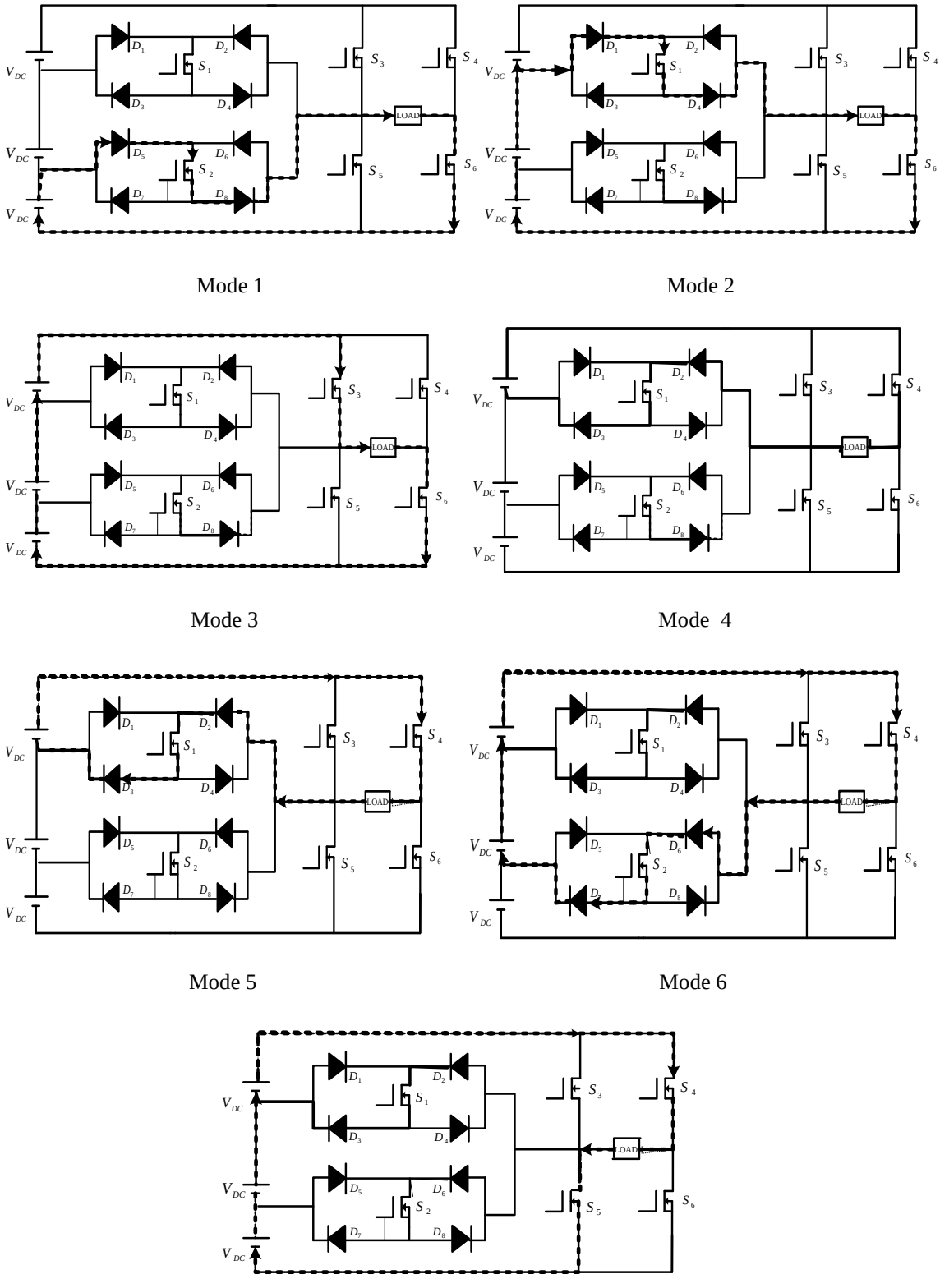


Figure 4. Different modes of operation of 7 levels, 6 switches and 3 Dc sources CMLI

4. PWM TECHNIQUES

The carrier based modulation techniques for multilevel inverters can be generally classified into two categories: phase shifted and level shifted modulations. Both modulation schemes can be applied to the cascaded multilevel inverter [8]-[9]. Total harmonic distortion of phase shifted modulation is much higher than level shifted modulation. Hence level shifted modulation technique is being chosen. In this paper SPWM method with different carrier based disposition as PDPWM and APODPWM have been analyzed.

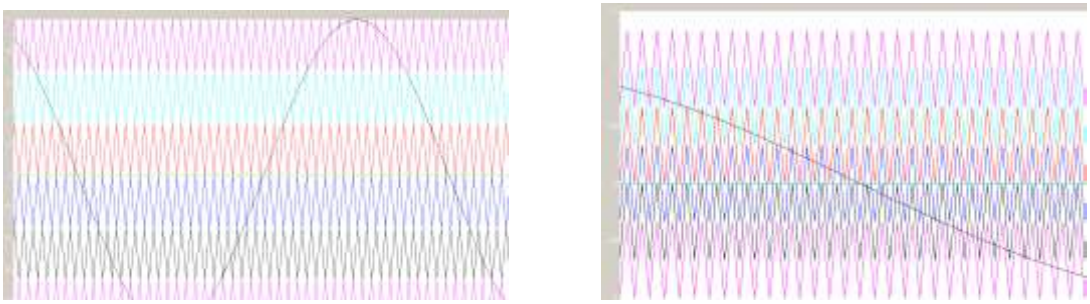


Figure 5. APOD and IPD PWM Switching Schemes

5. SIMULATION RESULTS

5.1. Topology - I

All the switches used in this circuit are MOSFETS. The switches S_2, S_3, S_4 are bidirectional and remaining switches are unidirectional.the loads are resistive and RL-load. The DC sources are 10V.

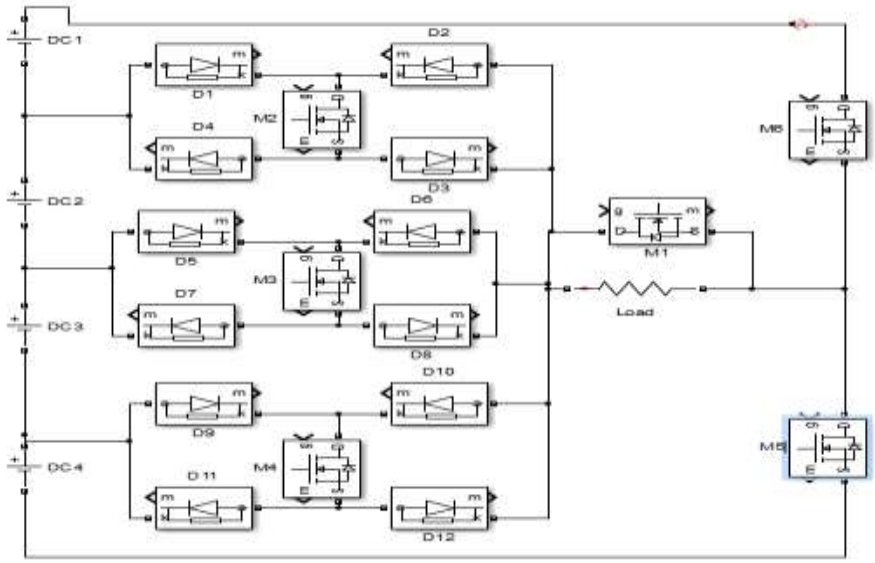


Figure 6. Simulation Diagram of Proposed Topology 1

Sine and triangular carriers are compared and 7 levels are generated. Both the Dc and different levels generated are fed to logic gates to produce gate signals. These gate signals are fed to switches S_1 to S_7 respectively.

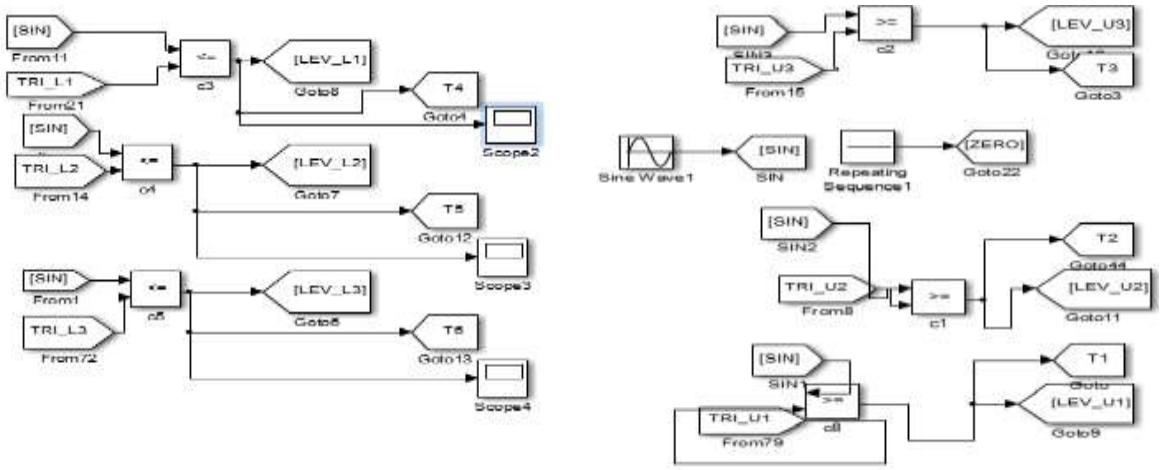


Figure 7. Different levels generation

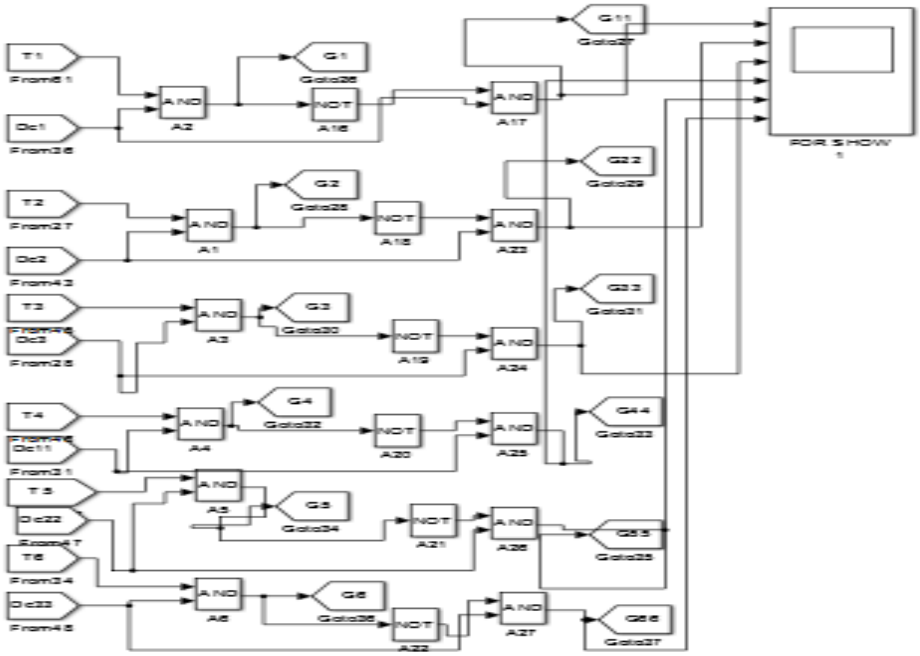


Figure 8. Gate Pulse Generation

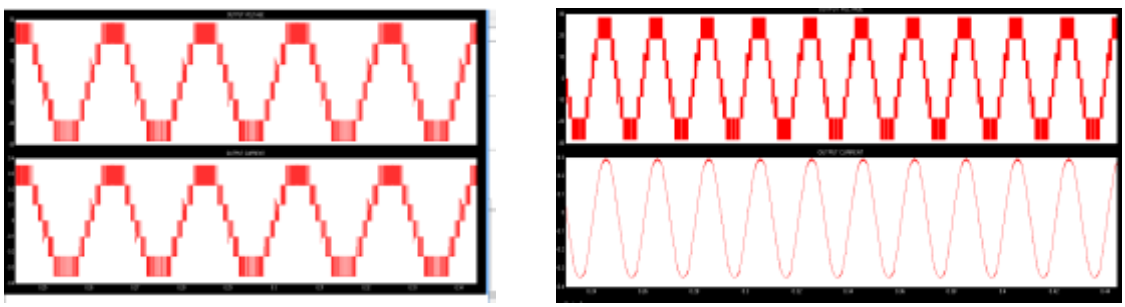
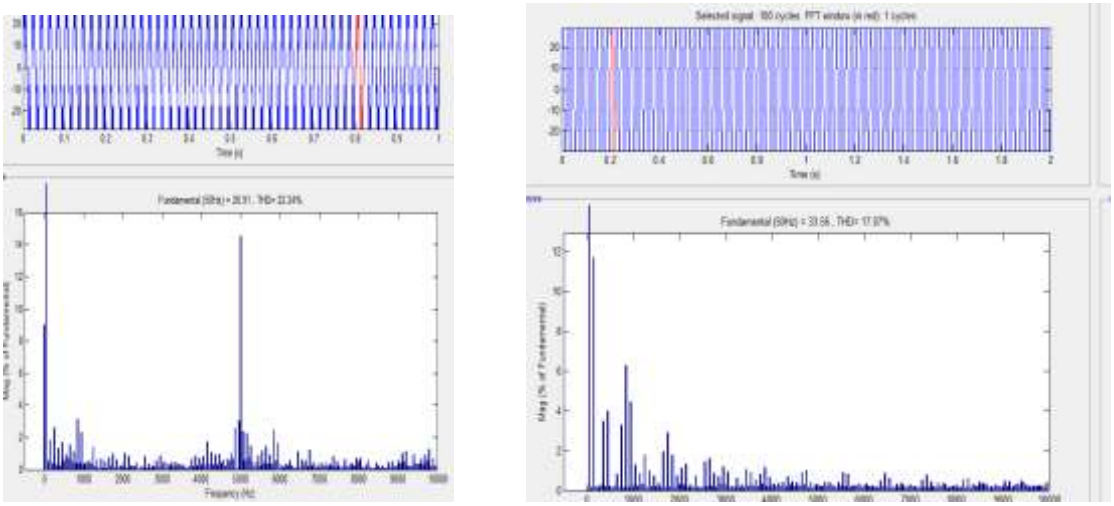


Figure 9(a). Output voltage and current with Resistive load (b) with RL -Load



(a) (b)

Figure 10(a). APOD switching scheme (b) IPD switching scheme

5.2. Topology II

All the switches used in this circuit are unidirectional except switches S1 and S2 of circuit diagram.All the Dc sources are taken as 10 Vdc and Resistance as 80 ohms.

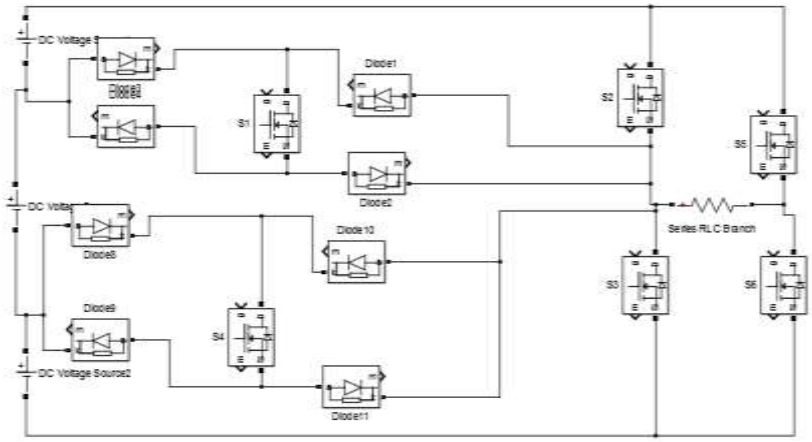


Figure 11. Simulation of 7 levels six switches and 3 Dc sources topology

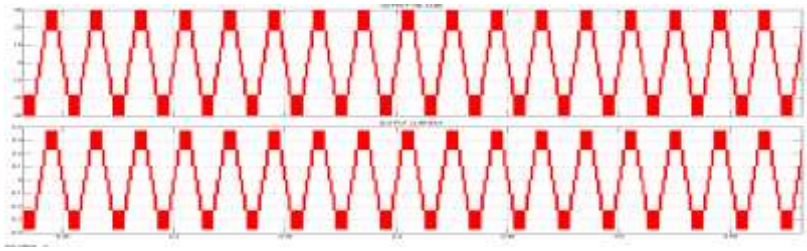


Figure 12. IPD PWM switching scheme, 7 levels, 6 switches, 3 DC sources

Comments: Vout=30V at R=80ohms and carrier frequency=5KHz

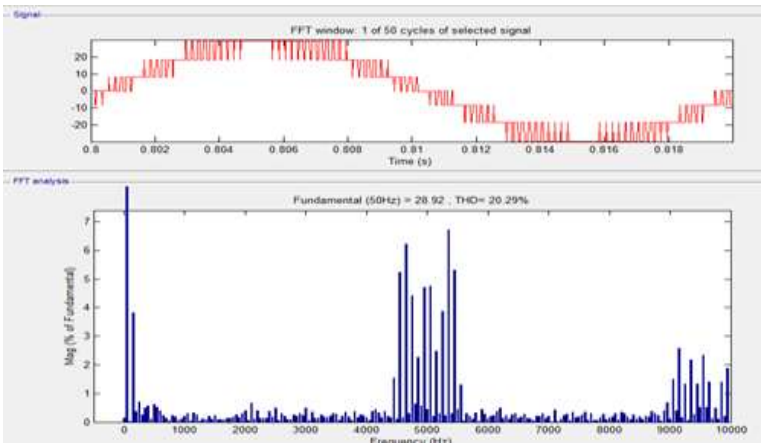


Figure 13. THD Analysis

At R=80 ohms, THD=20%, Fundamental output voltage=28.9V

6. COMPARISON OF TWO TOPOLOGIES

6.1. THD Analysis

Table 3. Comparison of two topologies with APOD and IPD switching schemes

7 levels, 6 switches, 4 DC sources Topology

PWM	MI	THD	Fundamental (Simulated)	Fundamental (Calculated)
APOD	0.8	23.73	22.46	23.7
	0.9	23.15	24.98	25.6
	1	19	27.8	28.3
IPD	0.8	23.48	22.53	23.4
	0.9	23.11	25.09	25.9
	1	19.08	27.94	29.3

7 levels, 6 switches, 3 DC sources Topology

PWM	MI	THD	Fundamental (Simulated)	Fundamental (Calculated)
APOD	0.8	24.87	22.69	24.2
	0.9	24.72	25.66	26.3
	1	20.29	28.9	30
IPD	0.8	24.82	22.82	24.2
	0.9	24.6	25.73	26.4
	1	19.8	29.01	29.9

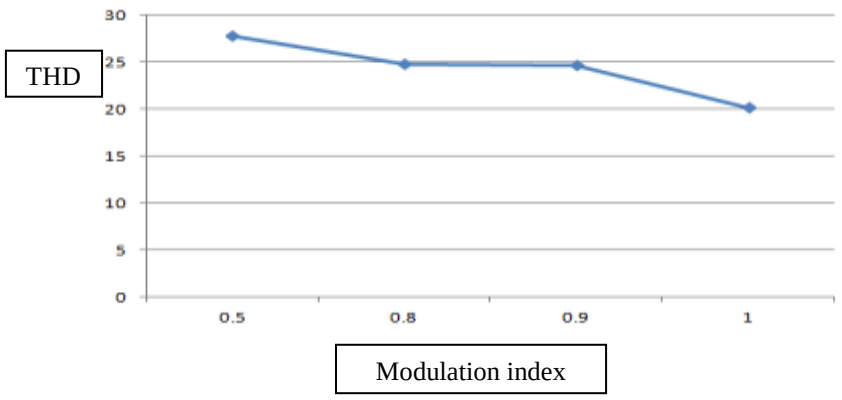


Figure 14. THD Vs Modulation Index of 7 level 6 switches and 4 Dc sources, Comment: With increase of Modulation index THD reduced

6.2. Voltage Stress Across Switches

It has been observed that reduced number of switches give more voltage stress compared to conventional CMLI.

Table 4. Voltage stresses across the switches

Conventional	7 levels 4 DC sources in V						7 levels 3 DC sources in V					
10V (Across all switches)	S_1	S_2	S_3	S_4	S_5	S_6	S_1	S_2	S_3	S_4	S_5	S_6
	28.4	20	10	20	40	40	18.2	18.2	30	30	30	30

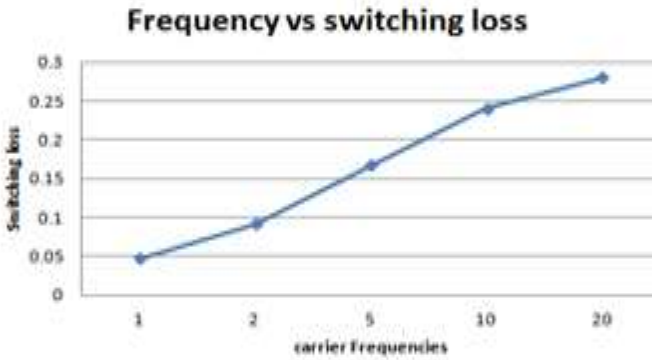


Figure 15. Carrier frequency Vs Switching loss of 7 level 6 switches 4Dc sources

7. LOSS CALCULATION

Each Mosfet loss has been calculated from simulation result. The voltage and current wave forms are observed from simulation diagram of each switch and thus power is being calculated. From power pulse of each switch at different carrier frequencies the switching and conduction losses are calculated. At carrier frequency 1 KHz, different losses are calculated as shown below.

Table 5. Calculation of Switching, Conduction and Total Circuit loss at different Carrier Frequencies

	S1	S2	S3	S4	S5	S6	Total
Swtching loss (in W)	0.035	0.0016	0.0012	0.0023	0.05	0.0489	0.0489
Conduction Loss (in W)	0.0045	0.0042	0.004	0.0042	0.0045	0.0041	0.005
Total Loss (in W)	0.0395	0.0058	0.0052	0.0065	0.0545	0.053	0.0539

Table 6. Loss at different carrier frequencies

Carrier Frequencies (in KHz)	Input Voltage (in Volt)	Input Current (in Amp)	Input Power (in Watt)	Output Voltage (in Volt)	Output Current (in Amp)	Output Power (in Watt)	Circuit Total Loss (in Watt)
1	40	0.354	14.16	28.35	0.351	9.95	4.05
2	40	0.35	14	28.35	0.35	9.92	4.08
5	40	0.351	14.04	28.35	0.3482	9.87	4.13
10	40	0.3458	13.83	28.35	0.354	10.03	3.97
20	40	0.35	14	28.35	0.3475	9.85	4.15

It shows with increase of carrier frequencies switching losses increases.

8. CONCLUSION

Inverter operation of 6 switches and 4 DC sources based topology was carried out and the required objective of low harmonics and 7 level output at THD is19.08% & Fundamental output at 27.9V at MI=1. Inverter operation of 6 switches and 3 DC sources based topology was carried out and the required objective of low harmonics and 7 level output at THD is 19.8% & Fundamental output at 29.01V at MI=1. Switching Loss, Conduction Loss and total circuit loss at different carrier frequencies are carried out successfully. Voltage stress of conventional and modified topologies are compared.

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