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Novel Symmetric and Asymmetric Multilevel Inverter Topology for Permanent Magnet Synchronous Motor

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ABSTRACT

In this paper a new, simple multilevel inverter topology is proposed. Multilevel inverter uses several dc sources and power switches to synthesize desired output voltage waveform. The single phase structure of proposed topology in this paper consists of two dc sources and eight power switches. When the magnitudes of dc sources are equal it operates in symmetric mode, however in order to increase output voltage levels unequal magnitudes of dc sources are selected, then it operates in asymmetric mode. So far, multilevel inverter topologies have been used in motor drive industry to run induction motors. Recently permanent magnet synchronous motors (PMSM) are replacing induction motors. Multilevel inverter is an attracting choice for driving high performance PMSM. However very few studies discuss the performance of multilevel inverter fed PMSM. In this paper simulation of novel symmetric and asymmetric multilevel inverter is carried out to analyze performance of PMSM. The topology is investigated through computer simulation using MATLAB/Simulink.

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1. INTRODUCTION

The basic idea of multilevel inverter is to attain higher power by using number of power switches with several low voltage dc sources [1]. It provides a desired output voltage waveform in steps closer to sine wave and reduces total harmonic distortion. This concept was patented by MIT researcher over thirty years ago [2],[3]. Advancement in power electronics has made this concept practical. Recently, this technology has become popular in industry for medium and high voltage applications [4]. Multilevel inverters have been widely recommended because of eminent advantages like high quality output voltage using low switching frequency, low harmonic components, low electromagnetic interference, low blocking voltage of power switches, more efficiency and low dv/dt stress on load [5],[6]. Improvement in these advantages is possible by increasing number of levels of output voltage waveform that requires large number of switches and increases circuit complexity. It also raises cost and size of the circuit.

The popular conventional multilevel inverter topologies are neutral point clamped (NPC) suggested by Nabae et al [7], flying capacitor (FC) suggested by Meynard et al [8] and cascaded H bridge (CHB) suggested by Peng et al [9]. NPC is first generation of multilevel technology and also known as diode clamped (DC) multilevel inverter. Researchers' efforts made this topology known as state-of-the art of multilevel technology [10]. The FC topology uses capacitors in ladder form to clamp the voltage. It requires

large number of capacitors. In CHB single phase inverters (H-bridges) with separate dc sources of equal magnitude are connected in series. Each H-bridge produces three voltage levels. Total output is obtained by adding voltages generated by each H-bridge. This topology has become popular because of its modular design, simple control, reliability, availability and the absence of capacitor imbalance problem.

Now a day, research is engaged to develop innovative multilevel inverter topologies to overcome disadvantages of conventional topologies, one prominent of them is requirement of large number of power switches [11]. The other objectives are to reduce number of dc sources, complexity of the circuit, total harmonic distortion, power losses, voltage stress on power switches etc. [12]-[16]. Newly developed topologies include asymmetric and/or hybrid inverters [17]-[18]. Unequal dc source values are used in asymmetric topology while hybrid inverters are composed by using variety of topologies, applying different modulation techniques or semiconductor technologies. Application areas of these newly developed topologies include low cost and efficient industrial drives, electrical vehicles, FACTS-flexible ac transmission systems etc. [19]. The rest of the paper is organized as follows: Section 2 presents novel multilevel inverter topology. Detailed working of topology is given in this section. In Section 3 information of PMSM is given in short. Simulation results and comparison among symmetric and asymmetric novel multilevel inverter topology is presented in Section 4. Finally, conclusions are summarized in Section V.

2. NOVEL MULTILEVEL INVERTER TOPOLOGY

Figure 1 shows single phase structure of novel topology. It consists of two dc sources V_X and V_Y and eight power switches, PS_1, PS_2, PS_3, PS_4, PS_5, PS_6, PS_7 and PS_8. This novel topology offers flexibility in generating output voltage levels. When both the voltage sources are of equal magnitude, $V_X = V_Y = E$, then load is supplied with five levels $\pm 2E$, $\pm E$ and zero. This is symmetric configuration of the basic structure. However with asymmetric source configuration the load is supplied with (a) seven levels $\pm 3E$, $\pm 2E$, $\pm E$ and zero for $V_X = 2E$ and $V_Y = E$ (i.e. $V_X = 2V_Y$, binary asymmetric configuration) (b) nine levels $\pm 4E$, $\pm 3E$, $\pm 2E$, $\pm E$ and zero for $V_X = 3E$ and $V_Y = E$ (i.e. $V_X = 3V_Y$, trinary asymmetric configuration) .

All the operating/ redundant modes are summarized in Table 1. The switching sequences for positive, zero and negative levels are as shown in Figure 2. This topology offers redundancy and flexibility in generating output voltage levels. Minimum switching transitions are chosen during different levels. It is seen that, only three switches are conducting in any switching mode. The load is supplied by different voltage levels. According to magnitude of voltage sources selected the same basic structure generates five level, seven level or nine level output voltage as shown in Table 1. Mode 1 generates maximum output voltage (V_X+V_Y). For this mode trinary asymmetric configuration generates V_{AB} = 4E; binary asymmetric configuration generates V_{AB} = 3E and symmetric configuration generates V_{AB} = 2E, as magnitude of output voltage. Zero level output can be produced by two switching modes. In mode 5 switches PS_2, PS_3, PS_6 are on and in mode 5' switches PS_2, PS_4, PS_5 are on while all other switches are in off state. Mode 9 generates negative maximum output voltage (-V_X-V_Y). For this mode trinary asymmetric configuration generates V_{AB} = -4E; binary asymmetric configuration generates V_{AB} = -3E and symmetric configuration generates V_{AB} = -2E, as magnitude of output voltage.

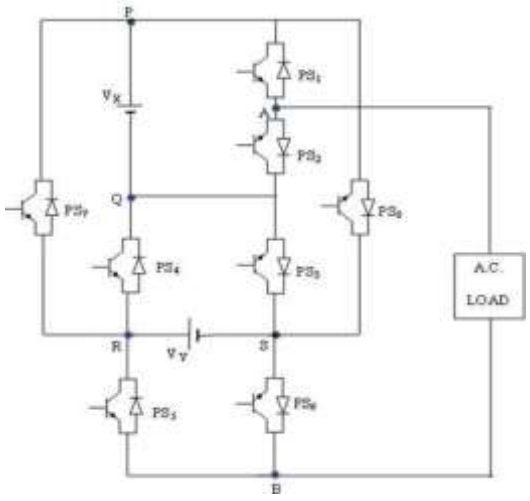
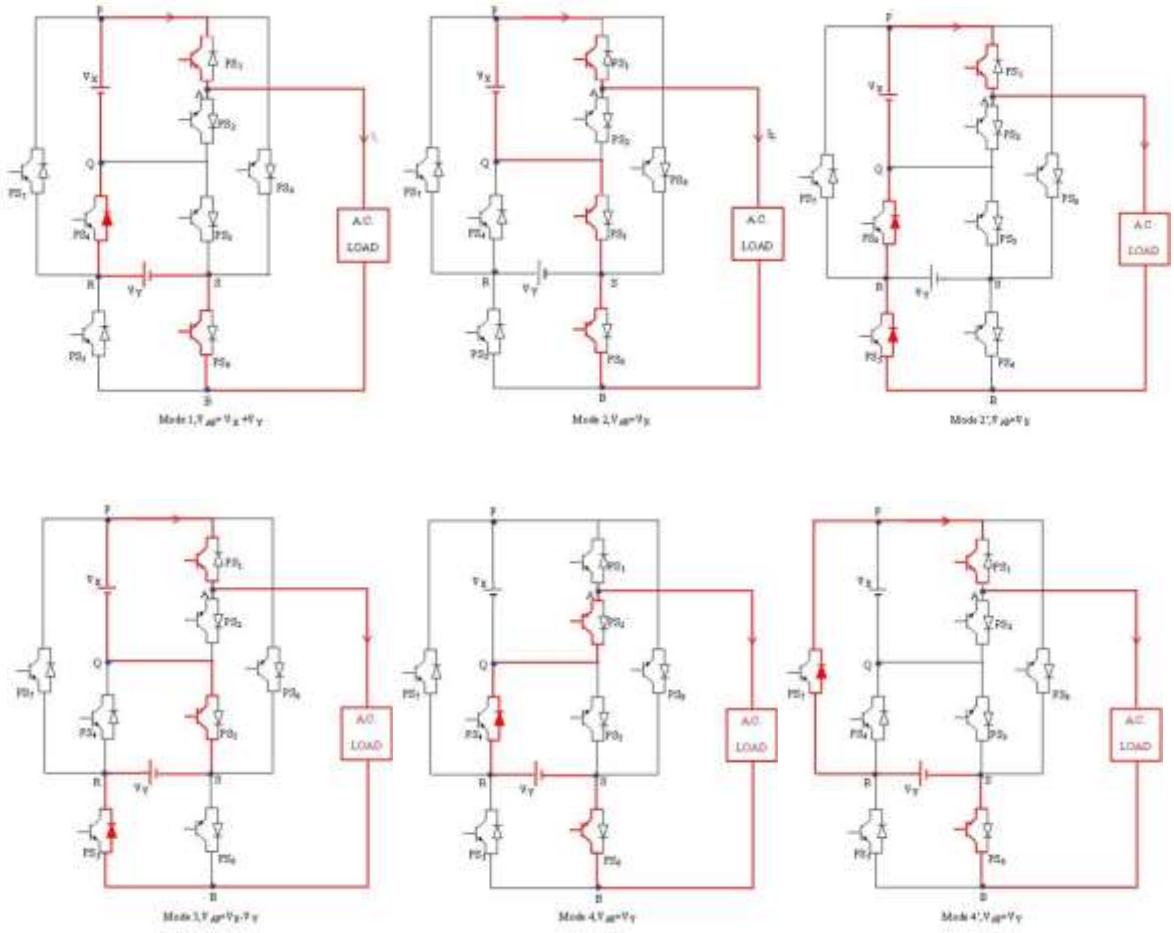


Figure 1. Single phase structure of novel topology

Table 1. Operating modes of proposed multilevel topology

Mode	Switching states (On=1; Off=0)								Output Voltage	Symmetric configuration	Binary asymmetric configuration	Trinary asymmetric configuration
	PS_1	PS_2	PS_3	PS_4	PS_5	PS_6	PS_7	PS_8		V_{AB} for V_X=E, V_Y=E	V_{AB} for V_X=2E, V_Y=E	V_{AB} for V_X=3E, V_Y=E
1	1	0	0	1	0	1	0	0	V_X+V_Y	2E	3E	4E
2	1	0	1	0	0	1	0	0	V_X	E	2E	3E
2’	1	0	0	1	1	0	0	0				
3	1	0	1	0	1	0	0	0	V_X-V_Y	0	E	2E
4	0	1	0	1	0	1	0	0	V_Y	E		E
4’	1	0	0	0	0	1	1	0				
5	0	1	1	0	0	1	0	0	0	0	0	0
5’	0	1	0	1	1	0	0	0				
6	0	1	1	0	1	0	0	0	$-V_Y$	-E	-E	-E
6’	1	0	0	0	1	0	0	1				
7	0	1	0	0	0	1	1	0	$-V_X+V_Y$	0		
8	0	1	0	0	1	0	1	0	$-V_X$	-E	-2E	-3E
8’	0	1	0	0	0	1	0	1				
9	0	1	0	0	1	0	0	1	$-V_X-V_Y$	-2E	-3E	-4E



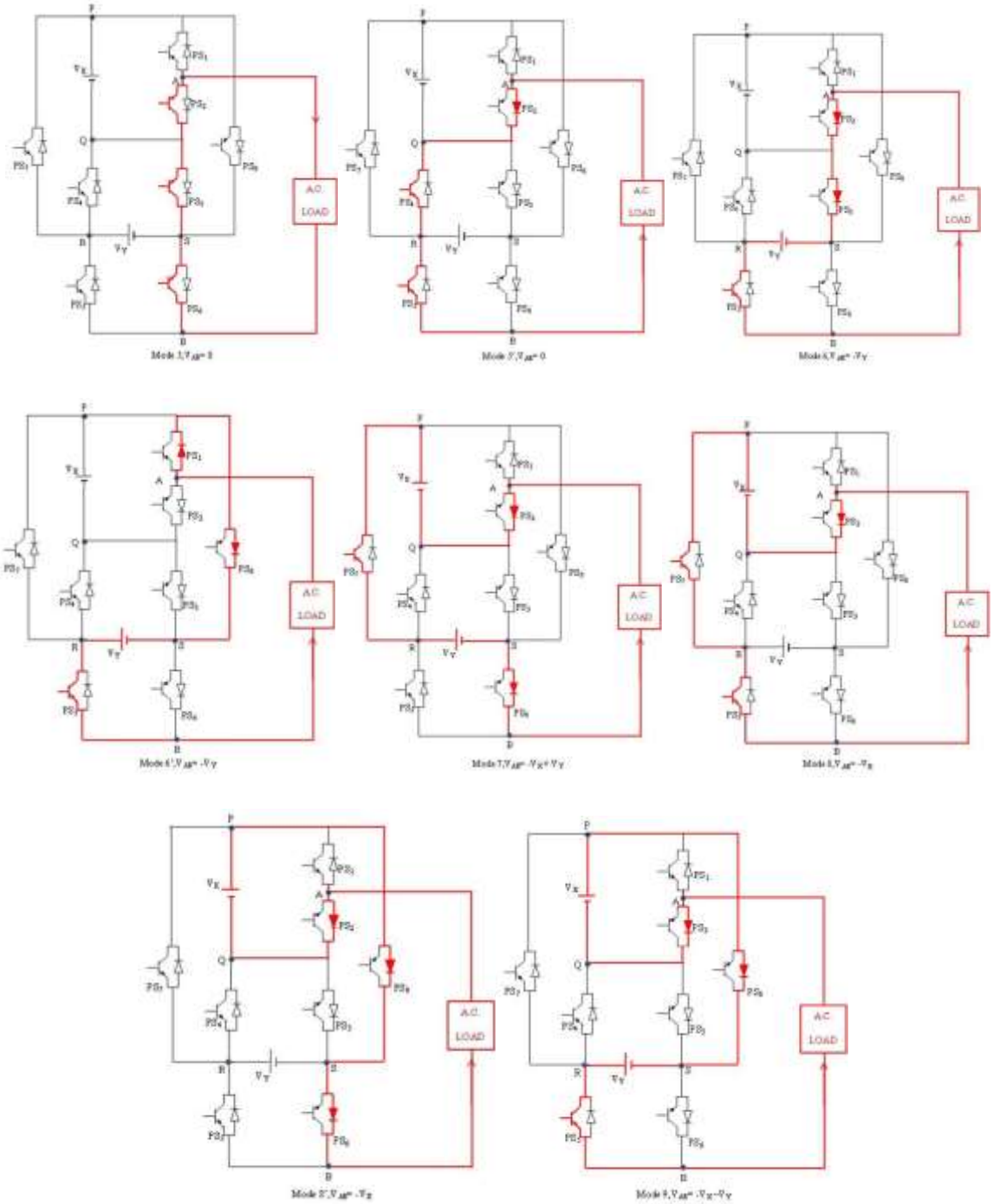


Figure 2. Operating modes of proposed multilevel topology

3. PERMANENT MAGNET SYNCHRONOUS MOTOR

In recent years permanent magnet synchronous motors (PMSM) are widely used in high performance drive applications such as industrial robots, machine tools automobiles etc. The power density of PMSM is higher than that of induction motor with the same ratings as stator power is not required for the magnetic field production. The use of permanent magnets has many advantages including the elimination of brushes, slip rings, and rotor copper losses in the field winding. It leads to higher efficiency. The lack of field winding and higher efficiency results in reduction of the machine frame size and higher power/weight ratio. Other advantages of the PMSM are low inertia, reliability and low cost of the power electronic converters required for controlling the machine [20]-[21]. All these facts make the PMSM an excellent alternative for many applications.

Permanent magnet synchronous motor drives using conventional three phase inverters have disadvantages of poor voltage and current qualities. To improve its performance, the switching frequency has to be raised which causes additional switching losses. Another option is to use filter between the inverter and motor, which causes additional weight. Multilevel inverter is good option for PMSM drive. As the number of levels increases, output waveform approaches to sine wave. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels. In this paper, three-phase novel symmetric and asymmetric topology is applied to PMSM and results are compared. Multicarrier sinusoidal pulse width modulation technique is used to generate pulses.

4. SIMULATION STUDY

The three phase five level symmetric, seven level binary asymmetric and nine level trinary asymmetric novel inverter and three phase permanent magnet synchronous motor are modelled in MATLAB/Simulink environment. Eight switches are used to obtain five level, seven level as well as nine level output voltage for each phase. Only by changing magnitude ratio of dc sources we can obtain flexibility in output voltage levels from same inverter module. All the switches in the simulations are considered to be ideal. The dc voltage sources used in the simulation studies are separate dc sources. These dc voltage sources are available in practice via distributed energy resources like photovoltaic panels, fuel cells and ultra- capacitors. If the available source is an ac source then the required dc voltage sources can be obtained by using rectifiers. The specifications of the PMSM and other parameters used for simulation are listed in Table 2.

Table 2. Simulation parameters

Description	Parameter	Value
Novel symmetric inverter	V_X	160.5 volts
	V_Y	160.5 volts
Novel binary asymmetric inverter	V_X	214 volts
	V_Y	107 volts
Novel trinary asymmetric inverter	V_X	240.75 volts
	V_Y	80.25 volts
Three phase permanent magnet synchronous motor	Stator resistance	2.875 ohms
	Rotor inductance	0.000835 H
	Flux linkage	0.1852 wb-turn
	Inertia	0.0001854 kg-m^2
	Friction factor	5.39e-5N-m.s
	Pole pairs	2

Simulation results for three phase voltage of novel symmetric five level inverter is shown in Figure 3 while stator currents ,electromagnetic torque and rotor speed of three phase PMSM fed by this symmetric inverter are presented in Figure 4. Figure 5 and 6 shows line voltage waveforms and harmonic contents of line voltage V_{AB} respectively. Figure 7 to 10 shows results for binary asymmetric seven level inverter. If we compare Figure 6 and 10 it is seen that THD in line voltage is reduced from 17.87% to 10.97% as number of levels in output voltage increases. Figure 11 to 14 shows simulation results for trinary asymmetric nine level inverter. There is further improvement in voltage quality, current quality, rotor settling time and torque ripples as compared to binary asymmetric inverter. Comparison among these three modules is given in Table 3.

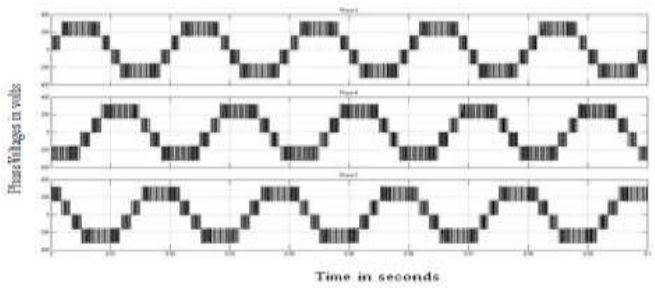


Figure 3. Three phase voltage waveform of novel symmetric five level inverter

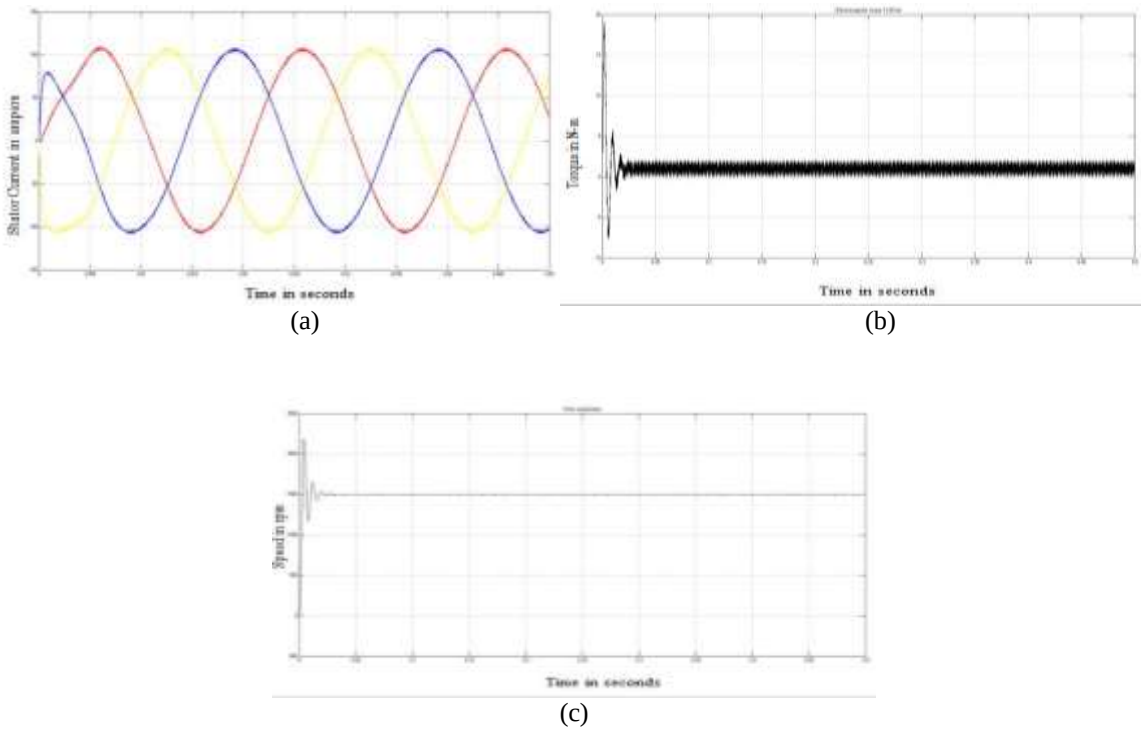


Figure 4. (a) Stator current (b)Electromagnetic torque (c) Rotor speed of three phase PMSM fed by novel symmetric five level inverter

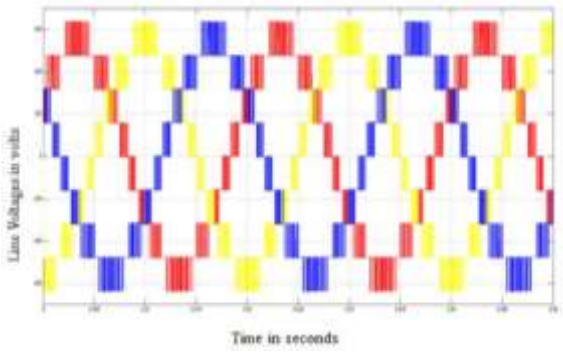


Figure 5. Line voltage waveform of novel symmetric five level inverter

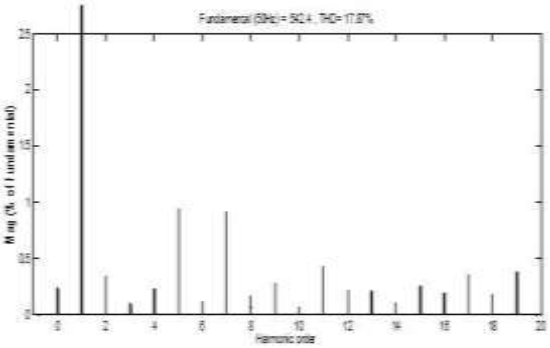


Figure 6. Harmonic analysis of line voltage V_{AB}

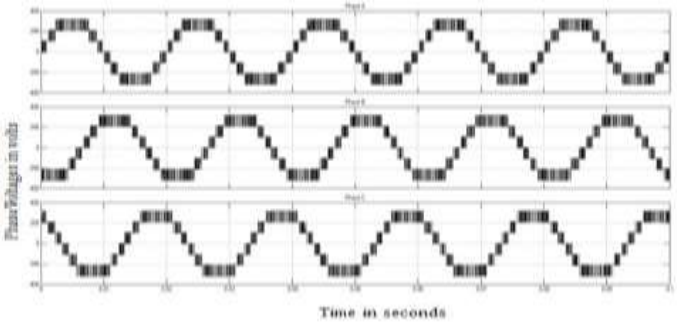
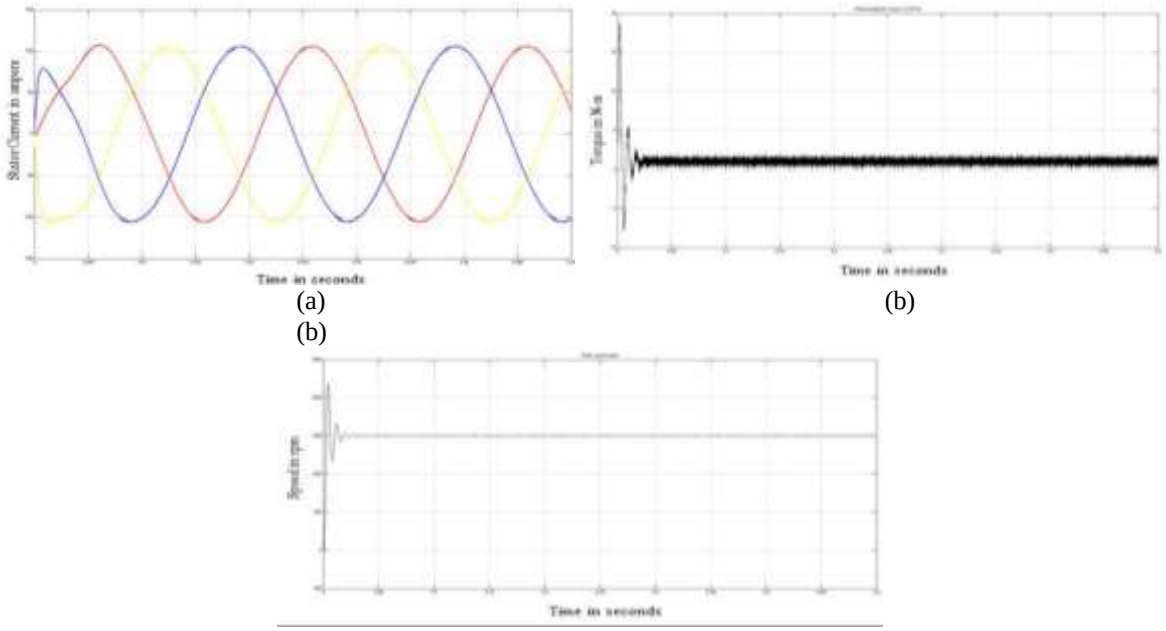


Figure 7. Three phase voltage waveform of novel binary asymmetric seven level inverter



(a) (b)

(b)

(c)

Figure 8. (a) Stator current (b) Electromagnetic torque (c) Rotor speed of three phase PMSM fed by novel binary asymmetric seven level inverter

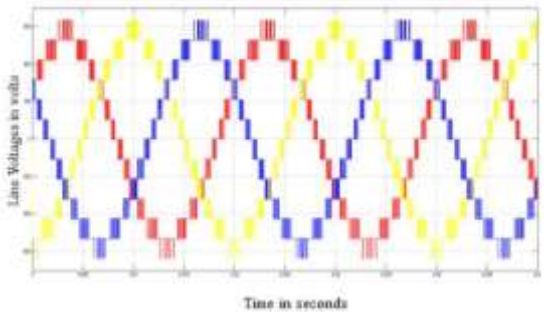


Figure 9. Line voltage waveform of novel binary asymmetric seven level inverter

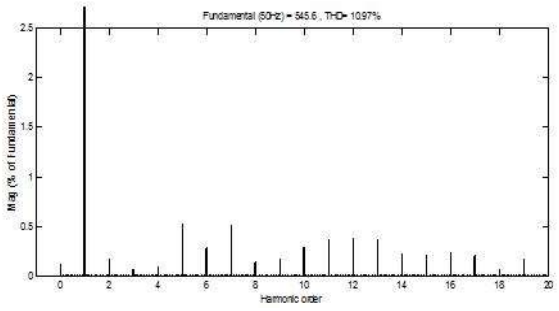


Figure 10. Harmonic analysis of line voltage V_{AB}

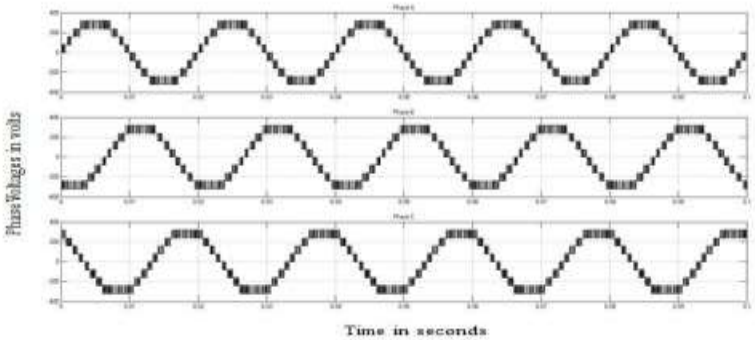
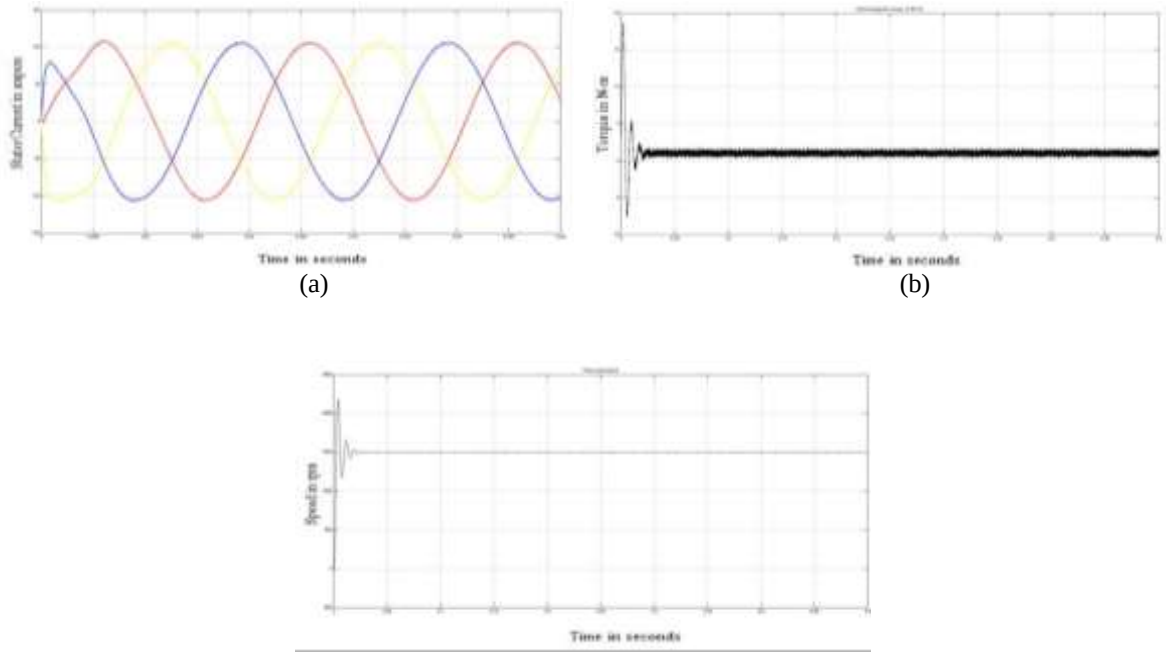


Figure 11. Three phase voltage waveform of novel trinary asymmetric nine level inverter



(a) (b)

(c)

Figure 12. (a) Stator current (b) Electromagnetic torque (c) Rotor speed of three phase PMSM fed by novel trinary asymmetric seven level inverter

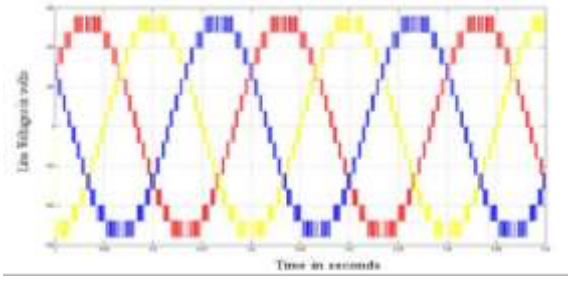


Figure 13. Line voltage waveform of novel trinary asymmetric nine level inverter

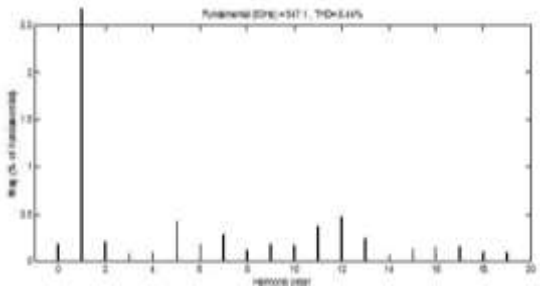


Figure 14. Harmonic analysis of line voltage V_{AB}

Table 3. Comparison of performance parameters of novel symmetric and asymmetric multilevel inverter

Parameters	Novel symmetric inverter $V_X = V_Y$	Novel asymmetric inverter	
		Binary asymmetric $V_X = 2V_Y$	Trinary asymmetric $V_X = 3V_Y$
Number of dc sources/phase	2	2	2
Number of switches/phase	8	8	8
Fundamental Frequency	50 Hz	50 Hz	50 Hz
Carrier frequency	5 KHz	5 KHz	5 KHz
Voltage levels	5	7	9
V_1 (Volts)	542.4	546.6	547.1
Voltage THD (%)	17.87	10.97	8.44
Current THD (%)	2.01	1.79	1.67

5. CONCLUSION

This paper proposes a novel multilevel inverter topology. This topology can be used in symmetric as well as asymmetric operating mode. The single unit shows flexibility in generating output voltage levels. It can generate five level (symmetric mode), seven level (binary asymmetric mode) or nine level (trinary asymmetric mode) output voltage.

Models of novel multilevel inverter operating in symmetric, binary asymmetric and trinary asymmetric mode are designed in MATLAB/Simulink to drive three phase PMSM. Multicarrier sinusoidal pulse width modulation technique is applied to produce switching pulses for eight power switches. The waveforms of output voltage, stator current, speed, electromagnetic torque for all the three models are compared. From simulation results it is seen that output voltage quality, current quality improves with increase in number of levels. Also rotor settling time and torque ripples are reduced.

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