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Implementation of Cascaded based Reversing Voltage Multilevel Inverter using Multi Carrier Modulation Strategies

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ABSTRACT

In this paper, a cascaded based reversing voltage (CBRV) multilevel inverter structure is proposed inorder to compensate the major drawbacks in the conventional multilevel inverters. The proposed topology requires less number of components, less carrier signals and gate drives when compared to existing multilevel inverters particularly at higher levels. Therefore, the complexity and overall cost are greatly reduced particularly for higher output voltage levels. This paper also presents the most relevant control and modulation methods by a triangular based multi carrier pulse width modulation (PWM) scheme for the proposed CBRV inverter topology. This paper presents a comparison between different modulation strategies for CBRV inverter topology based on sinusoidal and space vector references with multi triangular carrier waves. The work strive hard to present the scrutiny that has been made between various PWM control techniques for 1–Φ seven level CBRV inverter structure. The comparison is made in terms of Total Harmonic Distortion (THD) and fundamental RMS voltage. Finally, the simulation results are included to verify the effectiveness of the proposed CBRV inverter topology and validate the proposed theory. A hardware set up was developed for a 1–Φ seven level CBRV inverter topology using FPGA based pulse generation.

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1. INTRODUCTION

Multi-level inverters (MLIs) with various structures have more consideration in the recent implementations. These inverters are used in various applications such as electric vehicles, electric motor drives, active power filters, static compensators and renewable energy sources [1, 2]. Multilevel inverters have been considered for many advantages such as lower harmonics, high power quality, low electromagnetic interference and lower switching losses. The quality of a multi-level inverter is determined by the number of levels. But increasing the number of output levels leads to an increase in the number of components and thereby increases the complexity of control and also inverter operation. So,the number of semiconductor devices must be reduced. Conventional MLIs are classified as neutral point clamped (NPC), cascaded H-bridge (CHB) converters and flying capacitor (FC). These three types of MLIs require more number of components such as switches, clamping diodes and capacitors. As the number of voltage levels 'm' raises, the number of switches increases according to '2×(m-1)' for the conventional MLIs but for the proposed cascade based reversing voltage MLI (CBRV MLI) structure [10. 11] it is only 'm+3'.

This paper presents a 1–Φ seven level CBRV MLI structure based on multilevel dc link (MLDCL) and a full bridge inverter. When compared to the conventional MLIs, the proposed CBRV inverter strucure

can have superior performance by implementing the pulse width modulation (PWM) techniques. This paper also presents the most relevant control and modulation methods by a phase disposition multi carrier with modified spacevector PWM technique [8] for MLDCL inverter and comparing the performance of the proposed CBRV inverters with phase disposition multi carrier sine PWM technique and proposed CBRV structure validated experimentally through FPGA based pulse generation.

The block diagram of CBRV MLI is depicted in Figure 1 [3]. It consists of mainly level generator (LG) and polarity generator (PG) units to generate required number of levels [4]. The basic idea of the CBRV structure as a MLI is that the LG generates the required positive levels and the PG reverses the direction when the voltage polarity requires to be changed for negative polarity. In the proposed CBRV MLI structure there is no need to operate all the switches at high switching frequency, the LG unit switches operate at high frequency and PG unit switches operate at fundamental frequency. PG unit switches are used for reverse voltage appearance across the load and are triggered by simple pulse generator.

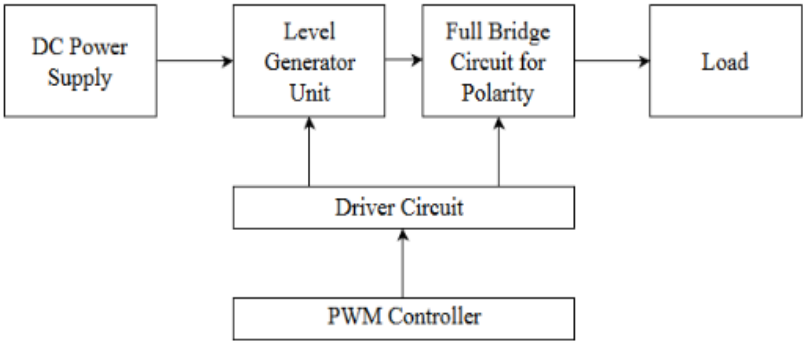

Figure1. Block Diagram of Proposed CBRV MLI

2. PROPOSED CBRV INVERTER STRUCTURE

The structure of the proposed 1–Φ CBRV MLI is shown in Figure 4. It consists of a multilevel dc source, LG unit, PG unit (single-phase full-bridge inverter) and a load [5, 6].

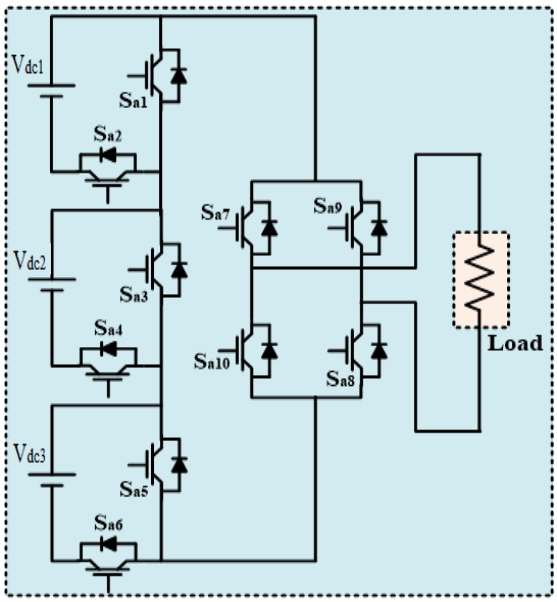

Figure 2. 1–Φ Seven Level CBRV Inverter

The components comparison for producing 1–Φ seven-level output voltage for the proposed CBRV and conventional cascaded based inverters are given in Table 1. It clearly shows substantial component reduction with the proposed CBRV MLI structure [8]. This saving in components increases as the number of

voltage level increases as mentioned before. For a 1–Φ seven-level CBRV inverter, the switching sequence to generate the required levels are given in Table 2.

Table 1: Components Comparison to Generate 1–Φ Seven-Level Output

Components	Proposed	Existing
Switches	10	12
Clamping diodes	0	0
Capacitors	0	0
DC sources	3	3

Table 2: Switching Sequence to Generate the 1–Φ Seven Level Output for CBRV Inverter

S.No	LG Unit		PG Unit		Voltage Levels
	On Switches	Off Switches	On Switches	Off Switches	
1	S_{a1}, S_{a3}, S_{a6}	S_{a2}, S_{a4}, S_{a5}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	+ V_{dc}
2	S_{a1}, S_{a4}, S_{a6}	S_{a2}, S_{a3}, S_{a5}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	+2 V_{dc}
3	S_{a2}, S_{a4}, S_{a6}	S_{a1}, S_{a3}, S_{a5}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	+3 V_{dc}
4	S_{a1}, S_{a3}, S_{a5}	S_{a2}, S_{a4}, S_{a6}	S_{a7}, S_{a8}	S_{a9}, S_{a10}	0
5	S_{a2}, S_{a4}, S_{a6}	S_{a1}, S_{a3}, S_{a5}	S_{a9}, S_{a10}	S_{a7}, S_{a8}	-3 V_{dc}
6	S_{a1}, S_{a4}, S_{a6}	S_{a2}, S_{a3}, S_{a5}	S_{a9}, S_{a10}	S_{a7}, S_{a8}	-2 V_{dc}
7	S_{a1}, S_{a3}, S_{a6}	S_{a2}, S_{a4}, S_{a5}	S_{a9}, S_{a10}	S_{a7}, S_{a8}	- V_{dc}

The maximum output voltage of LG unit for the proposed CBRV is obtained by using equation (1)

$$V_0, \max = \sum_{i=1}^{n} V_{dcn} \text{ ---------- } (1)$$

The equation (1) illustrates the output level of the LG unit and the positive and negative levels are synthesized by using the PG unit.
At load (V_o), the synthesized stepped output voltage level will be obtained by using the Equation (2) and (3).

$$V_0, \max = \sum_{i=1}^{n} + V_o, \text{ If } S_{a7}, S_{a8} = 1 \text{ ---------- } (2)$$

$$V_0, \max = \sum_{i=1}^{n} - V_0, \text{ If } S_{a9}, S_{a10} = 1 \text{ ---------- } (3)$$

3. PROPOSED MODULATION STRATEGIES

The pulse generation approach for the switches of LG unit and PG unit for the seven-level CBRV inverter are depicted in Figure 3.

3.1. Generation of Pulses for LG Unit

In this approach, multiple carrier modulation technique is incorporated into the sinusoidal PWM and modified space vector PWM techniques to produce PWM switching signals for the LG unit in the CBRV inverter. The proposed modulation scheme is based on the unipolar, symmetric PWM switching technique [7, 8]. It compares sinusoidal or space vector modulation signals along with in-phase level-shifted triangular carrier signals. These modified modulation signals have the same frequency 'f_0' and amplitude 'Ar'**.** Since the modulation is symmetric, the proposed modulation signals are sampled by the triangular carrier signal once in every carrier cycle. The carrier signal is a train of triangular waveform with frequency 'f_c', and amplitude 'A_c'. The pulse generation methodology is depicted in Figure 4 and 5 for the proposed seven level CBRV inverter using sinusoidal and space vector PWM strategies. For an m-level inverter, (m-1/2) carriers are needed to generate pulses for the proposed CBRV inverter i.e, for a seven level inverter three carrier signals (V_{tri1}, V_{tri2} and V_{tri3}) are used and these signals were compared with a reference signal (V_{ref}).

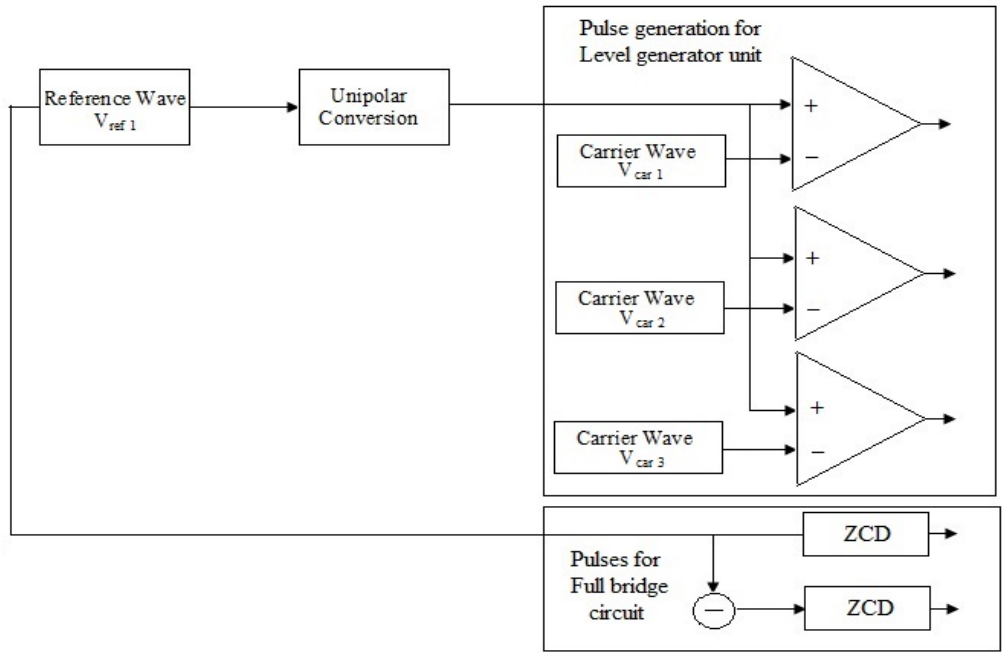

Figure 3. Generation of pulses for the proposed seven-level CBRV inverter

Theoretically, for a multiple carrier and a single reference signal, the modulation index (M) is defined by equation (4).

$$M = \frac{A_r}{\frac{(m-1)}{2} * A_c} \quad \text{----------} \quad (4)$$

where 'm' represents the number of levels.Hence, for the proposed RV seven level inverters, the modulation index (M) is defined by equation (5).

$$M = \frac{A_r}{3 * A_c} \quad \text{----------} \quad (5)$$

The principle of the proposed PWM techniques using in-phase triangular carrier for a seven-level CBRV inverter at M= 1 and m_f = 40 *is* shown in Figure 4 and 5 respectively. Instead of maintaining the same width of all pulses as in the case of multi-pulse modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse [1], and therefore THD is reduced significantly. The gating signals are generated by comparing a sinusoidal or space vector reference signal with a triangular carrier wave of frequency f_c. Figure 4 and 5 demonstrate the sine or space vector based in-phase triangle method for a single phase seven-level inverter. Therein, the phase modulation signal is compared with three ((n-1/2) in general) in-phase triangle waveforms to produce +3 V_{dc}, + 2V_{dc}, +V_{dc} and 0 using LG unit switches.

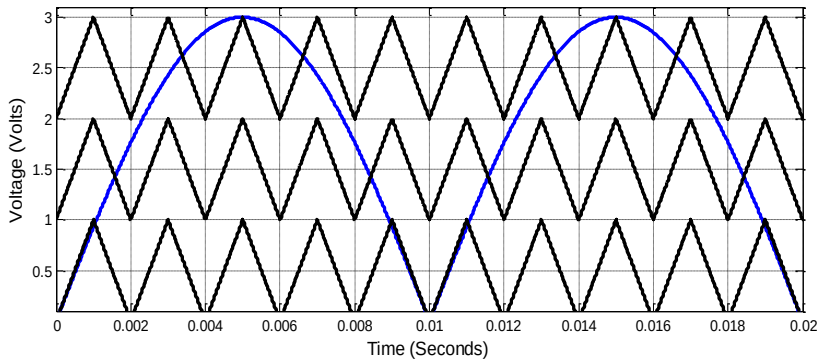

Figure 4.Multi Carrier Sinusoidal PWM with In-Phase Triangular Carrier (MCSPWM)

To achieve the maximum amplitude of the fundamental phase voltage, the offset voltage, V_{offset}, is added to the sinusoidal signal [9, 10], where the magnitude of V_{offset} is given by equation (6). The addition of the V_{offset} to the sinusoidal modulation signal results in space vector PWM technique [9].

$$V_{offset} = \frac{-(V_{max} + V_{min})}{2} \quad \text{----------} \quad (6)$$

In equation (6), V_{max} is the maximum magnitude of the sampled reference phase voltage, while V_{min} is the minimum magnitude of the three sampled reference phase voltage, in a sampling interval.

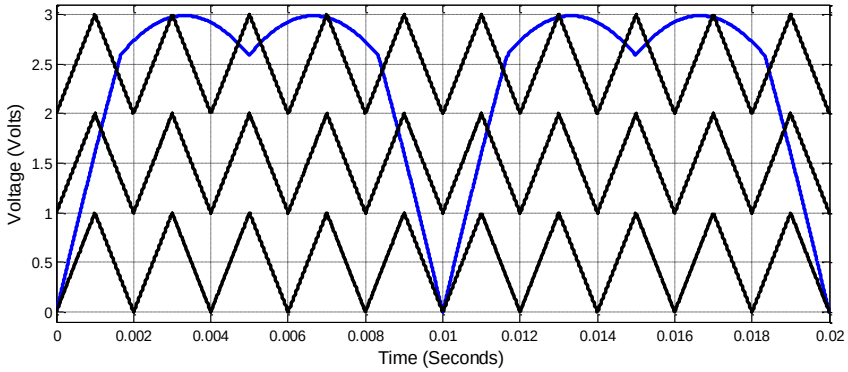

Figure 5.Multi Carrier Space Vector PWM with In-Phase Triangular Carrier (MCSVPWM)

3.2 Generation of pulses for PG unit:

Switches of PG unit are used to generate positive and negative levels of seven-level output voltage, which is triggered by using time based pulse generator with a fundamental frequency. The switches 'S_{a7}' and 'S_{a8}' are activated at the same instant initially with 0º delay using pulse generator and switches 'S_{a9}' and 'S_{a10}' are activated with delay of 180º. The switches 'S_{a7}' and 'S_{a8}' are activated to generate the positive levels of seven-level output across the load and the switches 'S_{a9}' and 'S_{a10}' are activated to generate negative levels of seven-level output to present across load. When the switches 'S_{a7}' and 'S_{a8}' are turned ON, the switches 'S_{a9}' and 'S_{a10}' are turned OFF and vice-versa.

4. SIMULATION RESULTS

The proposed 1–ϕ seven-level CBRV inverter has been simulated and analyzed for various modulation indices using MCSPWM and MCSVPWM strategies and the corresponding harmonic spectrum are presented. The simulation results of the 1–Φ seven-level CBRV inverter using MCSPWM and MCSVPWM with in-phase triangular carriers and its corresponding harmonic spectrum for M = 0.85 and mf = 100 are shown in the figures 6 to 9.

Simulation Parameters:

Input Voltage	=	300 Volts
Switching Frequency	=	5 KHz
Load Resistance	=	10 Ω

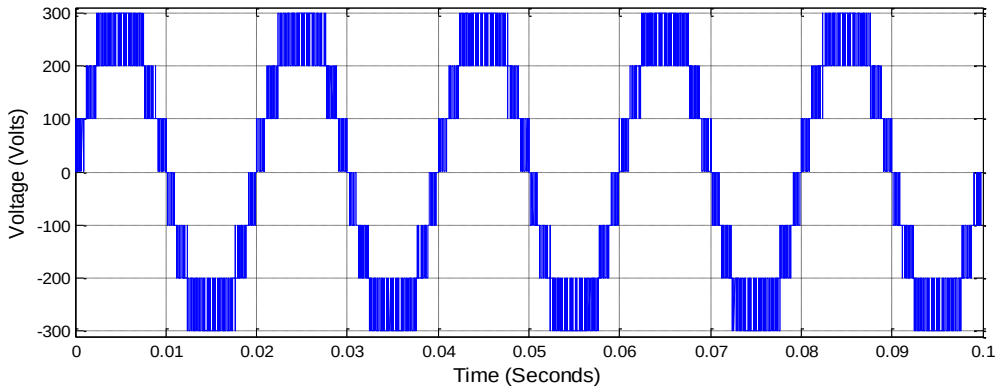

Figure 6. Phase voltage of 1–Φ seven-level CBRV inverter using MCSPWM (M=0.8 and m_f = 100)

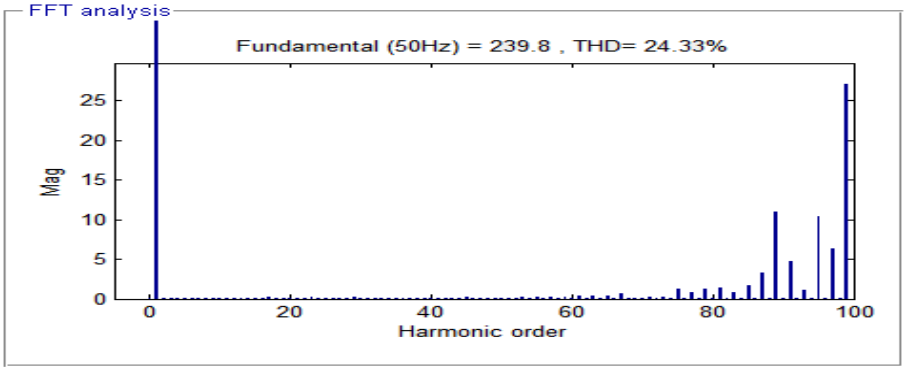

Figure 7. Harmonic spectrum of 1–Φ seven-level CBRV inverter using MCSPWM (M=0.8 and m_f = 100)

Figure 6 shows the simulation waveform of the seven-level CBRV inverter output using MCSPWM. The value of fundamental voltage of the inverter is 239.8 V (its RMS value is 169.6 V). Figure 7 shows the corresponding THD plot of the seven-level inverter. The %THD value of 7-level CBRV inverter is 24.33 %.

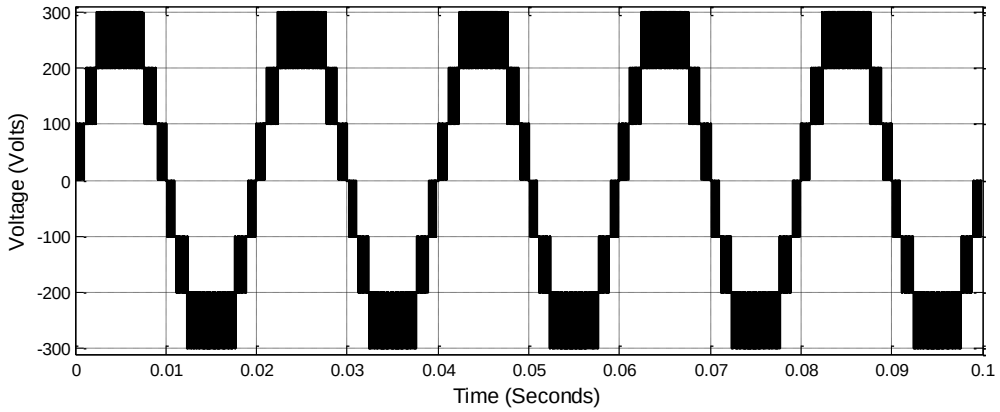

Figure 8. Phase voltage of 1–Φ seven-level CBRV inverter using MCSVPWM (M=0.8 and m_f = 100)

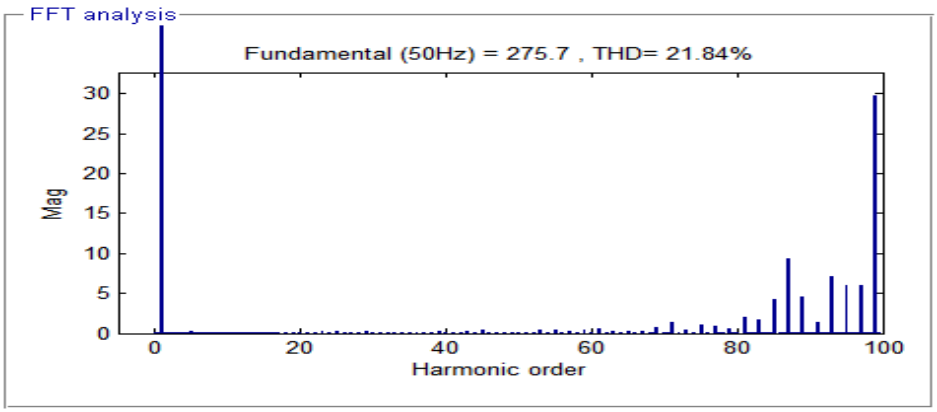

Figure 9. Harmonic Spectrum of 1–Φ Seven-Level CBRV Inverter Using MCSVPWM (M=0.8 and m_f = 100)

Figure 8 shows the simulation waveform of the seven-level CBRV inverter output using MCSPWM. The value of fundamental voltage of the inverter is 275.7 (its RMS value is 195 V). Figure 9 shows the corresponding THD plot of the seven-level inverter. The %THD value of 7-level CBRV inverter is 21.84 %.

Effect of Modulation index (M):
If M is in between $0 \leq M \leq 0.33$, only the first triangular wave (Vtri1) is compared with the reference signal, then the inverter behavior is similar to that of a conventional three-level PWM inverter. However, if M is more than 0.33 and less than 0.66, only Vtri1 and Vtri2 triangular signals are compared with the reference signal, then the output voltage consists of five voltage levels. The modulation index is set to be more than 0.66 to produce seven level output voltage. The effect of 'M' for the step changes in modulation indices with the corresponding load voltage is shown in Figure 10 to generate three, five and seven levels respectively [12].

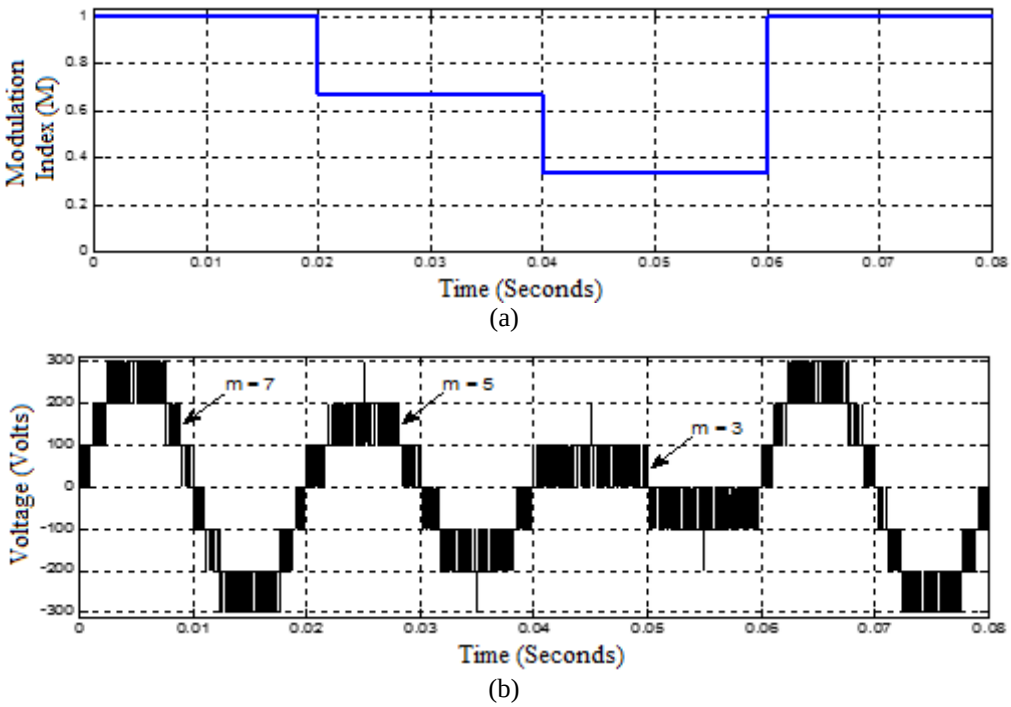

Figure 10. Dynamic response (a) step changes in modulation index (b) Phase voltage waveform

5. IMPLEMENTATION OF CBRV INVERTER USING FPGA BASED PULSE GENERATION

The prototype model of proposed cascaded based RV MLI is implemented using Xilinx Spartan FPGA [13,14] to validate the simulation results. The hardware realization circuit of the proposed system fed R-load is depicted in Figure 11 and 12. The prototype model consists of cascade based RV inverter, Resistive load, FPGA controller, PC, Buffer circuit, Opto isolator and Driver circuit.

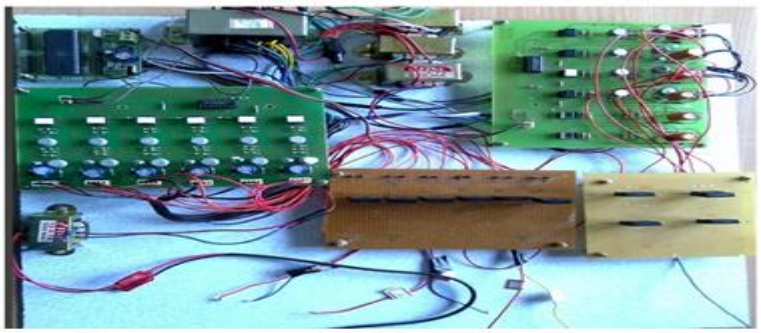

Figure 11. Implementation of 1-ϕ seven-level CBRV Inverter Using FPGA Processor

Figure 12. VHDL Code Successfully Embedded in FPGA for 1-ϕ Seven-Level CBRV Inverter

Generation of pulses using MCSPWM and MCSVPWM techniques through Xilinx ISE are depicted in Figure 13 and 14 respectively.

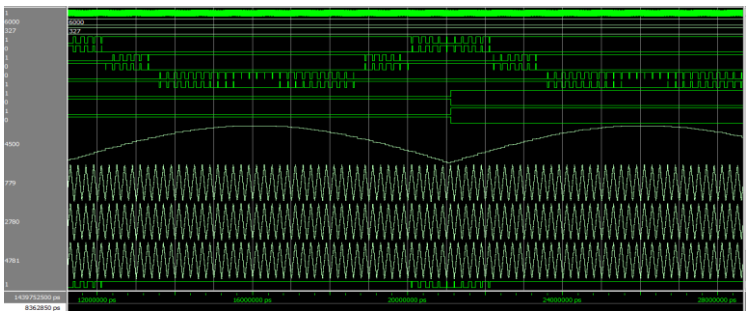

Figure 13. Generation of Pulses Using MCSPWM Method Through Xilinx ISE

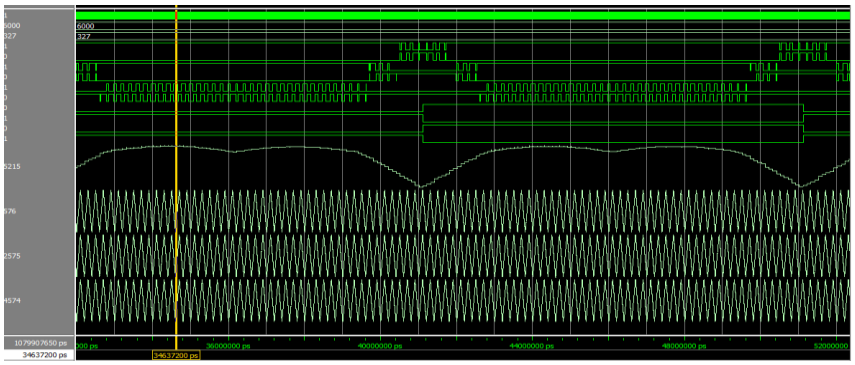

Figure 14. Generation of Pulses Using MCSVPWM Method through Xilinx ISE

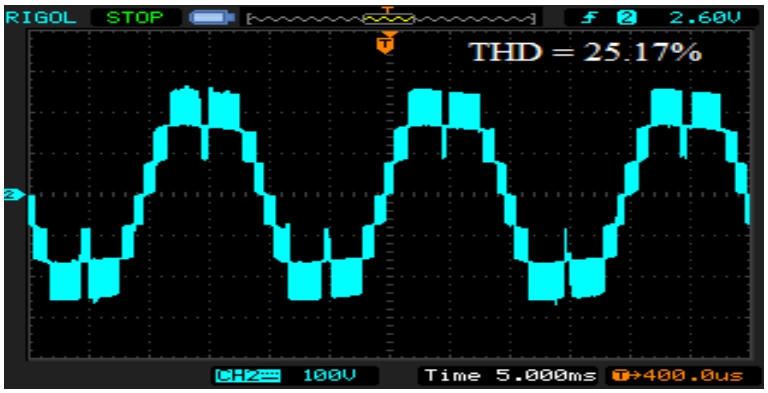

Figure 15. Experimental Output Phase Voltage of 1–Φ Seven-Level CBRV Inverter Using MCSPWM

Figure 15 shows the experimental output phase voltage waveform of seven-level CBRV inverter using MCSPWM. The RMS value of fundamental voltage of the inverter is 168.1 V. Figure 15 shows the corresponding THD plot of the seven-level inverter. The % THD value of seven-level CBRV inverter is 25.17 %.

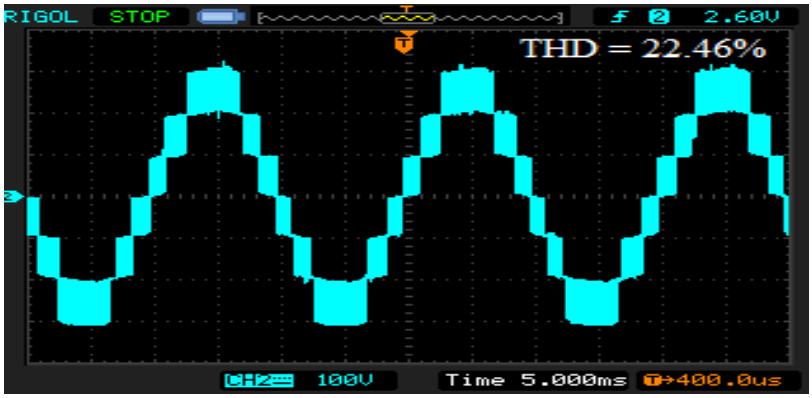

Figure 16. Experimental Output Phase Voltage of 1–ϕ Seven-Level CBRV Inverter Using MCSVPWM

Figure 16 shows the experimental output phase voltage waveform of seven-level CBRV inverter using MCSVPWM. The RMS value of fundamental voltage of the inverter is 193.2 V. Figure 15 shows the

corresponding THD plot of the seven-level inverter. The % THD value of seven-level CBRV inverter is 23.88 %.

6. COMPARISON OF SIMULATION AND EXPERIMENTAL RESULTS

In this section, simulation and experimental output phase voltage waveforms and corresponding THD spectrum of proposed 1-ϕ seven-level CBRV inverter system are depicted in Figure 6 to 16 for the MCSPWM and MCSVPWM modulation techniques respectively. Table 3 shows the simulation and experimental results of output phase voltage (Vrms) and harmonic content of CBRV inverter for different modulation indices. From the simulation and experimental analysis, it is observed that the maximum output phase voltage and lower THD is achieved by using MCSVPWM modulation technique. From the simulation harmonic spectral analysis, it is observed that the output voltage THD of the proposed 1-ϕ seven-level cascade based RV inverter system using MCSPWM and MCSVPWM modulation techniques are 24.33 % and 21.84 % respectively for the modulation index of 0.8. Harmonic spectrum of the prototype system for the proposed modulation techniques are carried using digital storage oscilloscope and the results are presented in figures 11 to 16 for MCSPWM and MCSVPWM modulation techniques respectively. It is observed that the THD of output voltages are 25.17 % and 22.46 % respectively for the modulation index of 0.85.

Table 3: Fundamental Output Voltage (V_{rms}) and % THD of 1–Φ Seven-Level CBRV Inverter Using MCSPWM and MCSVPWM

Modulation Index (M)	Number of Levels	PWM Technique							
		MCSPWM				MCSVPWM			
		Simulation		Experimental		Simulation		Experimental	
		V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)
0.8	7- Level	169.6	24.33	168.1	25.17	195	21.84	193.2	22.46
0.7	7- Level	148.4	25.31	145.8	26.7	170.8	24.27	168.6	25.6
0.6	5- Level	127.3	33.46	125.9	35.1	146.3	25.58	144.5	27.1
0.5	5- Level	106	40.23	104.7	42.3	121.9	35.47	119.7	36.3
0.4	5- Level	84.79	44.52	83.1	46.2	97.52	42.13	95.8	44.3
0.3	3-Level	63.57	64.54	61.4	65.8	73.23	49.36	75.4	51.2

Therefore from table 3, it is observed that the simulation results are validated with the experimental results with an acceptable error of ± 2%. From the analysis, it is noticed that the magnitude of output voltage and number of levels vary for different modulation indices.

7. CONCLUSION

Comparing with counterpart well-known and recent MLI structures, the proposed CBRVinverter structure came with reduced number of switching devices, gate driver circuits, DC voltage supplies, carrier signals and less installation area. The proposed RV inverters are used in power applications such as HVDC, PV systems, Back to Back converters, Reactive power compensation, UPS, FACTS etc. In the proposed structure, the switching operation is separated into high- and low- frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype.The modified modulation techniques depends on the switching states of inverter and was successfully implemented using FPGA based pulse generation.

REFERENCES

[1] J.Rodríguez, J.S.Lai, and F. Z.Peng,"Multilevel Inverters: A Survey of Topologies, Controls, and Applications", *IEEETransactions on Industrial Electronics*, Vol. 49, No. 4, August 2002, pp.724-739.

[2] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A Comparison of Diode-Clamped and Cascade Multilevel Converters for a STATCOM with Energy Storage," *IEEE Transaction on Industrial Electronics*, Vol. 53, No. 5, 2006, pp. 1512-1521. doi:10.1109/TIE.2006.882022.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez and M. Perez, "A Survey on Cascade Multilevel Inverters," *IEEE Transaction on Industrial Electronics*, Vol. 57, No. 7, 2009, pp. 2197-2206. doi:10.1109/TIE.2009.2030767.

[4] Su G.J and Adams D. J., *'Multilevel DC link inverter for brushless permanent magnet motors with very low inductance,"* in Conf. Rec. 2001 IEEE-IAS Annu. Meeting, vol. 2, pp. 829-834.

[5] Gui-Jia Su'Multilevel DC link inverter' Industry applications, *IEEE Transactions* on Volume: 41, Issue: 3 Digital Object Identifier: 10.1109/TIA. 2005.847306. Publication Year: 2005, pp.848-854.

[6] Kangarlu MF, Babaei E, Sabahi M. "Cascaded cross-switched multilevel inverter in symmetric and asymmetric conditions". *IET Power Electronics.* 2013; 6(6):1041–1050.
[7] Shantanu Chatterjee, "A Multilevel Inverter Based on SVPWM Technique for Photovoltaic Application," *International Journal of Power Electronics and Drive System (IJPEDS),* vol. 3, no. 1, pp. 62 -73, 2013.
[8] Rao, S.N.; Kumar, D.V.A.; Babu, C.S., "*New multilevel inverter topology with reduced number of switches using advanced modulation strategies*," Power, Energy and Control (ICPEC), 2013 International Conference on,pp. 693-699, 6-8 Feb. 2013 doi: 10.1109/ICPEC.2013.6527745.
[9] DevisreeSasi, et al., "Generalized SVPWM Algorithm for Two Legged Three Phase Multilevel Inverter", *International Journal of Power Electronics and Drive System (IJPEDS),* Vol.3, no.3, pp. 279-286, 2013.
[10] Y. Suresh Anup Kumar Panda "Investigation on hybrid cascaded multilevel inverter with reduced dc sources" *Renewable and Sustainable Energy Reviews* vol. 26 pp. 49-59 2013.
[11] Ebrahimi J., Babaei E., and Gharehpetian G.B.,"A New Topology of Cascaded Multilevel Converters with Reduced Number of Components for High-Voltage Applications" *IEEE Power Electron. Soc*., vol. 26, no. 11, pp. 3109-3118, Nov.2011.
[12] L.Ben-brahim and S.Tadakuma, ''Novel Multilevel Carrier Based PWM Control Method for GTO Inverter in Low Index Modulation Region'' *IEEE Transactions on Power Electronics*, Vol. 18, No. 1, January 2006 42(1), 121-127.
[13] VNB Reddy,; Rao, S.N.; Babu, C.S., " *Emphasis of Modulated Techniques for Cascaded Multilevel Inverters fed drive using FPGA,"* Power, Energy and Control (ICPEC), 2013 International Conference on, vol., no., pp. 686-692, 6-8 Feb. 2013 doi: 10.1109/ICPEC.2013.6527744.
[14] V. Naga Bhaskar Reddy, S. Nagaraja Rao, Ch. Sai Babu,''Advanced Modulating Techniques for Multilevel Inverters by Using FPGA'', *International Review of Electrical Engineering (IREE),* vol. 5. n. 3, May 2010,pp. 842-848.

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