

















































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
















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## Bidirectional single-loop current sensorless control applied to NPC multi-level converter considering conduction losses

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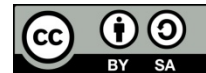
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### ABSTRACT

The current feedback is considered as unavoidable part of most control system driving power electronic converters. However, it is possible to eliminate the use of current sensor, if properly calculated volt-second balance is applied to input inductor. This paper describes the implementation of current sensorless control technique applied to neutral point clamped multi-level converter, where only voltage control-loop is used to stabilize internal capacitors voltage, while inductor's current is shaped by means of current sensorless control block in both discontinuous and continuous current modes. The capacitor voltage balancing is implemented by means of delta-controller that selects alternative capacitor in respect to main switching scheme. Finally, the analytical study of proposed solution is verified with simulation results.

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## 1. INTRODUCTION

Awareness of human impact on the environment resulted in increasing use of renewable energy sources [1] that in turn contributed to the development of power electronics applications: interface converters for renewable energy sources [2], reversible converters for energy storage systems [3]. Moreover, standards that govern the quality of electrical energy consumed from the network forces to use more efficient power supply blocks with utilisation of power factor correction schemes. As a result, the application sphere of modern switched mode power supplies is targeting wide range of nominal power [4]. The necessity of PFC is clearly demonstrated in [5], where it is concluded that household electrical appliances with poor PF can impact the voltage at the feeder terminal. Variety of power electronic topologies with power factor correction feature have been introduced and studied in the literature [6–14]. The effect of different PFC control approaches operating at distorted input voltage have been studied in [15], where it is stated that sinusoidal current consumption is better than emulated resistor behavior.

New enabling materials for power switches allow designing transistors with high electron mobility featuring higher switching frequencies, wide bandgap transistors allows higher blocking voltages, as well as production technology itself (GaN multi block) allows minimizing switching losses [16–21]. At the same time, development of digital control systems allows implementing advanced control algorithms for power electronic converters that also leads to increased converter's total performance. Specifically, the focus is made on new current control approaches that directly influence overall merits: the total harmonic distortion, unity power factor, converters' dynamics, ability to control current in mixed conduction mode, etc [22–28].

### 1.1. Literature overview on control methods

Presently most of current controlled power electronics converters are usually driven with traditional type of control strategies, where two control loops are implemented – one (slow) voltage control loop that stabilizes DC bus voltage, second (fast) current control loop that shapes the current form sinked/sourced from/to the grid (see Figure 1(a)). The current control loop is usually implemented with one of traditional current control techniques: hysteresis control, PID, proportional resonant, space vector PWM. All mentioned current control approaches are based on instantaneous current sampling, that utilises shunt resistor or galvanically isolated current sensor. The first one introduces additional power losses due to active resistance, while latter is costly and has limited bandwidth that limits its application with modern power electronic converters operating at higher commutation frequencies.

<sup>[1]</sup> Thus, to eliminate drawbacks caused by current sensor, current sensorless control algorithm has been studied. It allows eliminating instantaneous current measurement. Various researches have been conducted in this relation, where different implementations have been demonstrated. In [29–32] researchers have implemented CSC, where mathematical current rebuilding block is introduced that rebuilds the current based on PWM signals and precise model of converter (see Figure 1 (b)). Calculated value from mathematical block is compared with reference current shape and error is entered to PI block that adjusts the duty ratio of PWM signals. In this case, still two control loops are utilized.

Some other researches [33–35] have minimized the number of current sensors by introducing current decoder block. It estimates AC-side and each capacitor currents depending on the state of transistors. These researches are usually entitled “AC current sensorless approach...”, meaning that only AC current sensor is eliminated. Interesting research results are published in [36], where only one DC-side voltage sensor is used to control three-phase boost PFC converter, while all other parameters are estimated based on predefined converter parameters and pulsations of DC capacitor.

So-called single-loop current sensorless control (CSC) approach has been introduced in 2000 [37]. This type of control utilises only one control loop with feedback from the output capacitor voltage and does not use any current feedback signal as it is assumed that inductor's volt-second balance is perfectly calculated and inductor's current follows the reference signal (see Figure 1 (c)). Since that time the CSC has been applied to multiple type of PFC topologies: single switch PFC (diode bridge and boost converter) [38], [39], interleaved [40], [41], bridgeless [42], [43], half-bridge [44–46], full-bridge [47], [48] and also neutral-point clamped multi-level converter (NPC MLC) [49], [50]. Several recently published papers have been devoted to different type of three-phase converter topologies operated under CSC [51–53] that makes evidence of CSC use in high power applications.

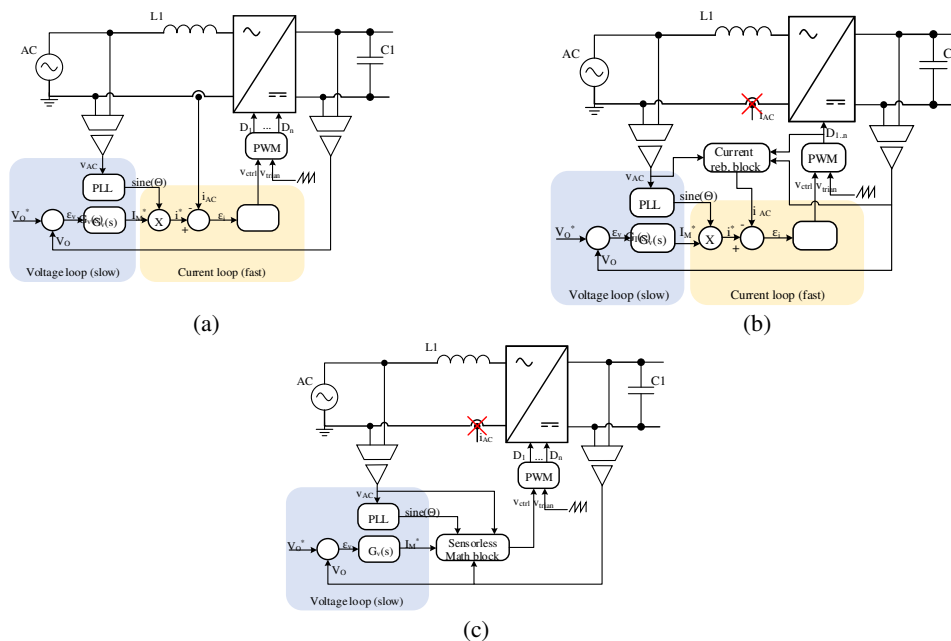


Figure 1. Preview of different control schemes used in PFC converters: <sup>[21]</sup> (a) Traditional double loop control scheme, (b) CSC scheme with current rebuilding block, (c) Single-loop CSC scheme

Most of mentioned CSC research papers deal with ideal models of semiconductor switches and do not consider conduction losses caused by parasitic circuit elements. The effect of neglecting parasitic losses on the shape of grid current is discussed in the literature [54–57], where multiple solutions are proposed to overcome this problem: current error compensators, adaptive inductor model and continuous estimation of parasitics based on zero-current detection. Negative effect of parasitic circuit components on the current shape increases with the number of transistors in the current path of the converter topology that is actual to MLC type of converter (see Fehler! Verweisquelle konnte nicht gefunden werden.). Thus, this paper is devoted to definition of single-loop CSC algorithm for NPC MLC with bidirectional current control and consideration of conduction losses. To the best knowledge of the authors, this type of control has not been described in the literature yet and potentially is interesting to industry due to economical and efficiency effect that will be stated at the end of this paper.

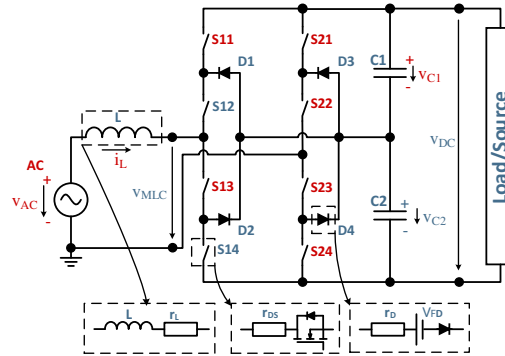


Figure 2. Power circuit topology of a neutral point clamped multilevel converter with considered parasitic components

## 2. RESEARCH METHOD

The research of original idea is based on analytical study of electrical circuit. The analytical analysis for duty cycle calculation equations are made describing both continuous and discontinuous operation modes. The analysis of all switching states of MLC converter is done, for each of which the identification of inductor voltage equation is made. In order to minimise the number of equations that are used to describe inductor's voltage the single-switch model is utilised. The proposed control approach is verified by means of simulation analysis demonstrating its performance during different step-response cases: changing load from light to nominal value, changing power flow direction back and forward, as well as THD performance is provided at different power ratings.

### 2.1. Definition of transition between operational voltage levels

The main goal of CSC is to provide proper volt-second balance applied to input inductor that would keep average inductor current to follow the sinusoidal reference. As the inductor might operate in discontinuous and continuous conduction mode (DCM and CCM), two calculation equations should be obtained.

The MLC converter is driven with PWM signal generated by control system that determine two basic states: 1) boosting inductor's energy and 2) releasing inductor's energy. The duty ratio of PWM signal is set by output signal ( $v_{CTRL}$ ) from control system that is compared with triangle voltage as follows:

$$d(t) = \begin{cases} 1, & \text{if } v_{CTRL}(t) \geq v_{trian}(t) \\ 0, & \text{otherwise} \end{cases} \quad (1)$$

Transition between different voltage levels are defined depending on the grid voltage ( $V_{AC}$ ) in respect to internal DC bus voltage ( $V_{DC}$ ):

$$LVL(t) = \begin{cases} 1, & \text{if } |v_{AC}(t)| \geq 0.5 \cdot v_{DC}(t) \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

Depending on MLC power flow direction (positive current amplitude ( $I_{M0}$ ) is assumed as rectifier mode, negative current amplitude ( $I_{M0}$ ) – inverter mode) and value of AC voltage different DC voltage is commutated at the AC-side of MLC converter during two states of PWM signal:



$$V_{MLC} \quad d=1 = \begin{cases} 0, \text{ if } I_M = 0 \text{ and } LVL(t) = 0 \\ V_{DC} \text{ if } I_M = 0 \text{ and } LVL(t) = 1 \\ V_{DC} \text{ if } I_M = 0 \text{ and } LVL(t) = 0 \\ \{ V_{DC}, \text{ if } I_M = 0 \text{ and } LVL(t) = 1 \end{cases} \quad (3)$$

$$V_{MLC} \quad d=0 = \begin{cases} V_{DC} \text{ if } I_M = 0 \text{ and } LVL(t) = 0 \\ V_{DC}, \text{ if } I_M = 0 \text{ and } LVL(t) = 1 \\ 0, \text{ if } I_M = 0 \text{ and } LVL(t) = 0 \\ \{ V_{DC} \text{ if } I_M = 0 \text{ and } LVL(t) = 1 \end{cases} \quad (4)$$

## 2.2. Definition of control laws for DCM and CCM

The control law of inductor's current in DCM differs significantly from CCM. The current always starts from zero in DCM and average inductor current has squared ratio to transistor's conduction time (see Figure 3(a)). Contrary to DCM, average current value has proportional ratio to conduction time during CCM and starting point of rising current is equal to the end value falling edge of previous switching cycle (Figure 3(b)). This potentially leads to the problem that the error of control signal can be accumulated and the current form can degrade significantly.

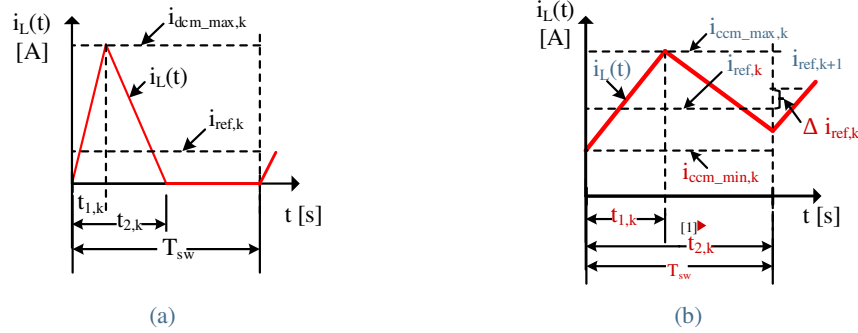


Figure 3. Current waveform during (a) DCM and (b) CCM

The equation that would allow to calculate the duty ratio for PWM signal during DCM could be estimated from the following definition:

$$i_{ref,k} = \frac{1}{T_{sw}} \int_{t_1,k}^{(k+1) \cdot T_{sw}} I_M \cdot \sin(t) dt \neq \frac{1}{T_{sw}} \int_{t_1,k}^{(k+1) \cdot T_{sw}} i_L(t) dt \quad (5)$$

Assuming that inductor current is rising and falling linearly, the equation above can be rewritten as

$$i_{ref,k} = \frac{1}{T_{sw}} \left( \int_0^{t_1} \frac{v_L^{d=1}(t)}{L} dt + \int_{t_1}^{t_2} \frac{v_L^{d=0}(t)}{L} dt \right) \quad (6)$$

Taking into account, that grid voltage and also capacitor voltage are almost invariable during single switching cycle, the voltage applied to inductor can be assumed as constant. Thus, the equation above allows defining the ratio between turn-on and turn-off time ( $t_{2,k}$  and  $t_{1,k}$  correspondingly) for the converter operating in DCM:

$$t_{2,k} = \left(1 - \frac{v_{L,k}}{v_{L,k}^{d=1}}\right) \cdot t_{1,k} \quad (7)$$

Inductor's peak current value can be defined as follows:

$$i_{DCM\_max,k} = \frac{v_{L,k}}{L} \cdot t_{1,k} \quad (8)$$

The DCM control equation can be found by using simple triangle area definition formula, substituting height of the triangle with (8) and base with (7). The resulted control law is seen below:

$$D_{DCM,k} = \frac{t_{1,k}}{T_{sw}} = \sqrt{\frac{2 \cdot L \cdot i_{ref,k}}{T_{sw}} \cdot \frac{\theta_{L,k}^{d=0}}{v_{L,k}^{d=1} \cdot (v_{L,k}^{d=0} - v_{L,k}^{d=1})}} \quad (9)$$

The control of transistor during CCM ensures that average inductor current will follow the changes of reference value that is described as:

$$\Delta i_{ref,k} = \frac{v_{L,k}}{L} \cdot t_{1,k} + \frac{d_{\theta_{L,k}}^{d=0}}{L} \cdot (T_{sw} - t_{1,k}). \quad (10)$$

Consequently, the CCM current control law can be defined as follows

$$D_{CCM,k} = \frac{t_{1,k}}{T_{sw}} = \frac{\frac{\Delta i_{ref,k} \cdot L}{T_{sw}} \cdot \frac{d_{\theta_{L,k}}^{d=0}}{v_{L,k}}}{v_{L,k}^{d=1} - v_{L,k}^{d=0}}. \quad (11)$$

The  $D_{CCM}$  crosses the  $D_{DCM}$  control function at the boundary conduction mode and has smaller value in CCM. Thus, the resulted control law is selected as minimal value out of both control laws.

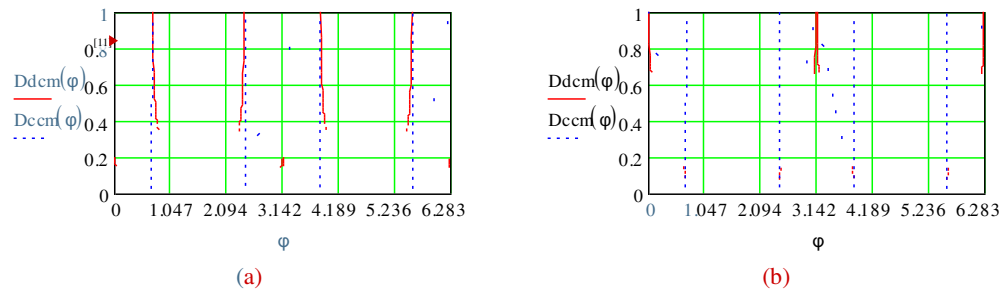


Figure 4. Preview of DCM and CCM duty ratios for (a) inductor operating only in DCM ( $I_M=0.1$  A) and (b) in mixed conduction mode ( $I_M=2.5$  A)

### 2.3. Definition of inductor voltage considering conduction losses

The Table 1 demonstrate all switching states of MLC for all operation modes and the equations of inductor's voltage are defined as well for each switching state. Keeping in mind that MLC allows commutating single capacitor voltage to AC input, it is assumed that during positive AC voltage the C1 capacitor is mainly used and capacitor C2 – during negative half-period. Opposite capacitor commutation logic can be used for capacitor voltage balancing (see Table 2).

As can be seen from Table 1, inductor's voltage equations are constituted by multiple variables, which might change its sign and integer coefficient. For this reason, two bool functions are defined that can help to track the changes of variables:

$$sign(x) = \begin{cases} -1, & \text{if } x < 0, \\ 1, & \text{if } x \geq 0 \end{cases} \quad (12)$$

$$gtz(x) = \begin{cases} 0, & \text{if } x < 0, \\ 1, & \text{if } x \geq 0 \end{cases} \quad (13)$$

As previously mentioned, there is main capacitor that is commutated during half-period of input voltage that can be formulated as follows:

$$v_{C\_main,k} = gtz(v_{AC,k}) \cdot v_{C1,k} + gtz(-v_{AC,k}) \cdot v_{C2,k}. \quad (14)$$

The number of switches ( $N_{SW}$ ) and number of diodes ( $N_D$ ) in the current path in both energy storing ( $d=1$ ) and energy releasing ( $d=0$ ) states can be defined as follows:

$$N_{SW,k}^{d=1} = gtz(I_M) \cdot (2 + LVL_k) + gtz(-I_M) \cdot (3 + LVL_k), \quad (15)$$

$$N_{SW,k}^{d=0} = gtz(I_M) \cdot (3 + LVL_k) + gtz(-I_M) \cdot (2 + LVL_k), \quad (16)$$

$$N_{D,k}^{d=1} = 4 - N_{SW,k}^{d=1} \quad (17)$$

$$N_{D,k}^{d=0} = 4 - N_{SW,k}^{d=0} \quad (18)$$

Table 1.<sup>[2]</sup> Summary of normal switching states of MLC converter and corresponding inductor voltage equation

Power flow	Input voltage polarity	Input voltage level	Switch state d(t)	S11	S12	S13	S14	S21	S22	S23	S24	Inductor's voltage
Rectifier ( $I_{k0}$ )	Positive	$ V_{Acl}  0.5V_{DC}$	1	-	-	1	-	-	1	-	-	$V_L = V_{AC} - 2 \cdot V_{FD} - I_{ref}(r_L + 2 \cdot r_{DS} + 2 \cdot r_D)$
			0	1	1	-	-	-	1	-	-	$V_L = V_{AC} - V_{C1} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$
		$ V_{Acl}  0.5^{[1]} V_{DC}$	1	1	1	-	-	-	1	-	-	$V_L = V_{AC} - V_{C1} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$
			0	1	1	-	-	-	-	1	1	$V_L = V_{AC} - V_{C1} - V_{C2} - I_{ref}(r_L + 4 \cdot r_{DS})$
	Negative	$ V_{Acl}  0.5 V_{DC}$	1	-	1	-	-	-	-	1	-	$V_L = -V_{AC} - 2 \cdot V_{FD} - I_{ref}(r_L + 2 \cdot r_{DS} + 2 \cdot r_D)$
			0	-	-	1	1	-	-	1	-	$V_L = -V_{AC} - V_{C2} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$
		$ V_{Acl}  0.5^{[1]} V_{DC}$	1	-	-	1	1	-	-	1	-	$V_L = -V_{AC} - V_{C2} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$
			0	-	-	1	1	1	1	-	-	$V_L = -V_{AC} - V_{C1} - V_{C2} - I_{ref}(r_L + 4 \cdot r_{DS})$
Inverter ( $I_{k0}$ )	Positive	$ V_{Acl}  0.5 V_{DC}$	1	1	1	-	-	-	-	1	-	$V_L = -V_{AC} + V_{C1} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$
			0	-	1	-	-	-	-	1	-	$V_L = -V_{AC} - 2 \cdot V_{FD} - I_{ref}(r_L + 2 \cdot r_{DS} + 2 \cdot r_D)$
		$ V_{Acl}  0.5^{[1]} V_{DC}$	1	1	1	-	-	-	-	1	1	$V_L = -V_{AC} + V_{C1} + V_{C2} - I_{ref}(r_L + 4 \cdot r_{DS})$
			0	1	1	-	-	-	-	1	-	$V_L = -V_{AC} + V_{C1} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$
	Negative	$ V_{Acl}  0.5 V_{DC}$	1	-	-	1	1	-	1	-	-	$V_L = V_{AC} + V_{C2} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$
			0	-	-	1	-	-	1	-	-	$V_L = V_{AC} - 2 \cdot V_{FD} - I_{ref}(r_L + 2 \cdot r_{DS} + 2 \cdot r_D)$
		$ V_{Acl}  0.5^{[1]} V_{DC}$	1	-	-	1	1	1	1	-	-	$V_L = V_{AC} + V_{C1} + V_{C2} - I_{ref}(r_L + 4 \cdot r_{DS})$
			0	-	-	1	1	-	1	-	-	$V_L = V_{AC} + V_{C2} - V_{FD} - I_{ref}(r_L + 3 \cdot r_{DS} + r_D)$

Table 2.<sup>[1]</sup> Switching states used for capacitor balancing

Power flow	Input voltage polarity	Input voltage level	Active state d(t)	S11	S12	S13	S14	S21	S22	S23	S24	Simplified inductor's voltage	dV <sub>C1</sub>	dV <sub>C2</sub>
Rectifier ( $I_{k0}$ )	Positive	$ V_{Acl}  0.5^{[1]} V_{DC}$	0	-	-	1	-	-	-	1	1	$V_L = V_{AC} - V_{C2}$	0	+
				1	1	-	-	-	1	-	-	$V_L = V_{AC} - V_{C1}$	+	0
		$ V_{Acl}  0.5^{[1]} V_{DC}$	1	1	1	-	-	-	1	-	-	$V_L = V_{AC} - V_{C1}$	+	0
				-	-	1	-	-	-	1	1	$V_L = V_{AC} - V_{C2}$	0	+
	Negative	$ V_{Acl}  0.5 V_{DC}$	0	-	1	-	-	1	1	-	-	$V_L = V_{AC} - V_{C1}$	+	0
				-	-	1	1	-	-	1	-	$V_L = V_{AC} - V_{C2}$	0	+
		$ V_{Acl}  0.5^{[1]} V_{DC}$	1	-	1	-	-	1	1	-	-	$V_L = V_{AC} - V_{C1}$	+	0
				-	-	1	1	-	-	1	-	$V_L = V_{AC} - V_{C2}$	0	+
Inverter ( $I_{k0}$ )	Positive	$ V_{Acl}  0.5^{[1]} V_{DC}$	1	1	1	-	-	-	-	1	-	$V_L = V_{C1} - V_{AC}$	-	0
				-	1	-	-	-	-	1	1	$V_L = V_{C2} - V_{AC}$	0	-
		$ V_{Acl}  0.5^{[1]} V_{DC}$	0	-	1	-	-	-	-	1	1	$V_L = V_{C2} - V_{AC}$	0	-
				1	1	-	-	-	-	1	-	$V_L = V_{C1} - V_{AC}$	-	0
	Negative	$ V_{Acl}  0.5^{[1]} V_{DC}$	1	-	-	1	1	-	1	-	-	$V_L = V_{C2} + V_{AC}$	0	-
				-	-	1	-	1	1	-	-	$V_L = V_{C1} + V_{AC}$	-	0
		$ V_{Acl}  0.5^{[2]} V_{DC}$	0	-	-	1	1	1	1	-	-	$V_L = V_{C1} + V_{AC}$	-	0
				-	-	1	1	-	1	-	-	$V_L = V_{C2} + V_{AC}$	0	-

At last, the commutated DC voltage should be defined. It is implemented with two variable components that defines conditions, when single capacitor voltage ( $v_{DC,k}$ ) and full DC voltage ( $v_{DC,k}$ ) is commutated at AC-side of MLC. It is defined as

$$v_{DC2}^{d=1,k} = v_{C\_main,k} \cdot (-gtz(I_M) \cdot LVL_k + gtz(-I_M) \cdot (1 - LVL_k)), \quad (19)$$

$$v_{DC2}^{d=0,k} = v_{C\_main,k} \cdot (-gtz(I_M) \cdot (1 - LVL_k) + gtz(-I_M) \cdot LVL_k), \quad (20)$$

$$v_{DC,k}^{d=1} = v_{DC,k} \cdot gtz(-I_M) \cdot LVL_k, \quad (21)$$

$$v_{DC,k}^{d=0} = -v_{DC,k} \cdot gtz(I_M) \cdot LVL_k. \quad (22)$$

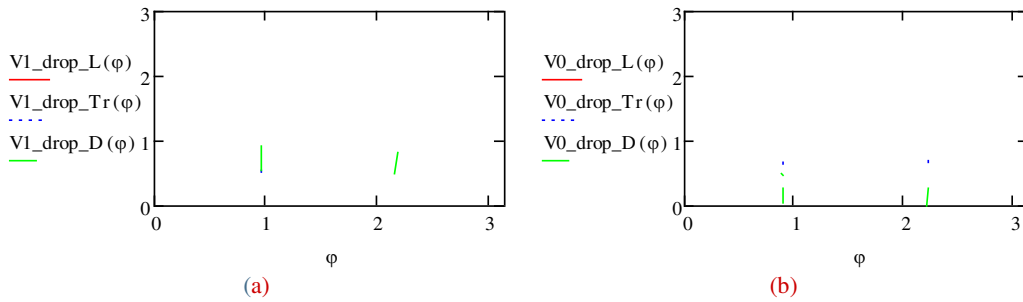
Having defined these functions, the final inductor's voltage during active and freewheeling state can be defined with two functions below

$$v_{L,k}^{d=1} = \text{sign}(v_{AC,k}) \cdot \text{sign}(I_M) \cdot v_{AC,k}^{d=1} - N_{D,k}^{d=1} \cdot V_{FD} - |i_{ref,k}| \cdot (r_L^{d=1} N_{FS,k} + I_{D,k}^{d=1} r_D), \quad (23)$$

$$v_{L,k}^{d=0} = \text{sign}(v_{AC,k}) \cdot \text{sign}(I_M) \cdot v_{AC,k}^{d=0} - N_{D,k}^{d=0} \cdot V_{FD} - |i_{ref,k}| \cdot (r_L^{d=0} N_{FS,k} + I_{D,k}^{d=0} r_D). \quad (24)$$

where  $V_{FD}$  and  $r_D$  are forward voltage and dynamic resistance of diode's equivalent model respectively;  $r_{DS}$  is MOSFET's on-state resistance;  $r_L$  is inductor's parasitic active resistance.

Defined equations allow easily tracking variable voltage drop caused by parasitic circuit elements that is demonstrated in the Figure 5.



**Figure 5.** Graphical representation of voltage drop caused by different parasitic components: inductor ( $V_{x\_drop\_L}$  caused by  $r_L=0.5 \, \Omega$ ), transistors ( $V_{x\_drop\_Tr}$  caused by  $r_{DS}=0.025 \, \Omega$ ) and diodes ( $V_{x\_drop\_D}$  caused by  $V_{FD}=0.5 \, V$  and  $r_D=0.012 \, \Omega$ ) at reference current amplitude  $I_M=3.5 \, A$  during (a) energy storing state ( $d(t)=1$ ) and (b) energy releasing state ( $d(t)=0$ )

#### 2.4. Capacitor voltage balancing

In normal case, the converter having two serially connected capacitors in the DC link experience voltage fluctuation during period of grid's voltage. In ideal, capacitors' voltage difference is described as follows:

$$v_{C1}(t) - v_{C2}(t) = \frac{I_M \cdot \cos(\omega t)}{C}. \quad (25)$$

This however is not perfectly match to MLC as capacitor's current direction changes during half-period of grid voltage. In order to minimize the calculation complexity, the digital controller of capacitor balancing can be implemented by sampling capacitor voltages during  $\pi/2$  and  $3\pi/2$ , where capacitor voltage crossing occurs in ideal case. The voltage difference can be used as input error for P or PI controller, that would add additional component to input current amplitude, in this way, capacitor voltage balancing is implemented. Asymmetrical input current amplitudes can generate DC component in the spectrum of the AC current that is prohibited by the standards, like IEEE Std 519-2014. Nevertheless, capacitor balancing with asymmetrical current amplitudes was utilized in some applications due to limitation of selected topology [46], [58].

Another solution is based on continuous monitoring of capacitor voltages and implementation of delta-controller that selects one of two switching options that minimizes capacitor voltage difference (defined

in Table 2). This solution is interesting due to following pros: 1) reduces thermal stress of switching components during half-period of input voltage and 2) minimizes voltage pulsations on capacitors.

Alternative function of selection single capacitor voltage (previously defined with eq.14) that should be used for capacitor balancing is defined below:

$$v_{C\_main,k} = \begin{cases} \text{if } (gtz(v_{AC,k}) \text{ xor } gtz(I_{M,k}) = 1), \text{ then } \begin{cases} gtz(v_{AC,k}) \cdot v_{C2,k} + gtz(-v_{AC,k}) \cdot v_{C1,k}, & \text{if } v_{C1,k} \geq v_{C2,k} \\ gtz(v_{AC,k}) \cdot v_{C1,k} + gtz(-v_{AC,k}) \cdot v_{C2,k}, & \text{if } v_{C1,k} < v_{C2,k} \end{cases} \\ \text{if } (gtz(v_{AC,k}) \text{ xor } gtz(I_{M,k}) = 0), \text{ then } \begin{cases} gtz(v_{AC,k}) \cdot v_{C2,k} + gtz(-v_{AC,k}) \cdot v_{C1,k}, & \text{if } v_{C2,k} \geq v_{C1,k} \\ gtz(v_{AC,k}) \cdot v_{C1,k} + gtz(-v_{AC,k}) \cdot v_{C2,k}, & \text{if } v_{C2,k} < v_{C1,k} \end{cases} \end{cases} \quad (26)$$

### 3. SIMULATION RESULTS

The simulation model was built by means of PSIM software. Simplified C Block was used to program CSC algorithm. The simulation parameters are as follows: a) grid voltage (RMS)  $V_{AC}=230$  V; b) grid frequency  $f_{AC}=50$  Hz; c) capacitor nominal voltages  $V_{C1}, V_{C2}=250$ V; d) inductance  $L=2.2$  mH; e) capacitance  $C1, C2=1$  mF; f) switching frequency  $f_{sw}=25$  kHz.

The impact of the parasitic circuit elements on the inductor current is clearly seen from the Figure 6. The figure on the left demonstrates current shape if conduction losses are not considered, where the average current deviates from the reference signal each switching cycle due to error in calculation of volt-second balance. The figure on the right demonstrates the performance of proposed duty cycle control approach with consideration of conduction losses, where  $THD_i$  is below 10%.

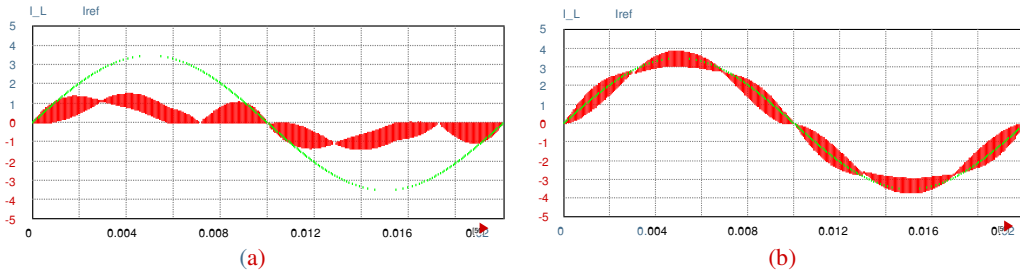


Figure 6. Simulation result of sensorless control applied to NPC MLC without (a) and with (b) consideration of conduction losses (simulation parameters:  $I_M=3.5$  A)

Demonstration of two capacitors' voltage balancing approaches is seen in the Figure 7. The current drawn from the grid is identical, while pulsations of capacitor voltages were decreased from 11 V to less than 4 V.

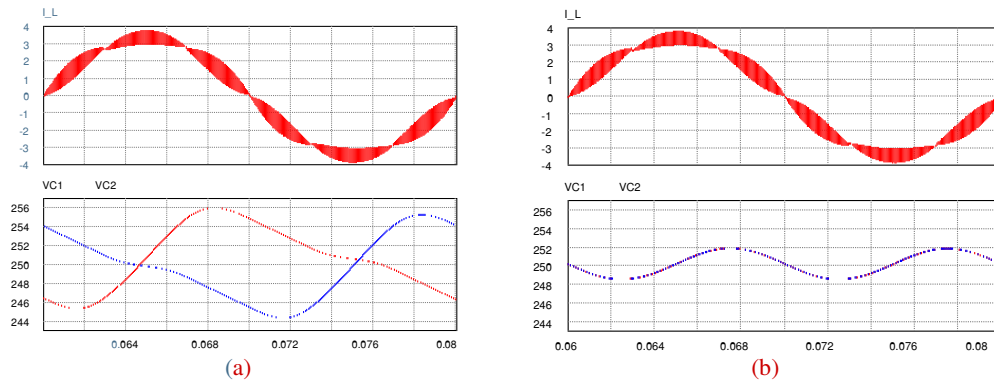


Figure 7. Simulation results of two capacitor voltage balancing approaches – (a) semi-period modification current amplitude and (b) delta-controller that selects alternative capacitor according to equation 26.

The simulation of step response was performed in order to evaluate transient responses of the proposed CSC. The controller consisted of single control loop with voltage feedback from DC voltage and reference signal of 500 V. It was based on PI controller with Notch filter, responsible for filtering out 100 Hz capacitor voltage pulsations. The current source was added to DC side that was sourcing 1 A, at 0.4 s changed to sinking of 1 A, and at 0.6 s changed back to sourcing of 1 A. The simulation results are presented in the Figure 8. The current was in phase with grid voltage before and after transient. The DC voltage overshoot was 30 V and transient time for voltage stabilisation was 150 ms that is comparable performance to similar control approaches implemented by other researchers [48], [52], [59], [60].

The Figure 9 demonstrate the performance of CSC at multiple points of power changing DC-side load from 500 W (consuming power) downto -500 W (sourcing power) with 100 W step each 100 ms. It can be seen that inductor current has sinusoidal shape at wide range of power with stable operation in DCM and CCM, contrary to other researches, where only CCM operation is considered and demonstrated [40], [46], [53]. The corresponding THD values are seen in the Figure 10.

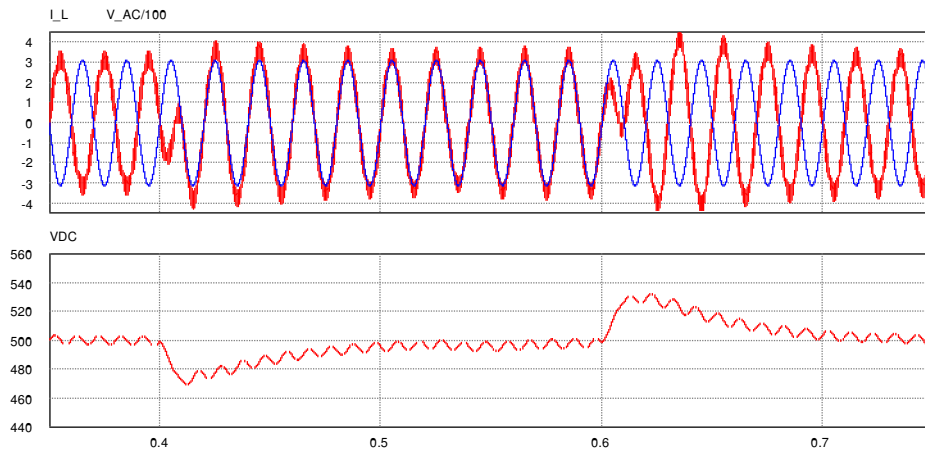


Figure 8. Simulation of step response on changing the power flow: at 0.4 s schematic changed to sinking of 500 W from the grid then at 0.6 s changed back to sourcing of 500 W to the grid (top figure scales: 1 A/div, 100 V/div; bottom figure scale: 20 V/div)

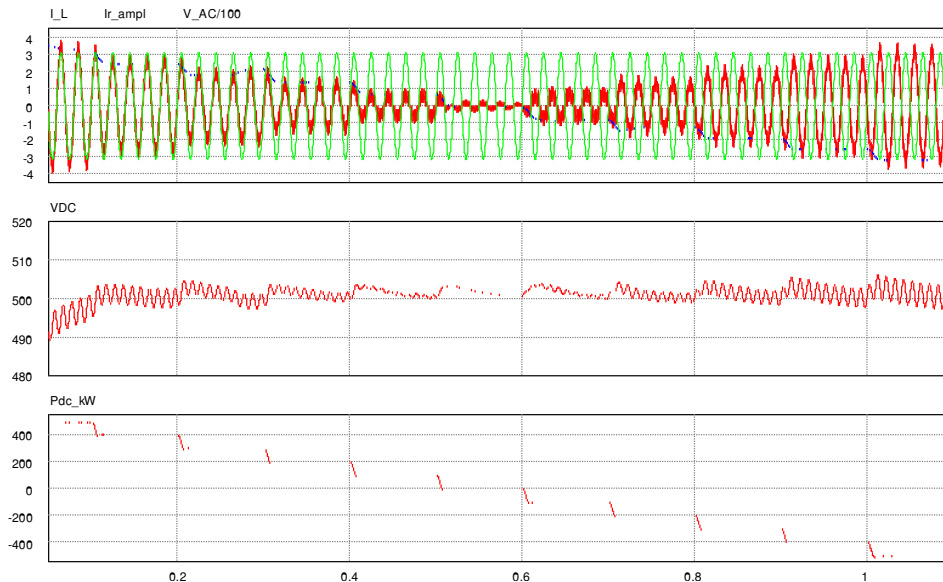


Figure 9. Simulation of step-response changing DC-side power from 500 W downto -500 W with 100 W step each 100 ms

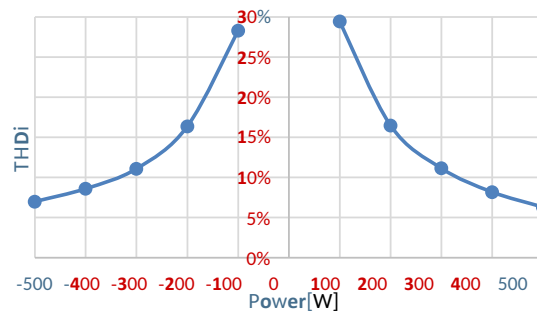


Figure 10. THD vs converter's DC power

## CONCLUSIONS AND DISCUSSIONS

The current sensorless control allows shaping inductor's current without feedback from the current sensor. The precise volt-second balance is calculated by means of digital control system taking into account grid's and both capacitors' voltages and major parasitic elements of the power circuit components. As a result, the current shape has acceptable THD and features stable sinusoidal current shape at wide range of input power.

The balancing of capacitor voltages is implemented by means of delta-controller that rapidly selects main or alternative capacitor for charging/discharging depending on converter mode (rectifier/inverter), polarity of input voltage and capacitor voltage mismatch. This is effective solution for voltage balancing and it is trivial for implementation in digital form. This type of controller minimizes the fluctuation of DC link capacitor voltages and eliminates the need of asymmetrical grid's current shape.

The practical implementation of CSC is useful for switched mode power supply engineers due to following facts:

- miniaturization of control system due to elimination of galvanically isolated current sensor;
- seamless sensorless detection of DCM and CCM by means of digital control system selecting minimal value from two duty ratios calculated for DCM and CCM operation;
- stable current shape in DCM due to precise calculation of volt-second balance applied to inductor, that is important in applications where light load operation is considered;
- immunity from distorted grid's voltage as current reference can be generated from internal pure sinusoidal signal.

Nevertheless, the implementation of CSC method has also some challenges that could be addressed in the future researches:

- dependency on precise voltage measurements and nominals of all parasitic elements;
- temperature drift of component nominals and non-linearity of circuit components are difficult to implement in converter's mathematical model. However, partially it could be solved by means of observing of the capacitor voltage pulsation during converter operation and adjustment of nominals of schematic components used for calculations;
- requirement for high computational resources as duty ratio should be calculated before each switching cycle. It means that all ADC values should be acquired and processed within previous switching cycle that involves multiple division operations and calculation of square root;
- CSC features accumulation of current error during CCM operation that has negative effect on current shape;

The authors also think of hybrid implementation of sensed and sensorless current control techniques, taking the best from both, that is a matter of another research.

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