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Small-Signal AC Model and Closed Loop Control of Interleaved Three-Phase Boost Converter

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ABSTRACT

Renewable energy sources are increasingly being used today and solar energy is the most readily and abundantly available energy source. Boost converters are an integral part of any solar energy system. In order to obtain maximum possible energy from the solar system multi-phase interleaved boost converters are used. This paper presents the small-signal ac modelling and closed loop control of three-phase interleaved boost converter. State–space modelling methodology has been adopted to have linearized equivalent model of the boost converter. The interleaved three-phase boost converter is averaged over its one switching period and perturbed with small ac variations and finally linearized around its quiescent point to have a small signal ac model. Type III compensator is employed to improve the frequency response and closed loop control of three-phase boost converter. The controller design procedure is discussed in detail. The effect of right-half plane zero in non-minimum phase system and the appropriate pole-zero placements to overcome the maximum phase lag in such system is discussed. The compensated closed loop system is tested for load variations to observe the transient response.

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1. INTRODUCTION

DC to DC converters are widely used in photo voltaic systems as a power interface. Rather than conventional boost converters, multiphase boost converters are preferred since they offer several advantages that are very desirable in low voltage and high power applications. First, several parallel power stages are added in parallel to the conventional dc-dc converter to attain multi-phase boost [1], [9]; it increases the power rating and current handling capability of the converter. Second, due to interleaved switching scheme, effective pulse frequency is increased by number of phase times and it also reduces the magnitude of inductor ripple current flowing into the filter capacitor, thereby reducing the size of the filter [2], [5].

Most of the dc-dc converter application systems demand its output to be held constant, in spite of variations in input or load [3]. It can be achieved by designing a control circuit that changes the duty cycle ratio, so as to maintain the output voltage constant and is equal to the desired reference voltage. In addition to regulating the output voltage, the feedback system should be stable, and the transient response should meet the desired specifications.Thus, the foremost objective of a typical DC-DC converter is to maintain its output voltage constant, in spite of disturbance in input voltage, load current and any parasitic effect of circuit elements. So, it is utmost important to adjust the duty cycle to keep output voltage constant .The negative feedback control technique is adopted to feed the sensed output voltage to the controller which in turn varies the duty cycle to regulate the output voltage. [3].

Many design procedures in the literature are empirically derived, its derivation process and descriptions are not provided. Thus, for a given system it is difficult to follow and evaluate these procedures [4], [7]. In this paper type III compensator is mathematically analyzed and employed. A linear control technique can be applied to a linear system, but all the switch mode power supply systems are non-linear as the system during one switching sub-interval is not the same as in other sub-interval. So, the power converter system needs to be modeled to a linear system in order to apply a linear control technique. The objective of the small signal ac modeling is to predict how small signal low-frequency ac variations in duty cycle results in small signal low frequency ac variations in the converter voltage and current waveforms.

Interleaved boost converters are now extensively used for wide range of applications. Benefits of multidevice interleaved converters over conventional converters for fuel cell applications is discussed in [10]. A PV fed interleaved boost converter is proposed for agricultural applications in [11]. Small signal model for n phase interleaved boost converter is presented in [12]. Only open loop control studies are performed. The small signal ac converter model is obtained by removing switching harmonics and averaging all sub-interval waveforms over one switching period .An averaged model implies the disappearance of any switching event to the benefit of a smoothly varying continuous signal. The averaged voltages and currents, in general comprises nonlinear functions of the converter duty cycle, voltages, and currents and results in a system of nonlinear differential equations [4]. Hence, it must be linearized to construct a small-signal linear converter model and is discussed in general in section 2.

2. STATE SPACE AVERAGE MODEL

It is a common practice to select state variables based on energy storage elements [6]. Unlike conventional dc-dc converter which has two states during each switching period, due to interleaved switching sequence of multi-Phased converter, it undergoes various different states, depending on the number of phase. The duration of each state is derived with relative to its duty ratio and the switching period. In three-phase dc-dc converter, the different phase switches are operated with relative phase shifts of 120 degree [13].

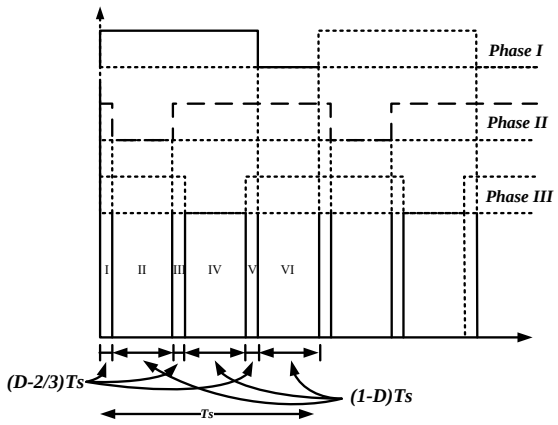

Figure 1. Three-Phase Interleaved switching pulse

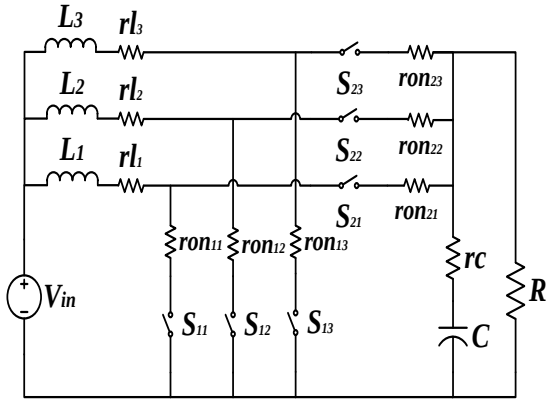

Figure 2. Three-Phase boost converter

The gate pulse for interleaved three-phase dc-dc converter is shown Figure.1. Due to interleaved switching, the three-phase system exhibits six states in each switching cycle. The states I, III and V lasts for (D – 2/3), while states II, IV, and VI lasts for (1-D) times the switching period T_s [13].

For a three-phase dc-dc converter shown in Figure 2, operating in continuous conduction mode, operating states form the state vector x(t), and the independent sources that drive the converter form the input vector u(t). During each subinterval of a switching period, the converter reduces to the linear circuit that can be represented by the following state equations as,

$$\frac{dx(t)}{d(t)} = A_n x(t) + B_n u(t) \quad (1)$$

$$y(t) = C_n x(t) + E_n u(t) \quad (2)$$

During each of the subintervals, the circuit configuration is different and represent different linear circuits; hence, the corresponding state equation matrices may also differ. These state equations are used to obtain small-signal ac model [2], [6].
Since the switching frequency of the converter is generally very much greater than the converter input frequency variations , the equilibrium state equations of the converter is given as,

$$0 = AX + BU \tag{3}$$

$$Y = CX + DU \tag{4}$$

$$\text{Where, } A = (A_1 + A_3 + A_5)\left(D - \frac{2}{3}\right) \ldots + (A_2 + A_4 + A_6)(1 - D) \tag{5}$$

$$B = (B_1 + B_3 + B_5)\left(D - \frac{2}{3}\right) \ldots + (B_2 + B_4 + B_6)(1 - D) \tag{6}$$

$$C = (C_1 + C_3 + C_5)\left(D - \frac{2}{3}\right) \ldots + (C_2 + C_4 + C_6)(1 - D) \tag{7}$$

$$E = (E_1 + E_3 + E_5)\left(D - \frac{2}{3}\right) \ldots + (E_2 + E_4 + E_6)(1 - D) \tag{8}$$

Here X, U and Y represent the state, input and output vectors respectively and D is the duty cycle. By perturbation and linearization of the converter waveforms around its quiescent operating point [2], [14], the state equation of the small signal ac model is given as,

$$\frac{dx(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + M\hat{d}(t) \tag{9}$$

$$\hat{y}(t) = C\hat{x}(t) + N\hat{d}(t) \tag{10}$$

where $\hat{u}$ (t) and $\hat{d}(t)$ represent small changes in the input vector and duty ratio. The vector $\hat{x}(t)$ and $\hat{y}(t)$ are the resulting small deviations in the state and output vector. Here it is assumed that, in comparision with the quiescent values, these deviations are much less [2].The matrices M and N are given as

$$M = \big((A_1 + A_3 + A_5) - (A_2 + A_4 + A_6)\big)X \ldots + \big((B_1 + B_3 + B_5) - (B_2 + B_4 + B_6)\big)U \tag{11}$$

$$= \big((C_1 + C_3 + C_5) - (C_2 + C_4 + C_6)\big)X \ldots + \big((E_1 + E_3 + E_5) - (E_2 + E_4 + E_6)\big)U \tag{12}$$

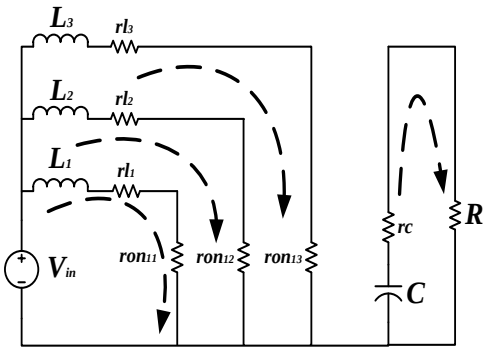

Figure 3 (a) State I, III and V

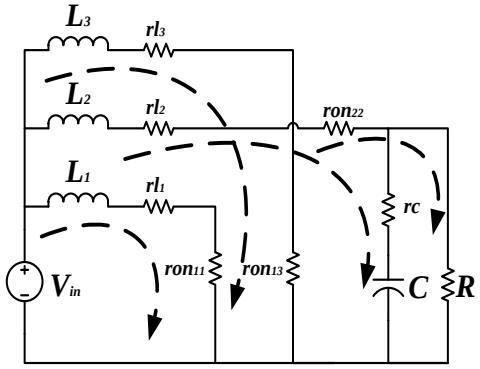

Figure 3 (b) State II

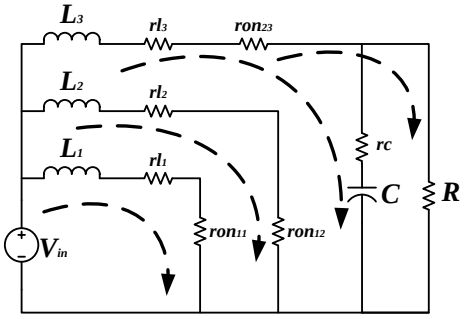

Figure 3 (c) State IV

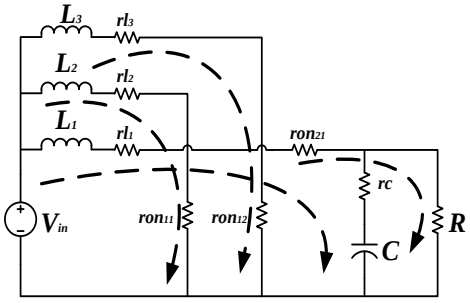

Figure 3 (d) State VI

2.1 Small Signal ac modelling of Three-Phase Boost Converter

Figure.2 shows a Three-Phase boost converter with synchronous switching. Very low voltage drop across the MOSFETs compared to diodes, resulting in higher efficiency is the prime advantage of synchronous switching dc-dc converter [14]. The conduction losses of the MOSFETs are modeled by on-resistance r_{on}, the dc resistance of the inductor as r_l and equivalent series resistance of the capacitor as r_c. The inductor current and capacitor voltage being independent states of the converter comprise the state vector.
The input voltage $V_{in}(t)$ being independent source comprise the input vector as,

$$x(t) = [i_{L1}(t)\ i_{L2}(t)\ i_{L3}(t)\ V_c(t)]' \quad (13)$$

$$u(t) = [V_{in}(t)] \quad (14)$$

The output vector is formed by the output port voltage variable $V_o(t)$

$$y(t) = [v_o(t)] \quad (15)$$

In order to have state equations for each subinterval, the circuit is analyzed for six different states during its switching period.

2.1.1 State I:

All the three low side switches S_{11}, S_{12} and S_{13} are closed, while its complementary switches S_{21}, S_{22} and S_{23} are let open..The reduced linear circuit is shown in Figure 3 (a)
The state equations for inductor voltage,

$$L_1 \frac{di_{L1}(t)}{dt} = V_{in}(t) - i_{L1}(t)(rl_1 + ron_{11}) \quad (16)$$

$$L_2 \frac{di_{L2}(t)}{dt} = V_{in}(t) - i_{L2}(t)(rl_2 + ron_{12}) \quad (17)$$

$$L_3 \frac{di_{L3}(t)}{dt} = V_{in}(t) - i_{L3}(t)(rl_3 + ron_{13}) \quad (18)$$

Capacitor current, $C\frac{dv_c(t)}{dt} = -\left(\frac{v_c(t)}{R+rc}\right)$ (19)

and Output voltage,

$$v_o(t) = \left(\frac{v_c(t)R}{R+rc}\right) \quad (20)$$

2.1.2 State II:

The low side switch S_{12} is turned OFF; while it's complementary S_{22} is turned ON. Thus the stored energy in inductor L_2 is freewheeled through switch S_{22} .Thus, the reduced linear circuit is shown in Figure 3 (b) The phase I and phase III continues to store energy, thus the phase II inductor voltage is given as,

$$\frac{di_{L2}(t)}{dt} = V_{in}(t) - i_{L2}(t)\left(rl_2 + + \frac{Rrc}{R+rc}\right) \ldots - \frac{v_c(t)R}{R+rc} \quad (21)$$

Capacitor current, $C\frac{dv_c(t)}{dt} = \frac{i_{L2}(t)R}{R+rc} - \frac{v_c(t)}{R+rc}$ (22)

Output voltage, $v_o = \left(\frac{Rrc}{R+rc}\right) i_{L2}(t) + \left(\frac{R}{R+rc}\right) v_c(t)$ (23)

2.1.3 State III: State III is similar to state I, where all the low side switches are closed and the inductors store energy.

2.1.4 State IV:

Complementary S_{23} is turned ON. Thus the stored energy in inductor L_3 is freewheeled through switch S_{23}. The reduced linear circuit is shown in Figure 3 (c). Thus the phase III inductor voltage is given as,

$$L_3\frac{di_{L3}(t)}{dt} = V_{in}(t) - i_{L3}(t)\left(rl_3 + ron_{23} + \frac{Rrc}{R+rc}\right) \ldots - \frac{v_c(t)R}{R+rc} \quad (24)$$

Capacitor current, $C\frac{dv_c(t)}{dt} = \frac{i_{L3}(t)R}{R+rc} - \frac{v_c(t)}{R+rc}$ (25)

Output voltage, $v_o = \left(\frac{Rrc}{R+rc}\right) i_{L3}(t) + \left(\frac{R}{R+rc}\right) v_c(t)$ (26)

2.1.5 State V*: S*tate V is similar to state I, where all the low side switches are closed and the inductors store energy.

2.1.6 State VI*:*

The low side switch S_{11} is turned OFF; while it's complementary S_{21} is turned ON. Thus the stored energy in inductor L_1 is freewheeled through switch S_{11}. The reduced linear circuit is shown Figure 3 (d). Thus the phase I inductor voltage is given as,

$$\frac{di_{L1}(t)}{dt} = V_{in}(t) - i_{L1}(t)\left(rl_1 + ron_{21} + \frac{Rrc}{R+rc}\right) \ldots - \frac{v_c(t)R}{R+rc} \quad (27)$$

Capacitor current,

$$C\frac{dv_c(t)}{dt} = \frac{i_{L1}(t)R}{R+rc} - \frac{v_c(t)}{R+rc} \quad (28)$$

Output voltage, $v_o = \left(\frac{Rrc}{R+rc}\right) i_{L1}(t) + \left(\frac{R}{R+rc}\right) v_c(t)$ (29)

The six state matrices, input vectors and output vectors are identified and evaluated for state-space averaged equations [2]. The approximations considered here are, all the three phase inductance is same and its rating too, thus its dc resistance is approximately equal to each other, and can be given as r_l. Similarly, all the same rated MOSFET's on-resistance is approximated to r_{on} and let $rl + ron = rl'$.

Also, $R + rc = R$ as $R >> rc$

Thus, using (5) and (16) to (29) the Averaged matrix A, is given by

$$\begin{bmatrix} -\left(\frac{rl' + rc\acute{D}}{L_1}\right) & 0 & 0 & -\frac{\acute{D}}{L_1} \\ 0 & -\left(\frac{rl' + rc\acute{D}}{L_2}\right) & 0 & -\frac{\acute{D}}{L_2} \\ 0 & 0 & -\left(\frac{rl' + rc\acute{D}}{L_3}\right) & -\frac{\acute{D}}{L_3} \\ \frac{\acute{D}}{C} & \frac{\acute{D}}{C} & \frac{\acute{D}}{C} & -\frac{1}{CR} \end{bmatrix} \quad (30)$$

Similarly, using (6), (7) and (16) to (29) the averaged matrix B and C,

$$B = \begin{bmatrix} 1/L_1 \\ 1/L_2 \\ 1/L_3 \\ 0 \end{bmatrix} \quad (31)$$

$$C = [Ḋrc \quad Ḋrc \quad Ḋrc \quad 1] \quad (32)$$

Using (11) and (12), vector coefficient of $\hat{d}(t)$ is given as,

$$M = \left[\frac{V_{in}}{L_1 D} \quad \frac{V_{in}}{L_2 D} \quad \frac{V_{in}}{L_3 D} \quad \frac{-V_{in}}{CRD^2}\right]' \quad (33)$$

$$N = \left[\frac{-V_{in}rc}{RḊ^2}\right] \quad (34)$$

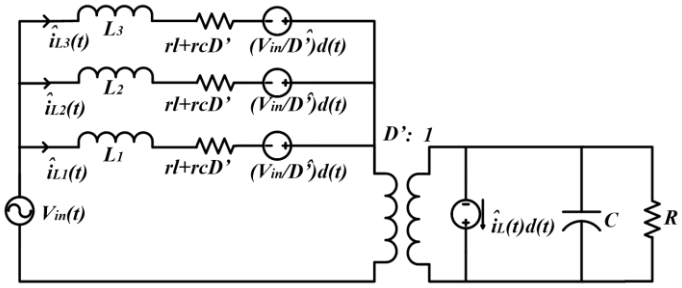

Figure 4. Small-signal ac model of Three-Phase boost converter

The small signal ac equations are obtained by perturbation with small ac variation and linearization with removal of DC terms and higher order terms [2], [14]. Thus, small-signal model is found by evaluation of (9), (10). When written in scalar form, the three-phase inductor voltages are given as,

$$L_1 \frac{d\hat{i}_{L1}(t)}{dt} = \hat{v}_{in}(t) - \hat{i}_{L1}(t)(rl' + rcḊ) - \hat{v}_c(t)Ḋ \ldots + \left(\frac{V_{in}}{Ḋ}\right)\hat{d}(t) \quad (35)$$

$$L_2 \frac{d\hat{i}_{L2}(t)}{dt} = \hat{v}_{in}(t) - \hat{i}_{L2}(t)(rl' + rcḊ) - \hat{v}_c(t)Ḋ \ldots + \left(\frac{V_{in}}{Ḋ}\right)\hat{d}(t) \quad (36)$$

$$L_3 \frac{d\hat{i}_{L3}(t)}{dt} = \hat{v}_{in}(t) - \hat{i}_{L3}(t)(rl' + rcḊ) - \hat{v}_c(t)Ḋ \ldots + \left(\frac{V_{in}}{Ḋ}\right)\hat{d}(t) \quad (37)$$

The capacitor current is given as,

$$C\frac{d\hat{v}_c(t)}{dt} = \hat{i}_{L1}(t)Ḋ + \hat{i}_{L2}(t)Ḋ + \hat{i}_{L3}(t)Ḋ - \frac{\hat{v}_c(t)}{R} \ldots - \left(\frac{\hat{v}_{in}}{RḊ^2}\right)\hat{d}(t) \quad (38)$$

The output equation,

$$\hat{v}_o(t) = (\hat{i}_{L1}(t) + \hat{i}_{L2}(t) + \hat{i}_{L3}(t))Ḋrc - \hat{v}_c(t) \ldots - \left(\frac{\hat{v}_{in}rc}{RḊ^2}\right)\hat{d}(t) \quad (39)$$

Circuits corresponding to equations (35) – ((39) are combined into a complete small-signal ac equivalent circuit model of non-ideal three-phase boost converter as shown in Figure 4. This will aid in frequency response based control system design.

2.2 Closed loop control of three phase boost converter

Open loop characteristics is essential to analyse the performance and stability of the control system that regulates the converter output voltage. The necessary transfer function is obtained by making the line voltage variation û(s) zero and then solving for the transfer function from $\hat{d}(s)$ to $\hat{v}_o(s)$ [2], [14]. Thus,

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = C(SI - A)^{-1}M + N \tag{40}$$

$$\frac{\hat{v}_o}{\hat{d}} = G_{do}\left(\frac{\left(1+\frac{s}{\omega_{esr}}\right)\left(1-\frac{s}{\omega_{rhp}}\right)}{\left(1+\frac{s}{Q\omega_o}+\frac{s^2}{{\omega_o}^2}\right)}\right) \tag{41}$$

Where,

DC gain is given by, $G_{do} = V_g\left(\frac{3R(3RD'^2 - rl')}{(3RD'^2 + rl')(3RD' + D'rc + rl')}\right)$

$$\omega_o = \sqrt{\left(\frac{3RD'^2 + D'rc + rl'}{CLR}\right)};\quad Q = \omega_o\left(\frac{1}{\frac{1}{CR} + \frac{D'rc + rl'}{L}}\right);$$

$$\omega_{rhp} = 1 - \frac{s}{\left(\frac{3D'^2R - (rl')}{L}\right)};\quad \omega_{esr} = 1 + \left(\frac{s}{1/Crc}\right)$$

The three-phase boost converter in its voltage mode control will have four main characteristics, a double pole due to LC filter which moves with operating conditions, an ESR zero due to equivalent series resistance of output capacitor, Right half plane zero and finally a variable gain dependent upon the input voltage of the converter [2].

Closed loop control systems are usually associated with stability and response time issues which may conditionally affect the output; even though control loop allows the converter to adjust to load variations or changes in the input voltage [10]. For compensated system, high DC gain ensures that the steady-state error between the output and the reference signal is small [4], [5]. Enough phase margin and bandwidth ensures satisfactory stability margin and transient response [4], [14].

2.2.1 Right half plane zero

A three-phase boost converter in voltage mode control will have an additional zero in the right half. With right half zero, it is a challenging design task to stabilize converter when operating with voltage mode control [5], [9]. RHP zero is introduced when the duty ratio is increased (low-side switch is of boost converter is switched on for a longer duration). The output initially reduces, in spite of the control command trying to increase it. This in fact is the characteristics of a zero in the right half; a rise in the control command to the system results in an initial reduction in the output response. After about 4 to 5 times the time constant associated with the right half zero, the output follows the input control command. Hence in a system with a RHP zero, the control system will take a certain time to respond to any changes in the output; response is not immediate [5]. In order to overcome this problem and to stabilize the system, the loop bandwidth must be much less than the frequency of the right half zero [7], [3].

3. RESULTS AND DISCUSSION

3.1 Type III Compensator Design Procedure

Type III compensator has a phase angle 90° at some frequencies. Required phase boost is therefore available to attain the desired phase margin. Figure 5 shows a closed loop three-phase boost converter with type III compensator in its feedback path. A type III compensator will have two zeros and three poles, with a pole at the origin [3]. Here, it is intended to place zeros coincident, one pole at origin and the remaining poles coincident to each other. Thus equation (42) gives the desired transfer function.

$$C(s) = \frac{K\left(1+\frac{s}{\omega_Z}\right)^2}{s\left(1+\frac{s}{\omega_P}\right)^2} \tag{42}$$

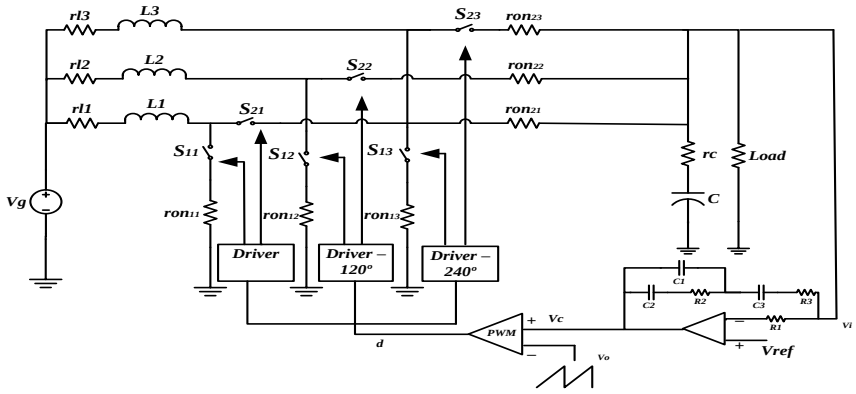

Figure 5. Closed loop voltage mode controlled three-phase boost converter

From (42), at any frequency ω, the amplitude and phase of the transfer function are given by (43) and (44) respectively and (44) is rewritten as (45).

$$C(j\omega) = \frac{K}{\omega}\frac{\left|\left(1+j\frac{\omega}{\omega_z}\right)^2\right|}{\left|\left(1+j\frac{\omega}{\omega_P}\right)^2\right|} = \frac{K}{\omega}\frac{1+\left(\frac{\omega}{\omega_z}\right)^2}{1+\left(\frac{\omega}{\omega_P}\right)^2} \quad (43)$$

$$\varphi[C(j\omega)] = \varphi\left(\frac{K}{j\omega}\right) + \varphi\left(1+\frac{j\omega}{\omega_z}\right)^2 - \varphi\left(1+\frac{j\omega}{\omega_P}\right)^2 \quad (44)$$

$$\varphi[C(j\omega)] = -\frac{\pi}{2} + 2\varphi\left(1+j\frac{\omega}{\omega_z}\right) - 2\varphi\left(1+j\frac{\omega}{\omega_P}\right) \quad (45)$$

From (45), the phase of C (jω) comprise of a constant value of – π /2 due to the pole at the origin, and a variable portion as a function of frequency ω,

$$\varphi_v(j\omega) = 2\tan^{-1}\frac{\omega(\omega_P-\omega_z)}{\omega^2+\omega_z\omega_P} \quad (46)$$

At the geometric mean of the ω_z and ω_p the maximum variable phase angle occurs and is given as,

$$\omega_m = \sqrt{\omega_P\omega_z} \quad (47)$$

Here, let ω_m be the maximum phase frequency of a type III compensator.
Let $k = \frac{\omega_P}{\omega_z}$ (48)

Then the maximum phase of $\varphi_v(\omega)$ can be written as,

$$\varphi_v(\omega_m) = 2\tan^{-1}\left(\frac{k-1}{2\sqrt{k}}\right) \quad (49)$$

Finally, the maximum phase of the type III compensator is given as,

$$\varphi[C(j\omega_m)] = -\frac{\pi}{2} + 2\tan^{-1}\left(\frac{k-1}{2\sqrt{k}}\right) \quad (50)$$

Here, 'k' is a measure of the separation between the zero and pole frequency. Due to RHP zero in the boost converter, it is non-minimum phase system, because of which extra phase lag is added to the system and it makes the system conditionally stable. Due to RHP zero, the system's phase plot goes below -180º, (more negative), but comes back again to -180º. Thus, it is required to have a phase boost at maximum phase lag frequency ω_{mp} [3]. Also, to attain desired phase margin and for loop stability, phase boost is necessary at the crossover frequency too. Thus the maximum phase boost frequency ω_m by type III compensator is required to be placed somewhere between ω_{mp} and ω_c [3]. The ω_m is given by,

$$\omega_m = \alpha\sqrt{\omega_{mp}\omega_c} \tag{51}$$

In order to attain the desired phase margin and bandwidth, α need to be adjusted. Thus, by adjusting the 'α' on trial and error basis, unconditional stability can be achieved. Once the ω_m is selected for the given system, and provided the ω_m, G_p, ω_{mp} and φ_p are noted. Using (50) and (46), it can be written as,

$$2\tan^{-1}\left(\frac{\omega_c(\omega_p-\omega_z)}{{\omega_c}^2+\omega_z\omega_p}\right)=\varphi_m-\varphi_p-\frac{\pi}{2} \tag{52}$$

$$\frac{\omega_c(\omega_p-\omega_z)}{{\omega_c}^2+\omega_p\omega_z}=\tan\left(\frac{\varphi_m-\varphi_p}{2}-\frac{\pi}{4}\right) \tag{53}$$

Based on (52) and (53), the following two equations are obtained,

$$\omega_p\omega_z={\omega_m}^2 \tag{54}$$

$$\omega_p-\omega_z=\omega_d \tag{55}$$

Where ω_d is defined as, $\omega_d=\tan\left(\frac{\varphi_m-\varphi_P}{2}-\frac{\pi}{4}\right)\left(\omega_d+\omega_{mp}\right)$ (56)

From (54) and (55), the compensator's zero and pole frequencies are given as,

$$\omega_z=0.5\left(\sqrt{{\omega_d}^2+{\omega_m}^2}-\omega_d\right) \tag{60}$$

$$\omega_p=0.5\left(\sqrt{{\omega_d}^2+{\omega_m}^2}+\omega_d\right) \tag{61}$$

The separation factor is be calculated as, $k=\frac{\sqrt{{\omega_d}^2+{\omega_m}^2}+\omega_d}{\sqrt{{\omega_d}^2+{\omega_m}^2}-\omega_d}$ (62)

From (50), it is known that, $|C(j\omega_c)|=\frac{K}{\omega_c}\frac{1+\left(\frac{\omega_c}{\omega_Z}\right)^2}{1+\left(\frac{\omega_c}{\omega_P}\right)^2}$ (63)

At the crossover frequency, $|C(j\omega_c)|G_P=1$ (64)

Thus, the gain K is, $K=\frac{\omega_c\left(1+\left(\frac{\omega_c}{\omega_P}\right)^2\right)}{G_P\left(1+\left(\frac{\omega_c}{\omega_z}\right)^2\right)}$ (65)

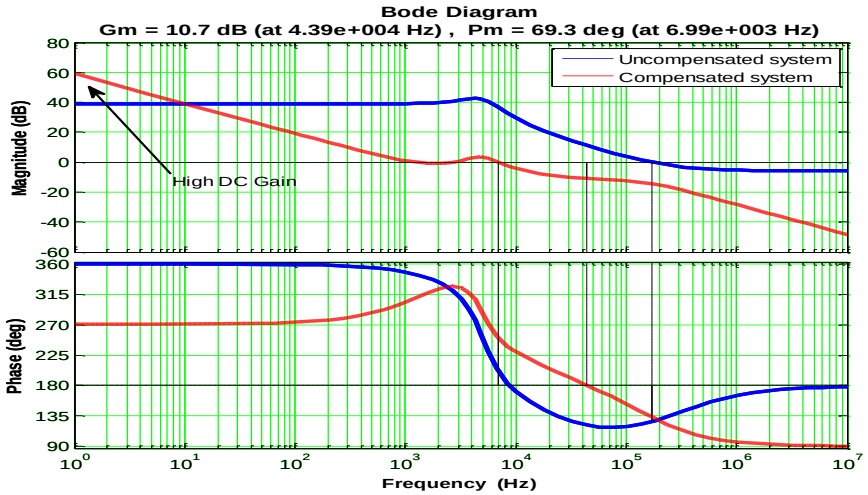

Figure 6. Frequency response of Three-Phase boost converter

3.2 Control System Design for Three-Phase Boost Converter

Design specifications of three phase boost converter is given Table.1.

Table.1. Three-Phase Boost converter design specifications

Specifications				
V_{in}		12 V		
V_{out}		40 V		
Power		700 watts		
Switching frequency		100 kHz		
Three-Phase Component details				
Phase	Inductance, DCR	Switch ON Resistance mΩ		Capacitance, ESR
I	6.08µH, 5mΩ	S_{11}	20	56µF, 10mΩ
		S_{21}	20	
II	6.08µH, 5mΩ	S_{12}	20	
		S_{22}	20	
III	6.08µH, 5mΩ	S_{13}	20	
		S_{23}	20	

3.2.1 Compensator Design

Figure 6 shows the open loop, control-to-output, uncompensated, Bode plot for three-phase boost converter. From Figure 6 the compensator can be designed by following the procedure given from (42) to (62). The crossover frequency i.e. the bandwidth of the compensated system is generally chosen to be less than one-fifth of switching frequency [2], [4]. In this case, the chosen crossover frequency is 7 kHz. The gain and the phase angle at 7 kHz are noted to aid in compensator design. From Figure 6, the gain and the phase angle at 7 kHz were found to be 36.5dB and -159° respectively and also the maximum phase lag due to RHP zero dips at 70 kHz. A phase margin of 70° ° is considered to ensure good stability and better transient response.

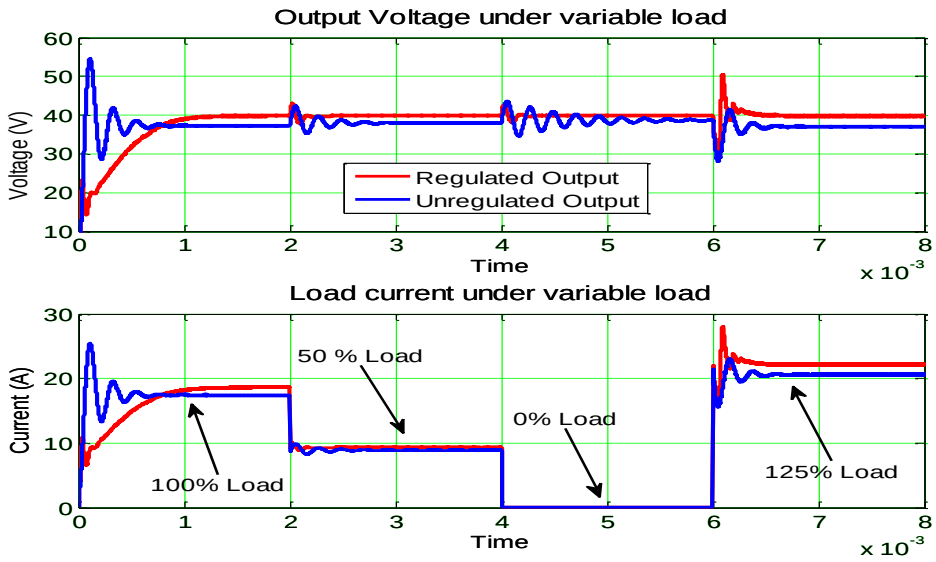

Figure 7. Transient response of Three-Phase boost converter

3.3 Discussion

The desired frequency response with high DC gain, enough bandwidth and phase margin is evident from the Fig.6. The complete closed loop compensated system is tested for instant variable load to observe the transient response. Fig.7 shows the output voltage waveform for regulated and unregulated three-phase boost converter. From the Fig.7, when load is varied, the output voltage of unregulated system varies, while in the regulated system the output voltage settles back to its desired reference voltage. Thus, this type of closed loop regulated system; find its utmost application in point of load power supplies.

4. CONCLUSION

The foremost feature of the multi-phased boost converter, self-regulation of output, is easily achieved by designing a closed loop control circuit which in turn is aided by small-signal ac model of the dc-dc converter. The state-space averaging of several sub-intervals during one switching period results in accurate small-signal ac model. The designing of compensator circuit for closed loop control is aided by the frequency response of the small-signal ac model of dc-dc converter. The compensated system met desired frequency domain responses such as, high DC gain, enough bandwidth and required phase margin for unconditional stability. The difficulty in the compensation of the non-minimum phase system, due to maximum phase lag is overcome by appropriate pole-zero placement of type III compensator. The step-by-step design procedure for type III compensator leads to have an easy methodology for control system design. The closed loop regulated system is tested for variable load and compared with unregulated system. The small-signal ac modelling and closed loop control of multi-phase dc-dc converter paves the way to have an advanced design methodology for high power applications requiring tight voltage regulation.

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