

Comparative Study of Three Different Topologies of Five-level Inverter with SPWM Modulation Technique

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ABSTRACT

Multilevel Inverter (MLI) has attracted a great attention by different researchers and industries due to its capability in handling high power application and minimizing the harmonics contents in the output. This study propose three different topologies of MLI (5-level) which are Cascaded H-Bridge Multilevel Inverter (CHMLI), Diode Clamped Multilevel Inverter and Flying Capacitor Multilevel Inverter (FCMLI). These three topologies have been modelled in MATLAB/SIMULINK and compared in terms of THD and number of components used. Sinusoidal Pulse Width Modulation is utilized to control both of the topologies with same DC source. The results showed that, CHMLI is superior compared to DCMLI and FCMLI in which the CHMLI produce 26.29% THD while DCMLI and FCMLI produce 29.14% and 33.53% respectively. Moreover less components and switching losses is obtained when using the CHMLI.

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1. INTRODUCTION

Nowadays, most of researchers as well as industries are paying much attention in developing and presenting new renewable energy resources [1]-[3]. The most common renewable energy resources are solar energy [4], wind energy [5], thermal energy [6] and many other renewable resources [7]. Naturally the energy produced by the renewable energy resources is DC energy. Because of most of the home appliances as well as industrial applications operate using AC energy, the renewable DC energy generated need to be converted into AC energy. This conversion can be achieved utilizing power electronic inverter [8] which mainly designed to convert the DC energy into AC energy.

The first designed inverter is 2-level inverter which limited to low power application due to less capability and power rating [9]. In order to handle high power applications and increase the power rating of the inverter, Multilevel Inverter (MLI) was introduced [10]-[12]. The main advantages of MLI are the capability of handling high and medium industrial application [13] and minimizing the cost of filtering circuit since the MLI produce almost sinusoidal AC signal [14]. MLI can be designed as Three-level [15], five-level [16], seven-level [17] and so on [18]. The number of level is in direct relationship with output signal, where the output signal can be enhanced as the number of level increased, however high number of level require large number of components which will result in very expensive design. Recently, various researchers and industries are focusing in utilizing the MLI in drive application such as Switched Reluctance Motor (SRM) [19], Induction Motor (IM) [20] and Permanent Magnet Synchronous Motor (PMSM) [21]. The multilevel inverter produce less harmonic contents in its output voltage and current. Also the power switches in multilevel inverter experience low voltage stress and low electromagnetic interferences (EMI) [25].

MLI can be presented in different configurations depending on the arrangement of the power electronic components, the most common topologies of MLI are Cascaded H-bridge Multilevel Inverter [22], Diode Clamped Multilevel Inverter [23] and Flying Capacitor Multilevel Inverter [24]. Each MLI topology has different combinations and power electronics components arrangement. A study by Colak [10] has reviewed the MLI topologies and their control scheme in which different control schemes are investigated. The study build a good basis to distinguish between MLI topologies and their preferred control techniques. This paper, presents the analytic study between three different MLI topologies which are CHMLI, DCMLI and FCMLI with Sinusoidal Pulse Width Modulation (SPWM). The topologies are compared in terms of number of components used, harmonics reductions, switching losses and DC sources. MATLA/SIMULINK environment is utilized to design and obtain the results of the MLI topologies. The block diagram shown in Figure 1 illustrates the main concept of this study.

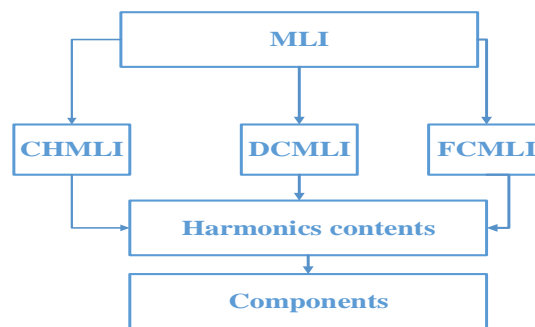


Figure 1. MLI topologies comparison block diagram

2. MLI Topologies

2.1. Cascaded H-Bridge

A cascade H-bridge multilevel inverter can be constructed by connecting a set of single full bridge inverter in series. Each bridge has its own isolated dc source which can be solar cells or batteries. These separated dc sources feeding the H-bridge multilevel inverter can generate almost sinusoidal waveform voltage. Figure 2 shows a five-level of CHMLI. Each H-bridge will be activated at certain amount of time at different start up angle and since each bridge is fed by separate dc source, the output of all the bridges which form the CHMLI output will be the sum of the the separated dc sources for three phase nth level of CHMI inverter. And the output Equation as follow [25]:

$$V_{an}=V_{a1}+V_{a2} \quad \textcircled{1}$$

$$V_{bn}=V_{b1}+V_{b2} \quad \textcircled{2}$$

$$V_{cn}=V_{c1}+V_{c2} \quad \textcircled{3}$$

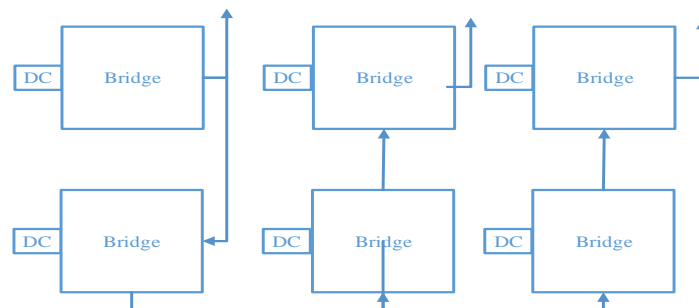


Figure 2. five level H-bridge MLI

2.2. Diode Clamped

The diode clamped inverter produce multiple outputs voltages utilizing the technique of connection of the phases to a series bank of capacitors. The first diode clamped was limited to three voltage level but nowadays the level can be extended by increasing the number of capacitor connected across the dc bus resulting in additional voltage levels. The diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage; however the number of level of multilevel inverter must be odd number because in the case of even number level, the neutral point can't be accessed [26].

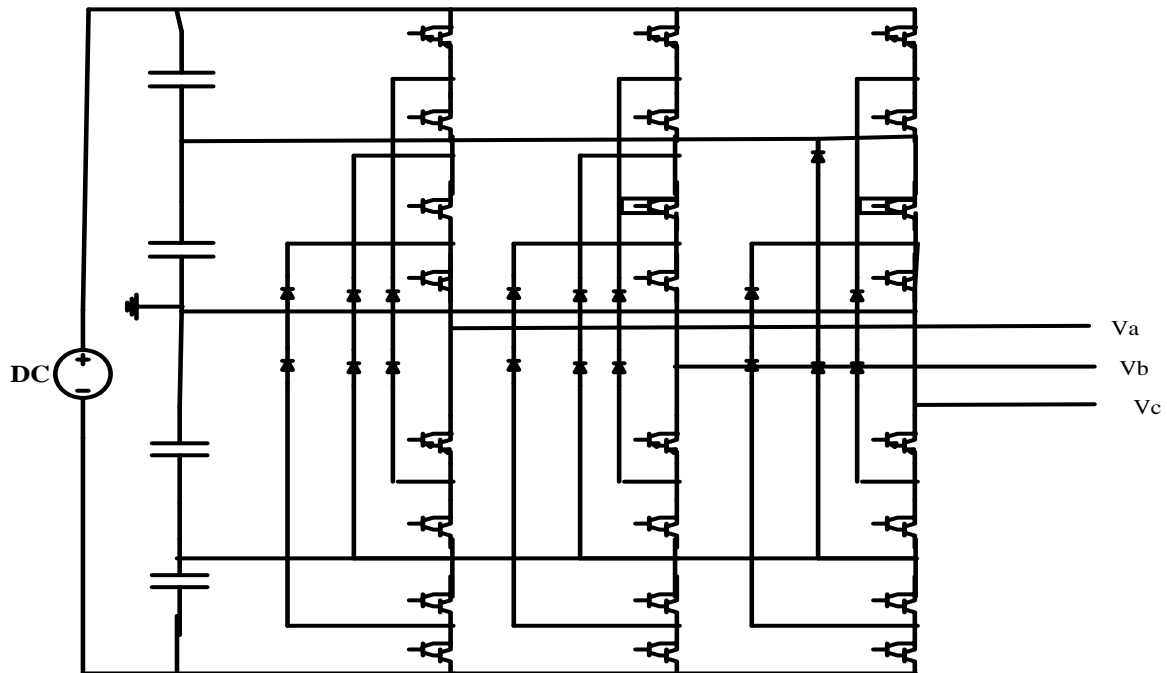


Figure 3. Five level flying capacitor MLI

2.3. Flying Capacitor

Another multilevel inverter topology is the flying capacitor which utilizes a series connection of capacitor. The main concept of this inverter is to use capacitors as clamping switching cells. The capacitors transfer the limited amount of voltage to electrical devices. This inverter use the same switching states as the diode clamping inverter but it doesn't require any clamping diode since it use capacitor instead [27]. Figure 4 shows the circuit block diagram of five-level of flying capacitor MLI.

3. SINOUSDAL PULSE WIDTH MODULATION

There are many different modulation techniques which can be applied to multilevel inverter; the most famous and simplest modulation technique is the sinusoidal pulse width modulation (SPWM). The MLI can be controlled by using the SPWM, where sinusoidal signal is compared with square waves to generate the switching pulses. These pulses will trigger the semiconductor switches in time sequence considering the phase between the phases shift of three phase inverter legs. This method uses $N-1$ level carrier signals to generate the N -level inverter output voltage. In multilevel inverter, the frequency modulation index, m_f and the amplitude modulation index, m_i are defined as [27]:

$$m_f = \frac{f_c}{f_m} \quad (8)$$

$$m_i = \frac{A_m}{A_c} \quad (9)$$

Where f_c = carrier signal frequency, f_m = reference signal frequency,
 A_c = carrier signal amplitude, A_m = reference signal amplitude.

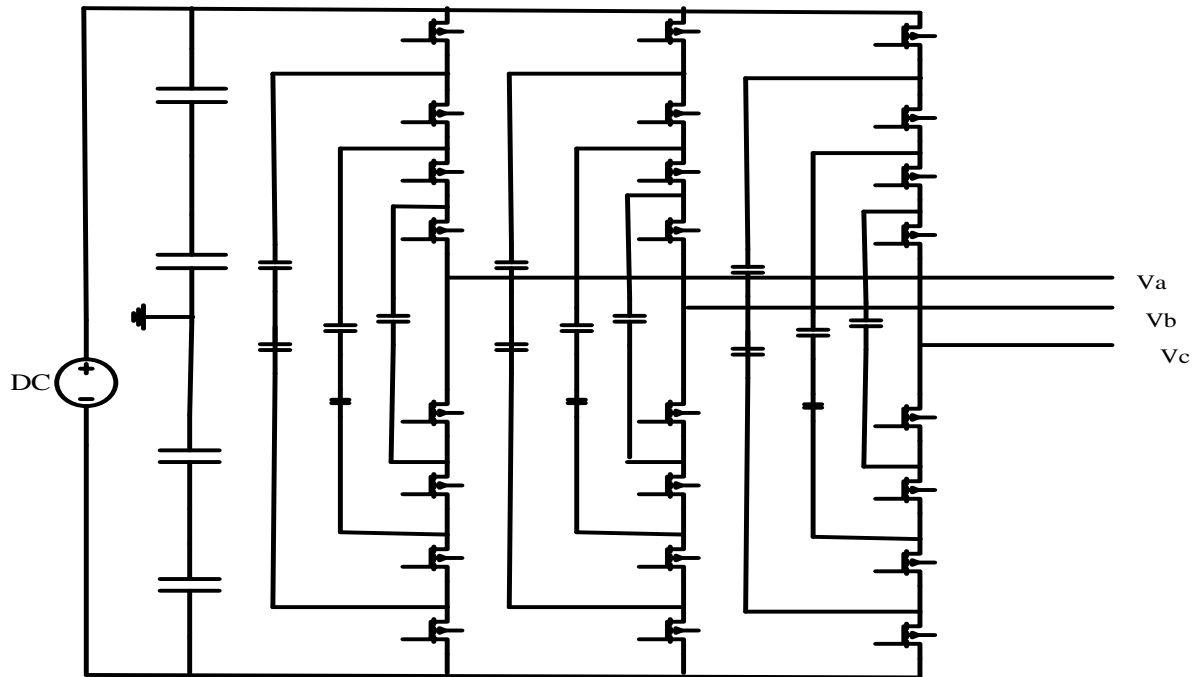


Figure 4. Five level flying capacitor MLI

In order to generate the switching pulses of 5-level inverter, the sinusoidal pulse width modulation four carrier signals are compared with one reference sine wave. Where the amplitude of the carrier signal divided into four regions to fit the reference sine wave amplitude. Figure 5 shows the SPWM carriers signal compared with reference sinusoidal signal for 5-level inverter.

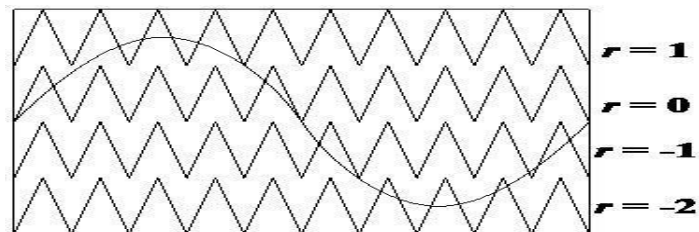
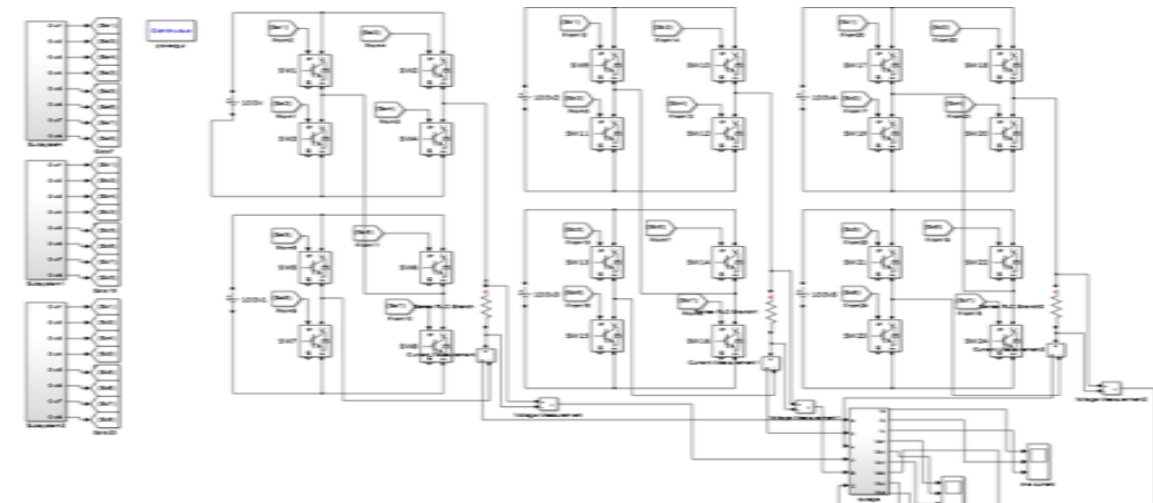


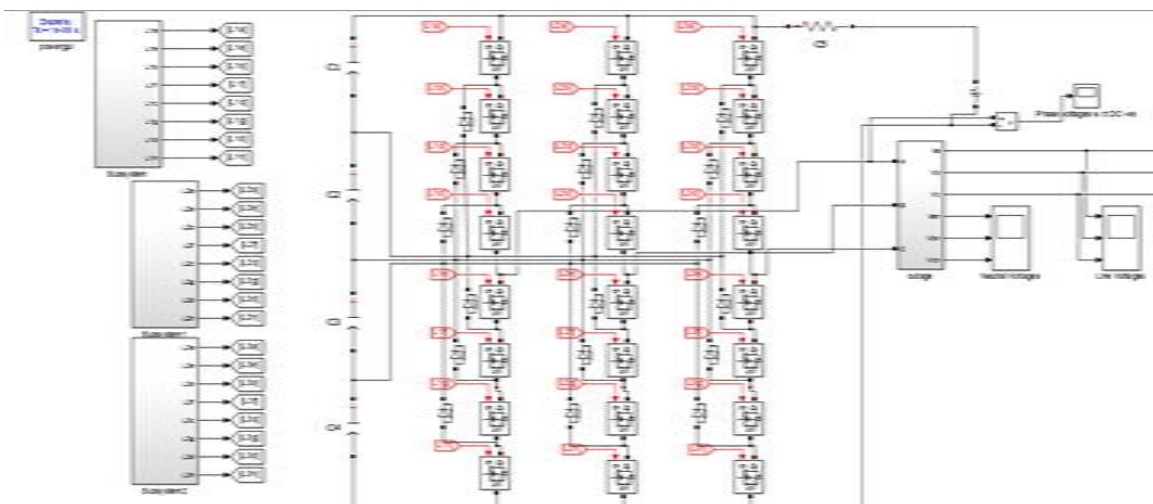
Figure 5. The SPWM carrier's signals of 5-level inverter

4. SIMULATION RESULTS

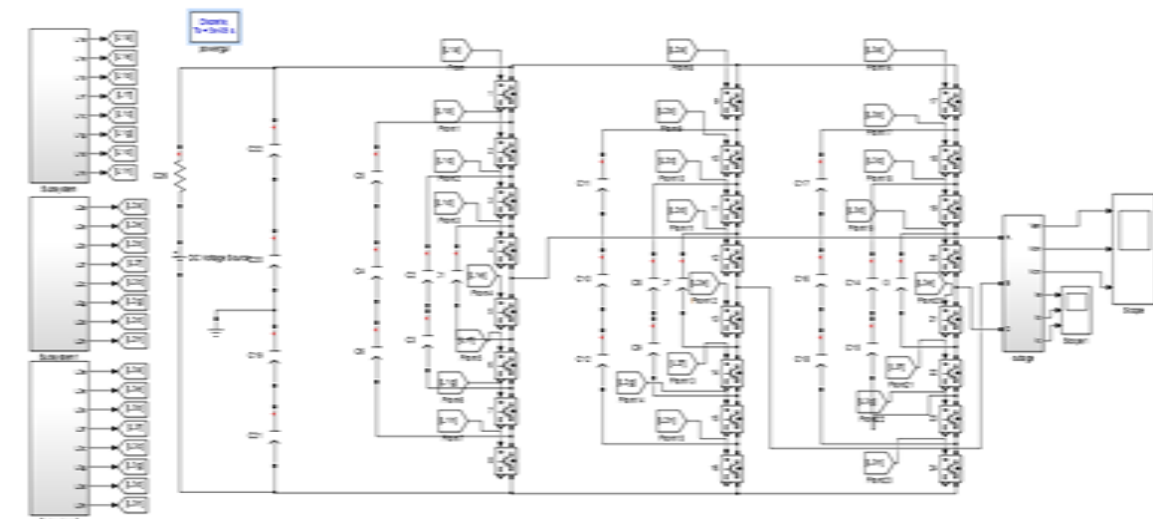
The three different topologies of five-level inverter have been designed by using MATLAB/SIMULINK environment, where the same SPWM modulation techniques is applied to each of them with 600Vdc and 100 ohm resistive load. Figure 6 shows the three different topologies of MLI designs in MATLAB/SIMULINK.



(a)



(b)



(c)

Figure 6. MLI topologies (a) CHMLI, (b) DCMLI and (c) FCMLI

The results are obtained which comprise the phase and line voltages as well as output current. The THD spectrum is generated for the voltage and current. Figure 7 presents the SPWM signal in which reference sign wave signal is compared against four triangular waves in order to generate the required pulses to control the inverter switches sequentially. Figure 8 shows the phase voltages for CHMLI, DCMLI and FCMLI along with their corresponding THD spectrum. As can be seen from the presented waveforms, CHMLI has better results compared to the DCMLI and FCMLI also produced less THD. All the topologies are simulated with same sampling and simulation time as well as same modulation index and switching pulses.

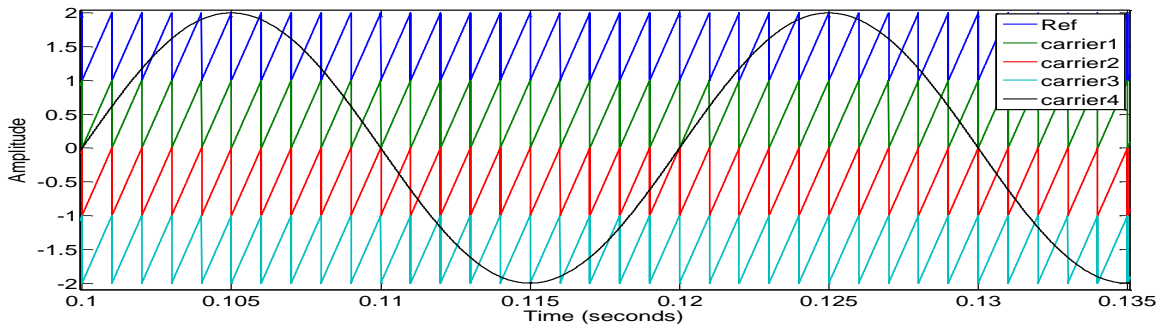


Figure 7. Comparison of reference signal with carrier signal

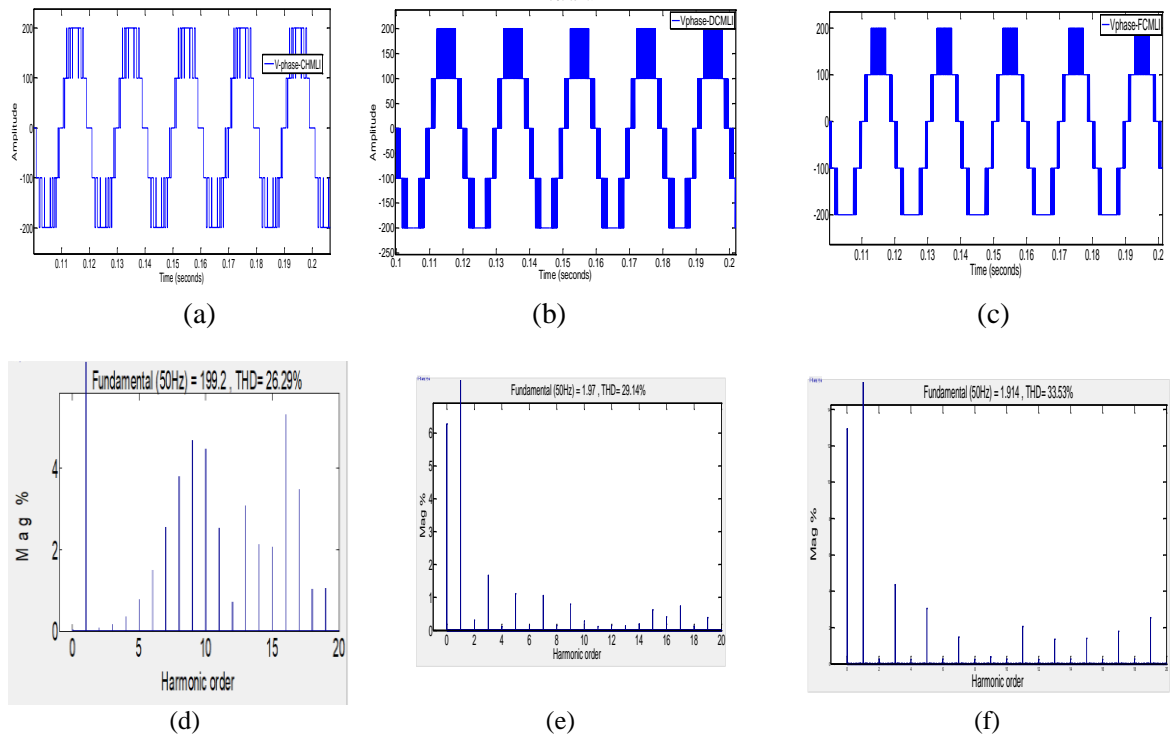


Figure 8. Phase voltage and THD ;(a)CHMLI,(b)DCMLI,(c)FLCMLI,(d)THD-CHMLI,(e) THD-DCMLI,(f) THD-FCMLI

Similarly, the phase voltages of the three different topologies are presented in Figure 9 along with THD spectrum showing that. CHMLI is superior in terms of performance and THD contents .The output line voltage and THD spectrum of the three topologies are presented in Figure 10 as well.

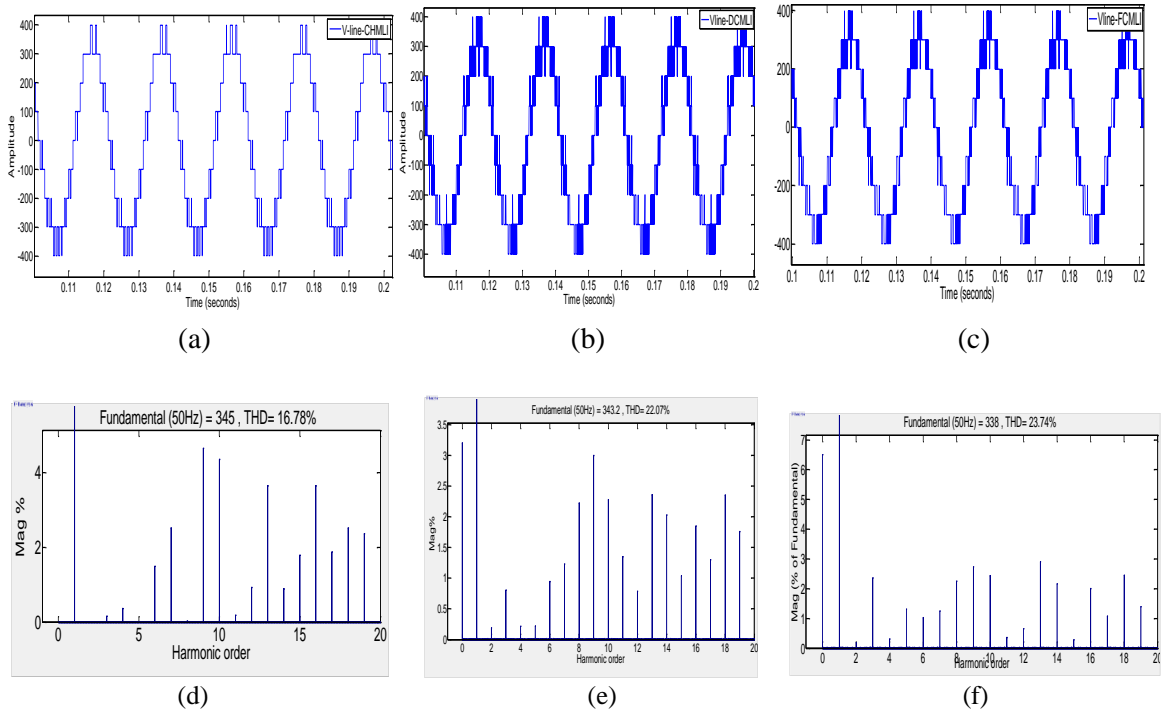


Figure 9. Line voltage and THD, (a)CHMLI, (b)DCMLI, (c)FLCMLI, (d)THD-CHMLI, (e) THD-DCMLI, (f) THD-FCMLI

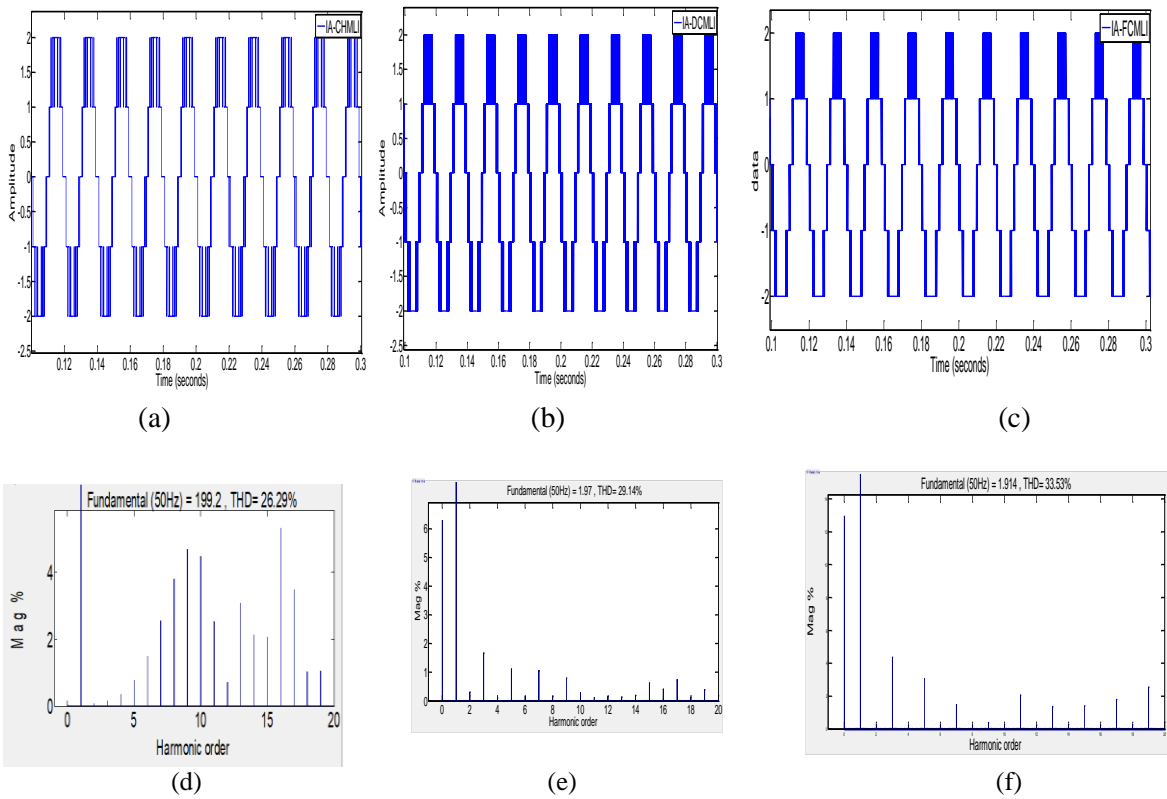


Figure 10. Output currents and THD ;(a)CHMLI,(b)DCMLI,(c)FLCMLI,(d)THD-CHMLI,(e) THD-DCMLI,(f) THD-FCMLI

Table 1 presents the comparison between the different topologies in terms of THD, components and DC sources. The superiority of the CHMLI is due to the less components used which may contribute in producing harmonics, hence affecting the inverter output. However, CHMLI requires single DC source for each bridge which can be costly, while the DCMLI and FCMLI use only one single DC source. MLI in general and CHMLI in specific comprises a set of advantageous features such as producing common voltage mode which minimize the stress on the motor switching frequency in which can operate at fundamental frequency higher or lower than the switching frequency and low switching frequency implies less switching losses and enhanced performance. In addition, the output of MLI is stepped waveform which almost sinusoidal with less harmonics contents.

Table 1. MLI topologies comparison

Type	No.Level	Components			THD			DC sources
		Capacitors	Diode	Switches	Vphase	Vline	Current	
CHMLI	5	0	0	12	26.29%	16.78%	26.29%	6
DCMLI	5	4	4	12	29.14%	22.07%	29.14%	1
FCMLI	5	12	0	12	33.53%	23.74%	33.53%	1

The comparison results have shown that, CHMLI is superior to DCMLI and FCMLI in terms of THD and number of components used. However, CHMLI utilizes many DC sources a DC source for each bridge while the DCMLI and FCMLI utilize single DC sources. Figure 11 shows the graphical representation of the THD for the different topologies, where CHMLI has the lowest THD value with (26.29%) followed by DCMLI with (29.14%), then FCMLI has the highest THD value with (33.53%).

The main source of the harmonics contents is from the components of the system or device. CHMLI generate less THD contents due to the less number components used in comparison to DCMLI and FCMLI which utilize active and passive components in the design. These components contribute to rise up the distortion to the output signal and hence increase its harmonics contents.

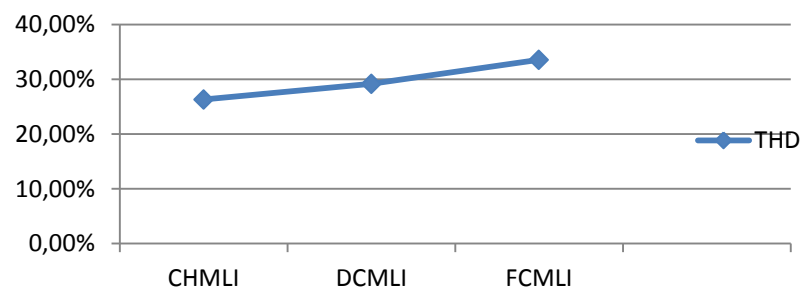


Figure 11. THD comparison between MLI topologies

5. CONCLUSION

Multilevel inverter has been attracted by many researchers and industries due to the capabilities of handling high and medium power application as well as renewable energy are DC in nature which require to be converted to AC utilizing inverter. There are many different configurations of MLI, hence this paper introduced three different topologies which are Cascaded H-bridge Multilevel Inverter (CHMLI), Diode Clamped Multilevel Inverter (DCMLI) and Flying Capacitor Multilevel Inverter (FCMLI). These topologies have been modelled in MATLAB/SIMULINK and controlled utilizing Sinusoidal Pulse Width Modulation (SPWM) with same sampling time and switching frequency. The obtained results shows that, CHMLI has less THD than other topologies also less components which make CHMLI superior and recommended to be used in many applications.

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REFERENCES

- [1] Dincer, Ibrahim. "Renewable energy and sustainable development: a crucial review." *Renewable and Sustainable Energy Reviews* 4.2 (2000): 157-175.
- [2] Ab Kadir, Mohd Zainal Abidin, Yaaseen Rafeeu, and Nor Mariah Adam. "Prospective scenarios for the full solar energy development in Malaysia." *Renewable and Sustainable Energy Reviews* 14.9 (2010): 3023-3031.
- [3] Sharma, Himanshu, et al. "Development and Simulation of Stand Alone Photovoltaic Model Using Matlab/Simulink." *International Journal of Power Electronics and Drive Systems* 6.4 (2015).
- [4] Fahrenbruch, Alan, and Richard Bube. *Fundamentals of solar cells: photovoltaic solar energy conversion*. Elsevier, 2012.
- [5] Zhao, Haoran, et al. "Review of energy storage system for wind power integration support." *Applied Energy* 137 (2015): 545-553.
- [6] Jaworski, Maciej, Marta Bednarczyk, and Marcelli Czachor. "Experimental investigation of thermoelectric generator (TEG) with PCM module." *Applied Thermal Engineering* 96 (2016): 527-533.
- [7] Twidell, John, and Tony Weir. *Renewable energy resources*. Routledge, 2015.
- [8] Hassaine, L., et al. "Overview of power inverter topologies and control structures for grid connected photovoltaic systems." *Renewable and Sustainable Energy Reviews* 30 (2014): 796-807.
- [9] Tang, Yu, et al. "Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability." *IEEE Transactions on Power Electronics* 24.2 (2009): 409-415.
- [10] Colak, İlhami, Ersan Kabalci, and Ramazan Bayindir. "Review of multilevel voltage source inverter topologies and control schemes." *Energy Conversion and Management* 52.2 (2011): 1114-1128.
- [11] Gupta, Krishna Kumar, et al. "Multilevel inverter topologies with reduced device count: A review." *IEEE Transactions on Power Electronics* 31.1 (2016): 135-151.
- [12] Z. B. Ibrahim, M. Hossain, M. Talib, R. Mustafa, and N. M. N. Mahadi, "A five level cascaded H-bridge inverter based on space vector pulse width modulation technique," in *Energy Conversion (CENCON)*, 2014 IEEE Conference on, 2014, pp. 293-297.
- [13] Manjrekar, Madhav D., Peter K. Steimer, and Thomas A. Lipo. "Hybrid multilevel power conversion system: A competitive solution for high-power applications." *IEEE transactions on industry applications* 36.3 (2000): 834-841.
- [14] Holmes, Donald Grahame, and Brendan P. McGrath. "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters." *IEEE Transactions on industry applications* 37.2 (2001): 574-582.
- [15] Ab Ghani, Mohd Ruddin, et al. "Investigation Study of Three-Level Cascaded H-bridge Multilevel Inverter." *TELKOMNIKA (Telecommunication Computing Electronics and Control)* 15.1 (2017): 125-137.
- [16] Ghani, Ab, et al. "Comparative Study of Different Multilevel Topologies of Five Level Inverter Using Spwm." *International Journal of Applied Engineering Research* 11.20 (2016): 10139-10145.
- [17] Palanisamy, R., et al. "Multicarrier-SPWM Based Novel 7-Level Inverter Topology with Photovoltaic System." *International Journal of Power Electronics and Drive Systems (IJPEDS)* 8.2 (2017): 826-834.
- [18] Rotella, Mauricio, et al. "PWM method to eliminate power sources in a nonredundant 27-level inverter for machine drive applications." *IEEE Transactions on Industrial Electronics* 56.1 (2009): 194-201.
- [19] Farah, Nabil, et al. "Multilevel Inverter Fed Switched Reluctance Motors (SRMs): 6/4, 8/6 and 10/8 SRM Geometric Types." *International Journal of Power Electronics and Drive Systems (IJPEDS)* 8.2 (2017).
- [20] Talib, Md Hairul Nizam, et al. "Characteristic of Induction Motor Drives Fed by Three Leg and Five Leg Inverters." *Journal of Power Electronics* 13.5 (2013): 806-813.
- [21] Lazi, Jurifa Mat, et al. "Speed and Position Estimator of Dual-PMSM for Independent Control Drives using Five-Leg Inverter." *International Journal of Power Electronics and Drive Systems (IJPEDS)* 8.2 (2017).
- [22] Wu, Bin. "Cascaded H-Bridge Multilevel Inverters." *High-Power Converters and AC Drives* (2006): 119-142.
- [23] Adam, Grain P., et al. "Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi two-state mode." *IEEE Transactions on Industrial Electronics* 55.8 (2008): 3088-3099.
- [24] Shukla, Anshuman, Arindam Ghosh, and Avinash Joshi. "Improved multilevel hysteresis current regulation and capacitor voltage balancing schemes for flying capacitor multilevel inverter." *IEEE Transactions on Power Electronics* 23.2 (2008): 518-529.
- [25] Yao, Wenxi, Haibing Hu, and Zhengyu Lu. "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter." *IEEE transactions on Power Electronics* 23.1 (2008): 45-51.
- [26] M. Kavitha, A. Arunkumar, N. Gokulnath, S. Arun 4. New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources. Final year students / Dept. of EEE / DR.S.J.S Paul Memorial College of Engineering & Technology / Pondicherry / India. ISSN: 2278-1676 Volume 2,

Issue 6 (Sep-Oct. 2012), PP 26-36

- [27] Dnyaneshwar D. Khairnar and V. M. Deshmukh. .Performance Analysis of Diode Clamped 3 Level MOSFET Based Inverter. Department of Electronics and Telecommunication, COET Bambhori, Jalgaon, India. International Electrical Engineering Journal (IEEJ) Vol. 5 (2014) No.7, pp. 1484-1489 ISSN 2078-2365
- [28] McGrath, Brendan Peter, and Donald Grahame Holmes. "Multicarrier PWM strategies for multilevel inverters." Industrial Electronics, IEEE Transactions on 49.4 (2002): 858-867.