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Analysis and Design of Single Phase High Efficiency Transformer Less PV Inverter Topology

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ABSTRACT

An inclination towards renewable energy resources has been increased due to the requirement of clean environment and to satisfy the increasing power demand for the long run. A grid connected system requires the availability of a transformer in its power conversion stages that provides galvanic isolation between the grid and the power system. But inclusion of transformer results in making the system bulky and more expensive. In this paper different transformer-less PV inverter topologies are analyzed by comparing their efficiency, leakage current and THD of load current using MATLAB/Simulink environment. To achieve maximum power from PV system, maximum power point controller (P&O algorithm) is used. From the simulation results, modified HB-ZVR is found to have minimum leakage current and constant common mode voltage with higher efficiency. The hardware results are obtained for modified HB-ZVR topology.

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1. INTRODUCTION

According to a recent report by International Energy Agency, the increase of amount of electricity produced from renewable sources increased from just over 13% in 2012 to 22% the following year. They also predict that that figure should hit 26% by 2020. The qualities of renewable energy resources like reliability, cheap and reusable has been able to catch the attention of every power industry available. Out of the different renewable energy resources available solar energy is considered as the most widely used as most renewable energy comes directly or indirectly from sun that can be used for generating electricity, solar cooling and variety of commercial purposes [1].

The grid connection allows injecting the power generated from the PV system into the grid [2]. In order to integrate PV system with utility grid, the PV system is commonly divided into three stages: the PV panel with MPPT controller, the power inverter and the grid filter. In the conventional grid connected PV systems, the last stage includes a low frequency transformer (LFT) to connect to the grid [3], [4]. Also, this LFT provide galvanic isolation avoiding leakage current between PV system and ground. But the main problem with LFT is that it results in making the system more bulky and expensive. Furthermore, heating is observed in the system which increases the losses, affecting the overall efficiency of the system. Moreover, the efficiency is also affected due to the inclusion of additional power stages into the system. So, a conventional approach towards transformer-less topology is provided to develop a more efficient system [5]. But the absence of galvanic isolation results in generation of leakage current flow through the capacitor between the photovoltaic array and earth that may lead to electromagnetic emissions that can damage the circuit. Hence an efficient transformer-less topology [6] has been selected which provides very less leakage current and constant common mode voltage [CMV].

In order to minimize the leakage current through the parasitic capacitor, the midpoint of the DC link capacitors should be connected to the neutral of the grid like the half bridge with neutral point clamped. This also prevents the DC current injection back into the grid preventing it from damage [7]. In order to develop an efficient system different transformer-less topology based on their higher efficiency levels are considered for analysis. The different transformer-less topologies are Unipolar switching using H-bridge, HERIC topology and HB ZVR topology.

Unipolar switching using H-bridge [8] ensures high efficiency but results in large leakage current due to variation in the CMV. HERIC topology on the other hand results in no CMV that leads to high efficiency. But this results in large switching losses due to the presence of six switches [9]. To reduce the switching losses and leakage current, a new topology has been adopted i.e. HB ZVR that results in constant CMV and reduced leakage current.

In this paper, the efficiency, leakage current and THD of output current are compared for different transformer-less topologies like Unipolar switching with H-Bridge, HERIC and HB-ZVR topology. Based on the simulation results obtained HB-ZVR is considered as the most efficient with minimum leakage current. But this topology suffers from varying CMV. Hence to overcome this disadvantage some modification is done in the conventional HB-ZVR topology. The MPPT technique is used to extract maximum power from PV array at any operating temperature and irradiance condition. The hardware circuit is implemented for modified HB-ZVR topology.

2. TRANSFORMER-LESS TOPOLOGIES

The common mode voltage measured influences the leakage current that flows through the parasitic capacitor of the PV panels. As the utility grid system is not influenced by the common mode behavior of the system, so common mode voltage of an inverter topology can be shown through a resistive load. Hence for the simulations and hardware implementation a resistive load is taken and CMV is measured between the positive terminal of the DC source and the mid-point between the resistors which is grounded.

2.1. Unipolar Switching Using H-Bridge

Single phase H-Bridge inverters prefer unipolar switching topology with a view to get better injected current quality of the inverters. In this method, two sine waves of same frequency and magnitude but 180 degrees out of phase, V_m and V_m- are compared with a triangular wave, generating two gate signals as shown in Figure 1 for the switches S_1 and S_3 of the unipolar circuit as shown in Figure 2. In this case, the inverter output voltage either switches between 0 to +V during positive half or between 0 to –V in the negative half cycle. It offers reduced switching losses and has higher efficiency than Bipolar PWM but the CMV measured in this topology is varying and hence leads to large leakage current i.e. unsafe for operation of inverter [10, 14, 16].

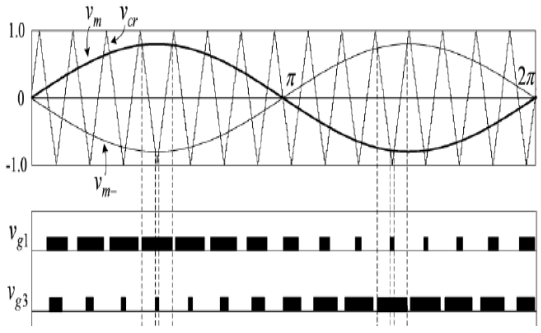

Figure 1. Waveform of Unipolar Modulation Scheme

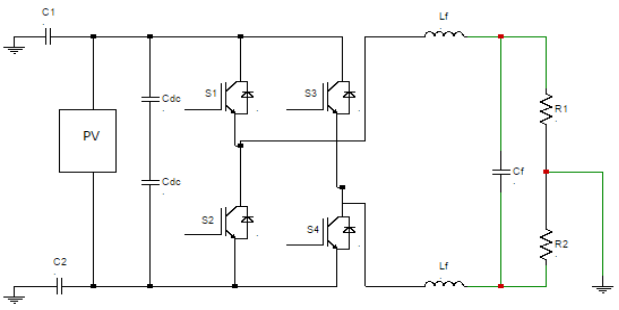

Figure 2. Unipolar Topology

2.2 HERIC Topology

HERIC stands for highly efficient and reliable inverter concept. HERIC topology adds up the merits of both unipolar and bipolar topology. It has three levels of voltage output, higher efficiency and has very less leakage current. Here Zero voltage state can be achieved by introducing a bi-directional switch that consists of two MOSFETs (S_5 and S_6) and two diodes as shown in Figure 3. The function of these bidirectional switches is to provide zero voltage stages during the positive and negative half cycles. In the

positive half cycle, S_1 and S_4 are in ON state and freewheeling period occurs when S_6 is turned ON. Similarly, in negative half cycle, S_2 and S_3 are turned ON and S_5 is used during the freewheeling period. Although efficiency is increased here and system generates almost no CMV but in this type of topology the number of semiconductors used is more that increases the switching losses [11] and the efficiency goes down.

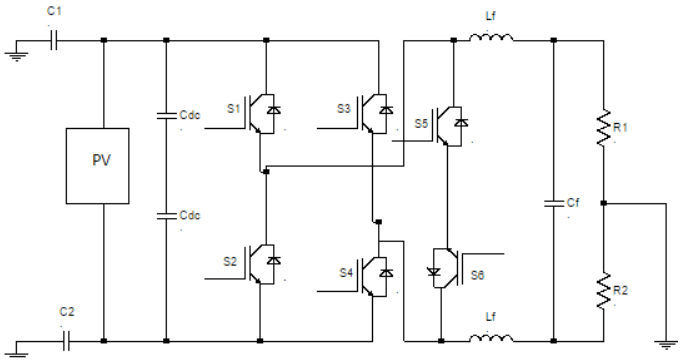

Figure 3. HERIC Topology

2.3 HB ZVR Topology

In this method, zero state can be generated by using bi-directional switch which comprises of one MOSFET and diode bridge. The bi-directional switch is connected to the midpoint of the DC-link capacitors through a diode as shown in Figure 4, in order to make the voltage constant during the zero state. The zero voltage is achieved when S_5 is turned ON and consequently all other switches S_1, S_2, S_3 and S_4 are in OFF state [11]. The required gate signal for S_5 is complementary to that of S_1, S_4 in positive cycle and S_2, S_3 in negative cycle with a small-time interval so that short circuit of input capacitor will not happen. In the positive cycle S_1 and S_4 are in ON state that generates positive output voltage and S_5 is controlled using the complementary signal. Similarly, in the negative half other two switches (S_2, S_3) are in ON state that generates the active vector and when they are OFF, S_5 is ON. Three levels of output voltage are observed here and ripples in load current is very less. The CMV is almost constant leading to very less leakage current [11, 15].

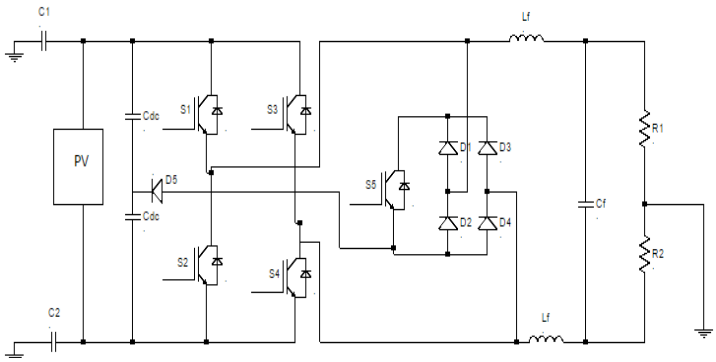

Figure 4. HB ZVR Topology

2.4 Modified HB ZVR Topology

The HB- ZVR is the most efficient topology but it suffers from some disadvantages. This topology incurs losses in the small-time interval between active and zero voltage states due to the flow of freewheeling current through the diodes while the switches are in OFF state [12, 13]. To solve this problem one more diode is introduced in antiparallel to D_6 as shown in the Figure 5. When the freewheeling period occurs, V_{AN} and V_{BN} are not constant to $V_{dc}/2$ and there are variations in the amplitude which depends on the circuit

specifications and junction capacitances. When S_5 is ON freewheeling period occurs. When V_{fp} is greater than $V_{dc}/2$, diode D_5 gets forward biased and D_6 gets reversed biased. On the other hand, when the V_{fp} is less than $V_{dc}/2$, D_6 is forward and D_5 is reversed biased resulting current owing from the diode D_6, to increase the V_{fp} to Vdc/2. In the small time between the conduction and freewheeling period, CMV is varying with the magnitude. In HB ZVR, the clamping branch has only one diode D_5. Hence, the clamping is restricted only for the period when V_{fp} is more than V_{dc} /2. Since D5 is reverse biased in the region when V_{fp} is less than $V_{dc}/2$, the clamping branch does not function. This leads to variation in the CMV, resulting in the flow of leakage current. This drawback is corrected by extra added diode D_6 in this modified topology. With both D_5 and D_6 CMV is constant to $V_{dc}/2$ throughout the freewheeling period. As a result, leakage current is almost eliminated.

$$V_{cm} = \frac{V_{AZ} + V_{BZ}}{2} \tag{1}$$

Positive cycle:

$$V_{cm} = \frac{V_{AZ}+V_{BZ}}{2} = \frac{V_{dc}+0}{2} = \frac{V_{dc}}{2} \tag{2}$$

Negative cycle:

$$V_{cm} = \frac{V_{AZ}+V_{BZ}}{2} = \frac{0+V_{dc}}{2} = \frac{V_{dc}}{2} \tag{3}$$

Zero state:

$$V_{cm} = \frac{V_{AZ}+V_{BZ}}{2} = \frac{\frac{V_{dc}}{2}+\frac{V_{dc}}{2}}{2} = \frac{V_{dc}}{2} \tag{4}$$

As shown in the equations (1) to (4), the CMV is constant for all the switching states which results in small leakage current through the parasitic capacitor of the PV panels.

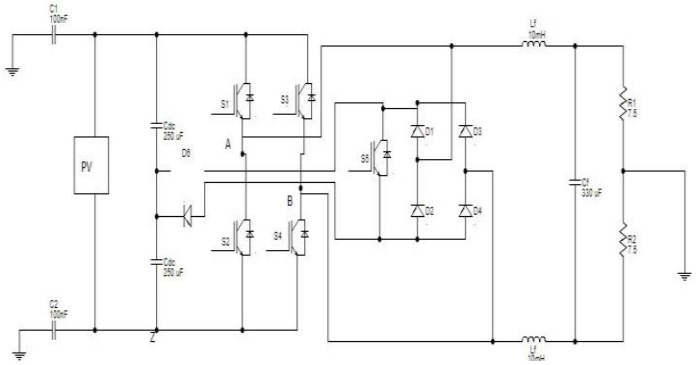

Figure 5. Modified HB ZVR Circuit

3. SIMULATION RESULTS

For the performance analysis, different transformer-less PV inverter topologies were simulated using the MATLAB/Simulink software. The parameters are given in Table 1. The efficiency and total harmonic distortion (THD) level are evaluated for different inverter topologies. The results indicate that modified HB ZVR topology has minimum THD and leakage current which prevents the circuit from damage.

Table 1. Circuit Parameters

DC Link Capacitor, C_{dc}	250 uf
Parasitic Capacitor	100 nf
Load Resistor, R	7.5 ohm
Filter Capacitor, C_f	330 uf
Filter Inductor, L_f	10 mH
Switching Frequency	4kHz
Input DC Voltage	12 V

The full bridge with unipolar modulation has three level output voltage shown in Figure 6(a) and it has high efficiency. However, this topology generates varying CMV and causes high leakage currents compared to other topologies which can be observed in Figure 6(b). Figure 6(c) shows load current waveform for Unipolar inverter topology and the amplitude of load current is 0.8A. It is observed that THD of load current is 3.38% as shown in Figure 6(d). This topology is not advisable for the transformer-less PV inverter because of safety issues due to large leakage current. The efficiency is measured to be 95-96%.

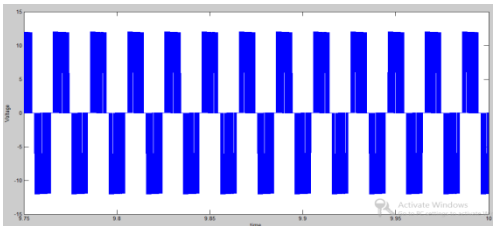

Figure 6(a). Output Voltage of Unipolar Inverter

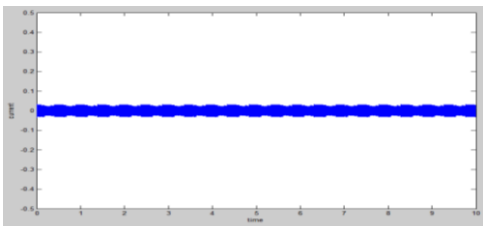

Figure 6(b). Unipolar Leakage Current

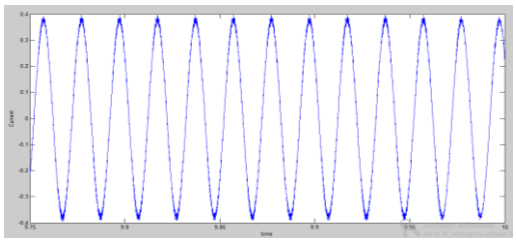

Figure 6(c). Load Current of Unipolar topology

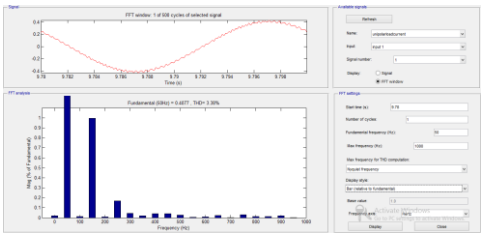

Figure 6(d). Unipolar THD Plot

In case of HERIC topology, the output voltage has 3 levels as in unipolar topology as depicted in Figure 7(a). In this case, due to almost zero CMV, the leakage current is very less as observed in Figure 7(b) during simulation. But it involves the use of more semiconductor devices and THD is less than the Unipolar topology as seen from Figure 7(d) for the load current of Figure 7(c). The efficiency level is least in this topology i.e. 93-94 percent and the THD levels is 2.91%.

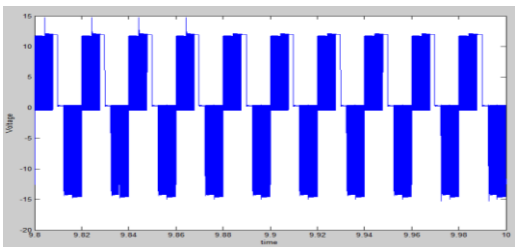

Figure 7(a). HERIC Inverter Output Voltage

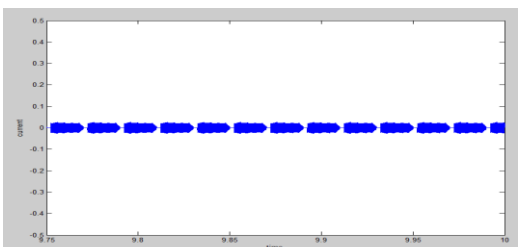

Figure 7(b). HERIC Leakage Current

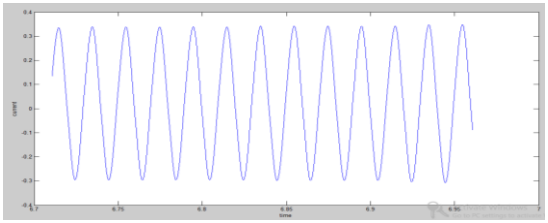

Figure 7(c). Load Current of HERIC Topology

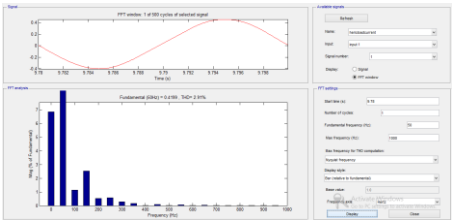

Figure 7(d). THD Plot of HERIC Topology

HB-ZVR also has three level output voltage as shown in Fig. 8(a) and constant CMV. Fig. 8(b) depicts the load current of HB-ZVR topology. Also, the leakage current is least among all the topologies as observed from Fig. 8(c) which can be further reduced by adding a diode as shown above in Fig. 5. The leakage current can be made very less by making the CMV constant to $V_{dc}/2$ as can be seen from Fig. 8(d). Here THD is least among all the topologies discussed i.e. 2.63% as seen from Fig. 8(e) which can be reduced to 2.37 as observed in Fig. 8(f) by adding an extra diode. The efficiency is around 94-95 percent in this topology.

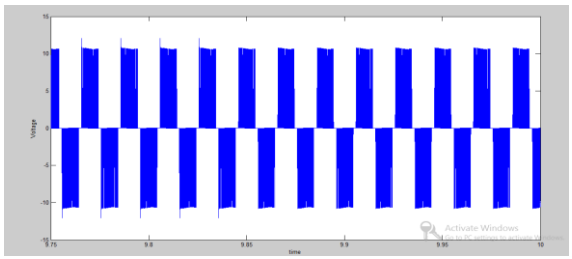

Figure 8(a). HB ZVR Inverter Output Voltage

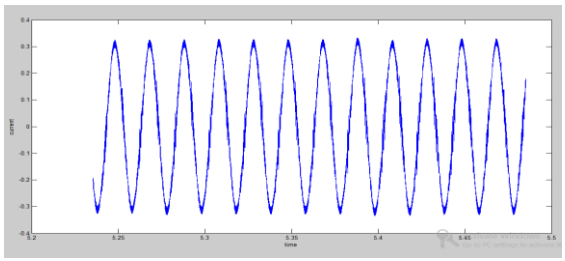

Figure 8(b). HB-ZVR Load Current

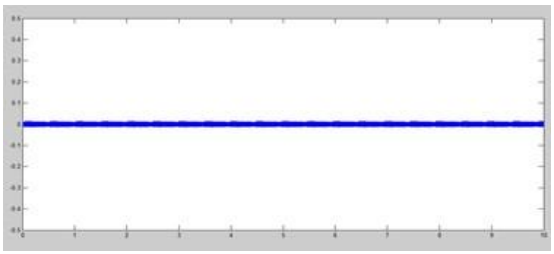

Figure 8(c). HB ZVR Leakage Current

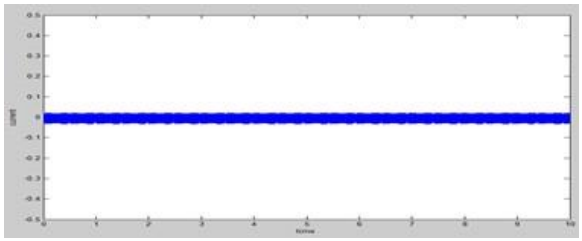

Figure 8(d). Modified HB ZVR Leakage Current

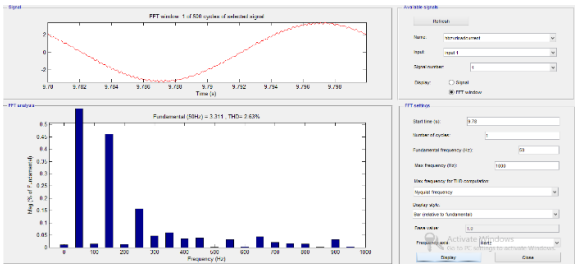

Figure 8(e). THD Plot of HB-ZVR

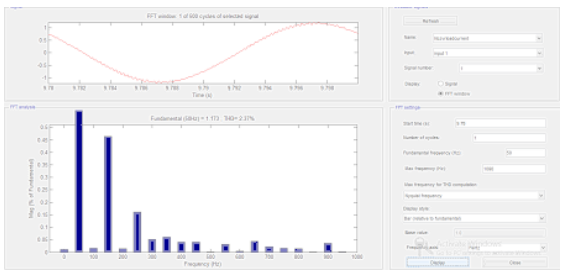

Figure 8(f) THD Plot of Modified HB-ZVR Topology

4. HARDWARE RESULTS

Simulation results have been reported to compare the performance of the different transformer-less inverter topologies. From these simulation results it is revealed that the leakage current is found to be very less for the modified HB ZVR topology with higher efficiency and low THD of load current. For the hardware implementation of the modified HB ZVR, same specifications as in the case of simulation are considered. The hardware setup of the modified HB ZVR topology is shown in Figure 9. Arduino UNO is used to generate the PWM signal that is given to the gate of MOSFETs present in the inverter circuit through the MOSFET driver IR2110.

The output voltage of the modified HB ZVR inverter topology is depicted in Figure 10 and has 3-levels i.e. +V, 0 and –V. Figure 11 depicts the filtered output voltage of modified HB ZVR topology which is sinusoidal in nature and given to load. From the given hardware setup in Fig. 9 we were able to achieve high efficiency 95.4% with the least leakage current to be around 2.3% which matches to the simulation results presented above. On comparing with the HB-ZVR topology with our proposed topology we were able to achieve high efficiency from 94% to 95.5% through minimizing the losses by inserting an extra diode thereby limiting the transition losses between active and zero voltage state. Also, we found that the leakage current is 2.3% which is least among all topologies by making the CMV constant through insertion of freewheeling diode. Through this we were able to achieve high efficiency and low leakage current combined to achieve higher power.

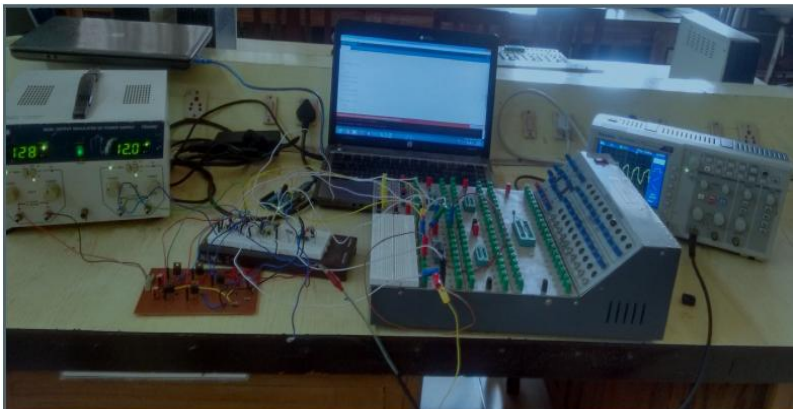

Figure 9. Hardware Setup of Modified HB ZVR

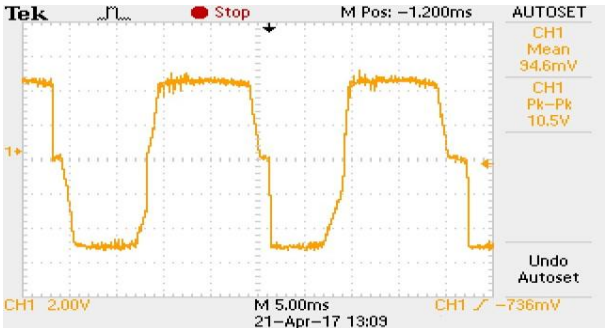

Figure 10. Inverter Output Voltage of Modified HB ZVR

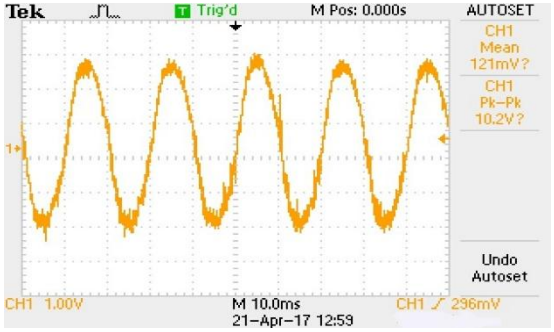

Figure 11. Inverter Output Voltage of Modified HB ZVR

5. CONCLUSION

Transformer less inverters has more efficiency as compared to those inverters that have transformer. It has been observed that when the transformer is removed, the CMV of the inverter topology has a significant impact on the ground leakage current. In this paper a comparison between different transformer-less topologies is done based on efficiency, leakage current and THD of the output current. From the simulation results it is found that the common-mode voltage of modified HB-ZVR topology is constant and

having higher efficiency compared to other topologies with minimum leakage current. The modified HB-ZVR topology is implemented and hardware results are obtained.

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