International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 9, No. 2, June 2018, pp. 504~518
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v9.i2.pp504-518

Level Shifted Discontinuous PWM Algorithms to Minimize Common Mode Voltage for Cascaded Multilevel Inverter Fed Induction Motor Drive

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Article Info

Article history:

Received Jan 12, 2018
Revised Apr 10, 2018
Accepted Apr 24, 2018

Keyword:

Cascaded multi level inverter
Multicarrier PWM
Common mode voltage (CMV)
DPWM
Total harmonics distortion

ABSTRACT

This paper presents combinations of level shifted pulse-width modulation algorithm with conventional discontinuous pulse-width modulation methods for cascaded multilevel inverters. In the proposed DPWM a zero sequence signal is injected in sinusoidal reference signal to generate various modulators with easier implementation. The analysis four various control strategies namely Common Carrier (CC), Inverted Carrier (IC), Phase Shifted (PS) and Inverted Phase Shift (IPS) for cascaded multilevel inverter fed induction motor drive has been illustrated. To validate the proposed work experimental tests has been carried out using dSPACE controller. Experimental study proves that using proposed algorithms reduction in common-mode voltage with fewer harmonics along with reduced switching loss for a cascaded multilevel inverter fed motor drive has been achieved

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1. INTRODUCTION

In recent years, multilevel inverters have been intensively developed for industrial power converters and some of interesting advantages of multilevel inverters such as low distortion in output voltage with relative less common mode voltage, low harmonic and electromagnetic interference (EMI), attracted researcher attentions [1-4]. Multilevel Inverters are used in many applications such as uninterruptible power supply (UPS), Medium voltage Industrial (induction motor) drives, ship propulsion Induction heating, high voltage direct current (HVDC) power transmission, grid connected photovoltaic system, railway locomotives, active filters, wind Energy System, and applications of power system for example flexible AC transmission (FACTS). As the number of levels increases the output of the voltage is very close to sinusoidal signal reduces harmonic distortion.

Their main topologies such as: diode-clamped type, cascaded type and capacitor clamped type are commonly used as shown in Figure 1. Three PWM techniques such as selective harmonic elimination PWM (SHEPWM), carrier-based PWM (CPWM), and space vector PWM (SVPWM) , have been favorably used in practice. Because of having a small number of switching, the selective harmonic elimination PWM method shows be advantageous for high power applications. Two remaining PWM techniques are commonly used in various fields because of their excellent PWM qualities. The DPWM methods of two-level inverters have been studied for many years, and they are introduced as an approach to reduce the switching loss [5-6]. DPWM methods can be realized using space vector PWM approach by eliminating one from the redundant zero vectors in the switching state sequence ; or carrier-based PWM ones by adding offset to make some leg-

voltage attain one of two dc-rail levels [7-10]. Some studies were concentrated on the analyzing the impacts of DPWM waveforms on the current ripple.

Three level inverters continue to attract the attention of researchers ever since introduced by Nabae,A. et.al. [11]. Though simple and elegant, the neutral-clamped circuit topology suggested in [11], has a few disadvantages. The neutral point fluctuation is a commonly encountered problem in this configuration, as the capacitors connected to the DC-bus carry load currents. Also, there is an ambiguity regarding the voltage rating of the semi-conductor devices, which are connected to the neutral point. This calls for a conservative selection of these devices for reliable operation, enhancing the cost.

In this paper, a new circuit configuration for a 3-level inverter as shown in figure1 has been proposed. In this circuit configuration, 3-level inversion is realized by connecting two 2-level inverters in cascade as shown in Figure 1. The DC-link capacitors in this circuit do not carry the load currents and hence the voltage fluctuations in the neutral point are absent. However, the power semi-conductor switches in one bank (three in number) in one of the inverters in this circuit have to be rated for the full DC-link voltage.Each inverter is powered with an isolated DC-power supply, with a voltage of Vdc/2 in Figure 1. The symbols V_{a1o}, V_{b1o}, Vc_{1o} respectively denote the output voltages of inverter-1 with respect to the point 'O' in Figure 1. Similarly, the symbols V_{a2o}, V_{b2o}, V_{c2o} respectively denote the pole voltages of inverter-2 with respect to the point 'O' in Figure 1.

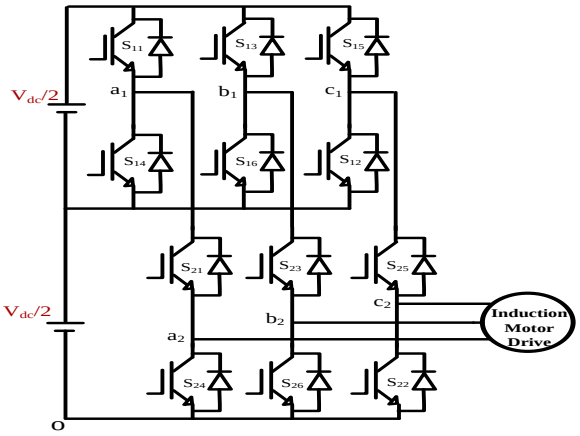


Figure 1. Proposed three-level cascaded inverter configuration

The pole voltage of any phase in inverter-2 attains a voltage of V_{dc}, under the following conditions:

a) The top switch of that leg in inverter-2 is turned on.
b) The top switch of the corresponding leg in inverter-1 is turned on.

Similarly the pole voltage of any phase for inverter-2 attains a voltage of $V_{dc}/2$, under the following conditions:

a) The top switch of that leg in inverter-2 is turned on.
b) The bottom switch of the corresponding leg in inverter-1 is turned on.

Thus, the DC-input points of individual phases of inverter-2 may be connected to a DC-link voltage of either Vdc or Vdc/2 by turning on the top switch or the bottom switch of the corresponding phase leg in inverter-1.

Additionally, the pole voltage of a given phase in inverter-2 attains a voltage of zero, if the bottom switch of the corresponding leg in inverter-2 is turned on. In this case, the DC-input point of that phase for inverter-2 is floating as the top and bottom switches are switched complimentarily in any leg in a 2-level inverter. Thus, the pole voltage of a given phase for inverter-2 is capable of assuming one of the three possible values 0, $V_{dc}/2$ and V_{dc} which is the characteristic of a three level inverter.The mathematical expression for the common mode potential can be derived from the inverter pole voltages as

$$V_{com} = \frac{V_{a2o} + V_{b2o} + V_{c2o}}{3}$$

Table 1. Pole Voltage of Inverter-2

Switches turn on Inverter-I	Switches turn on Inverter-2	pole voltage of Inverter-2
S14 or S16 or S12	S21 or S23 or S25	V_{dc}
S14 or S16 or S12	S21 or S23 or S25	$V_{dc}/2$
S11 or S13 or S15	S22 or S24 or S26	0
S11 or S13 or S15	S22 or S24 or S26	0

2. SIMPLIFIED DISCONTINOUS PWM ALGORITHM

Conventional SVPWM technique can be implementation in digital approach or in carrier based modulation approach. In CSVPWM algorithm, the desired reference voltage vector is generated by time averaging the suitable discrete voltage vectors in every sub cycle or sampling time period T_s. For a given reference voltage vector and Ts, the duration T1, T2 and TZ are unique. The expressions for the various active state time durations and zero states time duration in the first sector can be given in [3]

$$T_1 = \frac{V_{ref}\sin(\pi/3-\alpha)}{\sin(\pi/3)}T_s \quad (1)$$

$$T_1 = \frac{V_{ref}\sin(\pi/3-\alpha)}{\sin(\pi/3)}T_s \quad (2)$$

$$T_Z = T_s - T_1 - T_2 \quad (3)$$

The calculation of switching times requires angle and sector information which increases complexity of the algorithm. Hence to reduce complexity involved in conventional SVPWM, simplified scalar PWM algorithm has been proposed which does not require angle and sector information.

Consider three reference signals expressed as

$$V_i = V_p * Sin(w_e t - 2(j-1)\pi/3) \quad (4)$$

Where i=a,b,c and j=1,2,3 (i = j)

It is recognized and proposed that an addition of a zero sequence signal to each of the reference modulator makes it possible to utilize the DC bus voltage 15.5% more as compared with conventional SPWM method. It means that it is possible to increase the fundamental output voltage of the inverter by 15.5%. On the other hand the use of zero sequence signal [12-13] not only increases the DC bus utilization by 15.5% but also reduces the switching loss of the inverter, it means that number of on and off of the inverter switch is reduced by 33% by clamping each of the pole voltage to either positive bus or negative bus for a period of 120^o.

The proposed simplified discontinuous algorithm uses the concept of injected zero sequence signal [12-13], different modulators can generated by adding the zero sequence component to the three phase reference sinusoidal signal, different zero sequence components thus leads to different modulating signals with different properties.A generalized expression that generates the zero sequence components V_0 as a function of V_M, V_m and Z_0 is given by [14]

$$V_o = -[(1-2*Z_0) + Z_0 * V_M + (1-Z_o) * V_m] \quad (5)$$

Where $Z_0 = \frac{T_7}{T_0 + T_7}$ (6)

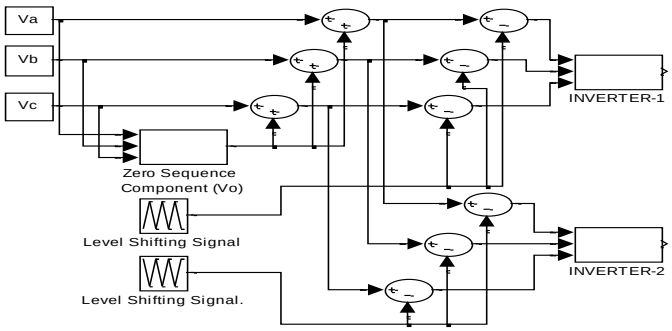


Figure 2. Block diagram illustrating scalar PWM for cascaded three level inverter configuration

By using the zero sequence component various PWM Modulators can be generated, can be expressed in terms of V_0 and reference signal as

$$V_i^* = V_i + V_o \quad (7)$$

$T_0+T_7 = T_z$ gives the total freewheeling time (Zero state time) of the inverter, V_M and V_m are the maximum and minimum values of the three phase reference signal (V_i).Moreover, by utilizing the concept of unequal division of zero state time, various PWM algorithms can be generated. In the proposed simplified DPWM algorithm, by varying the zero sequence component partition parameter Zo between 0 and 1, various PWM algorithms can be generated.

Table 2: Generation of CPWM and DPWM algorithms

S No.	PWM algorithm	Zero sequence Component V_o value
1	CSVPWM	Vo = -(V_M+V_m)/2
2	DPWM1	*If* |V_m|> V_M $\Rightarrow$ Vo = -(1+V_m) *If* |V_m|< V_M $\Rightarrow$ Vo = (1-V_M)

When Z_0=0.5, from equation (7) describes the equal division of zero state time, i.e. T_0=T_7 which results in the conventional space vector PWM algorithm, and the corresponding zero sequence component is equal to average of V_M & V_m , V_0= - (V_M+V_m)/2.Among various Continuous PWM possibilities, Z_0=0.5 is the best choice which have been concluded in the literature[15]. In case DPWM, change of Z_0 from 1 to 0 coincides with middle of the reference signal, the resultant modulating signal is known as DPWM1 which clamps at any fundamental time instant one of the pole is connected to negative bus for a period of 120^0 while the other two are modulating.

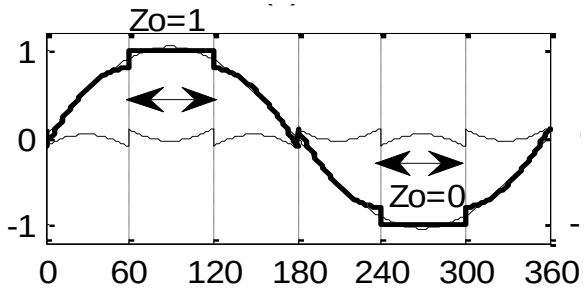


Figure 3. Showing DPMW1 Moulator

3. MULTI CARIER CONTROL STRATEGIES

Together with the development of multilevel inverter topologies appeared the challenge to extend traditional modulation methods to the multilevel case. The switching frequency can subdivide multilevel modulations into three different classes, namely, fundamental, mixed and high switching frequency. Fundamental switching frequency modulations produce switch commutations at output fundamental frequency and can be aimed to cancel some particular low frequency harmonic while, mixed switching frequency modulations are those in which switches commutate at different frequency, like hybrid multilevel modulation, and are particularly suited for hybrid converters, different cells can easily commutate at different frequencies. And finally, high switching frequency modulations are the adaptation of standard PWM to multilevel and they are meant to switch at very high frequency, about 10 to 20 kHz [16]-[18]. But this paper focus only on some high frequency switching control schemes such as CC, IC, PS and IPS.

3.1 Common Carrier Control Scheme (CC)

Common carrier control scheme as shown in Figure 4 is one of the PWM technique for multilevel inverter. For N level inverter N-1 in-phase carriers and a reference signal with the amplitude Am and the frequency Fm (50 or 60 Hz) are required.

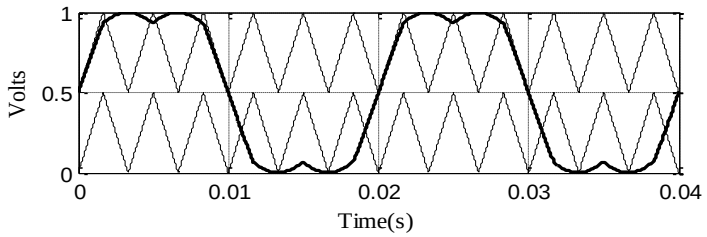


Figure 4. Proposed CCPWM scheme for cascaded three level inverter.

The control concept is the top carrier and bottom carrier signal are in phase with each other and are compare with a three phase reference signals given in equation (5) to obtain three level operation. Top carrier signal generates the pulse pattern for inverter-1 and similarly bottom carrier signal generates pulse pattern for inverter-2.

3.2 Inverted Carrier Control Scheme (CC)

In inverted carrier control scheme as shown Figure 5, top carrier and bottom carrier signal are in out of phase (180^{O}) with each other and are compared with a three phase reference signals given in equation (5) to obtain three level operation. Top carrier signal generates the pulse pattern for inverter-1 and similarly bottom carrier signal generates pulse pattern for inverter-2.

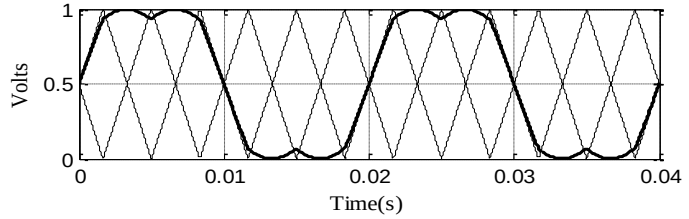


Figure 5. Proposed ICPWM algorithm for cascaded three level inverter

3.3 Phase Shifted control scheme (PS)

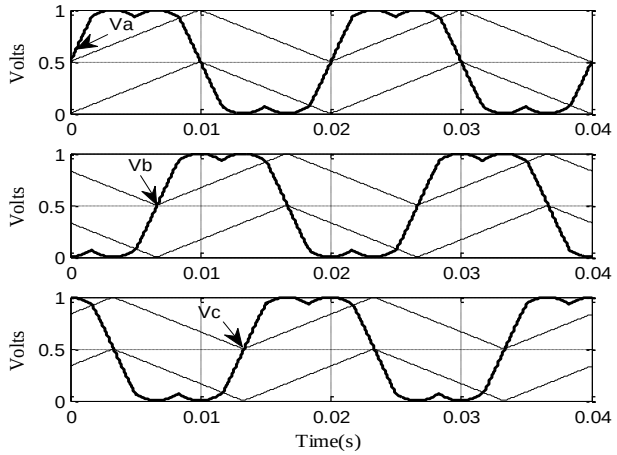


Figure 6. Proposed PSPWM algorithm for cascaded three level inverter.

In the proposed phase shifted control scheme carrier signals of each leg are phase shifted by 120^{O} horizontally but where as in the previous scheme for all the three legs of the inverter carrier signals are in same phase. As shown in Figure 6, it may be noted that top and bottom carrier signals are in same phase.

3.4 Inverted Phase Shifted control scheme (IPS)

In this inverted phase shifted control scheme, carrier signals of each leg are phase shifted by 120^{O} horizontally and also the top and bottom carrier signals of same leg are in out of phase (180^{O}) as shown in Figure 7.

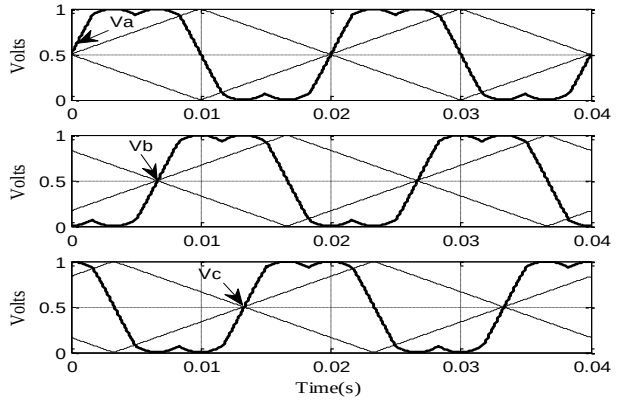


Figure 7. Proposed IPSPWM algorithm for cascaded three level inverter
as shown below and cited in the manuscript

4. EXPERIMENTAL RESULTS AND ANALYSIS

To evaluate the performance of proposed multi carrier PWM algorithms experimental tests have been carried out on v/f controlled 1 Hp, 415 V, 1.8 A and 50 Hz induction motor drive. The induction motor drive is fed by two 9.2 kVA dc-link inverters with uncontrolled rectifier at its front end. dSPACE 1104 control board has been used t generate switching pulses (1 kHz) for both inverters.

A DC voltage of 270 V is given to inverter-1and inverter-2, so that an effective DC voltage of 540 V is employed. To measure line voltage and current on digital storage oscilloscope (DSO), a 500 V to 6.3 V regulator (LV20-P) is used. The obtained results are shown from figure 8 to figure 47.

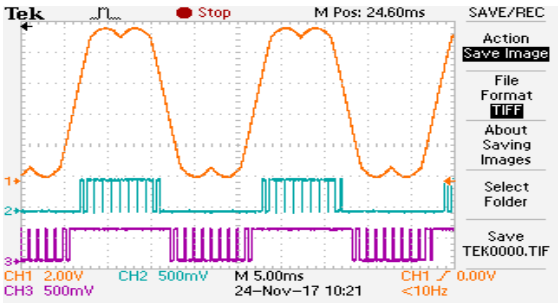


Figure 8. Common Carrier Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II :SVPWM

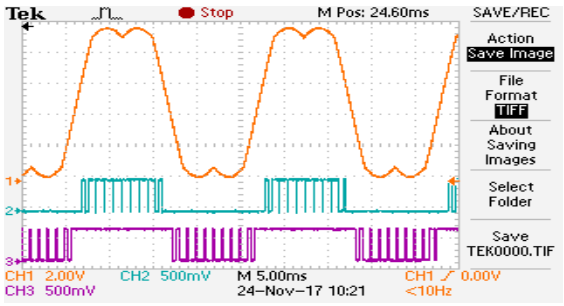


Figure 13. Inverted Carrier Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II :SVPWM

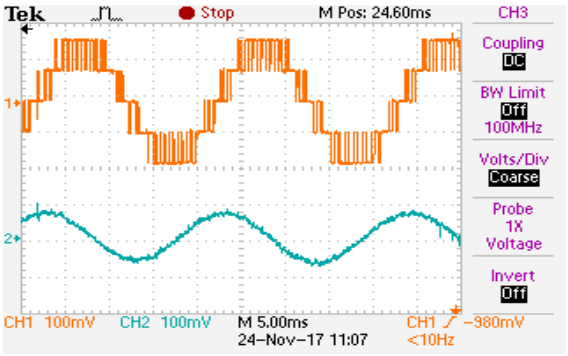


Figure 9. Common Carrier Control Scheme at M_i=0.81: Line Voltage, Stator Current :SVPWM

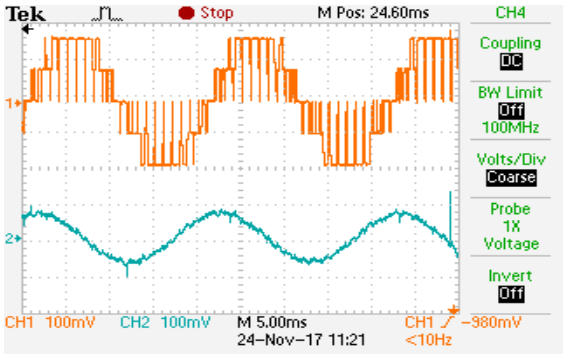


Figure 14. Inverted Carrier Control Scheme at M_i=0.81: Line Voltage, Stator Current :SVPWM

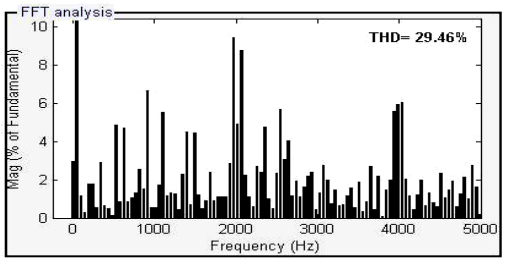


Figure 10. Common Carrier Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

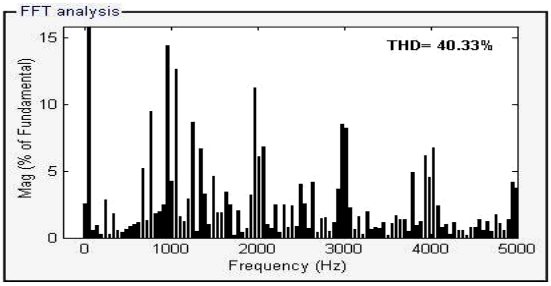


Figure 15. Inverted Carrier Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

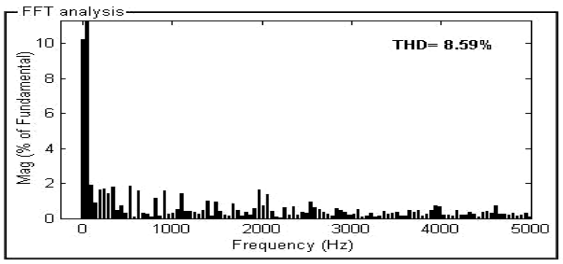


Figure 11. Common Carrier Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

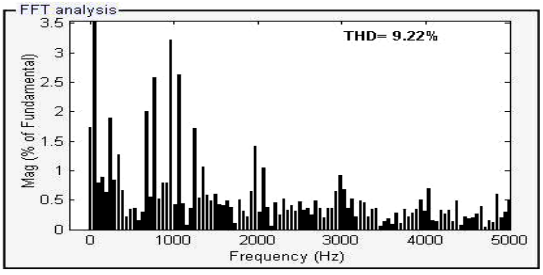


Figure 16. Inverted Carrier Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

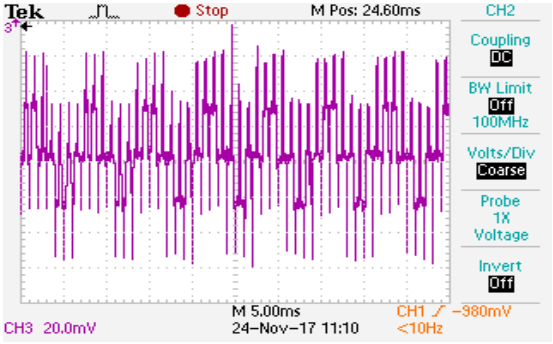


Figure 12. Common Carrier Control Scheme at M_i=0.81: Common mode voltage :SVPWM

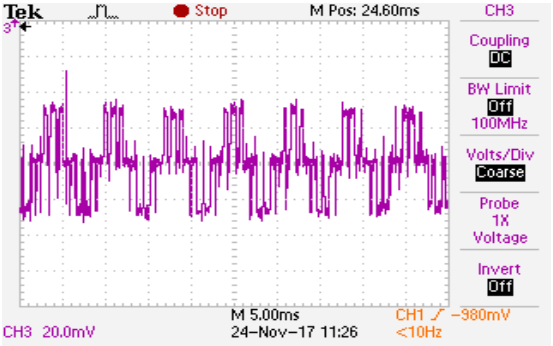


Figure 17. Inverted Carrier Control Scheme at M_i=0.81: Common mode voltage :SVPWM

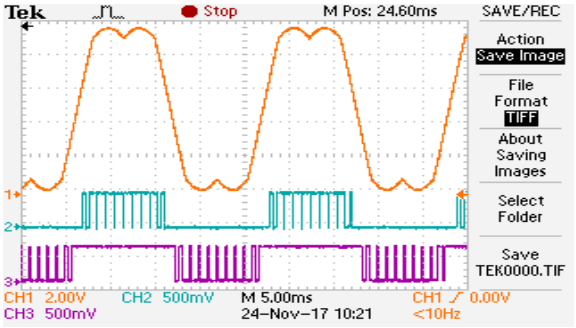


Figure 18. Phase Shifted Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II :SVPWM

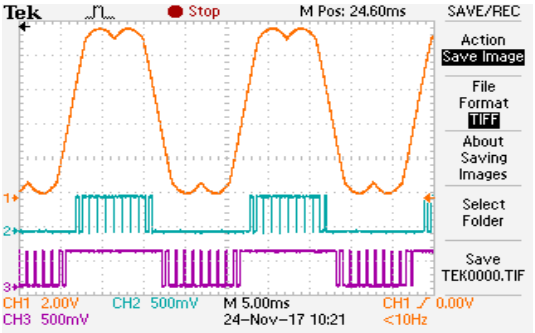


Figure 23. Inverted Phase Shifted Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II :SVPWM

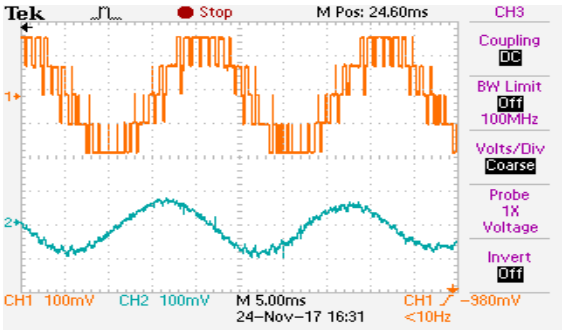


Figure 19. Phase Shifted Control Scheme at M_i=0.81: Line Voltage and Stator Current :SVPWM

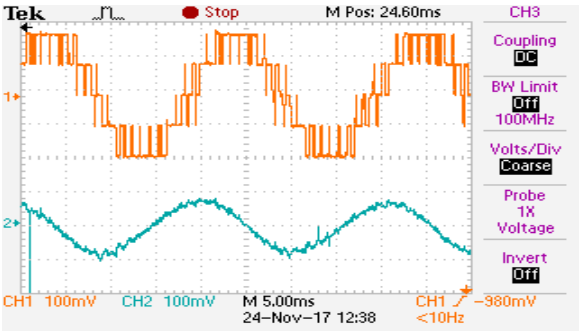


Figure 24. Inverted Phase Shifted Control Scheme at M_i=0.81: Line Voltage and Stator Current :SVPWM

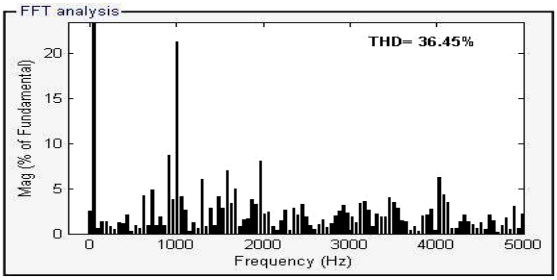


Figure 20. Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

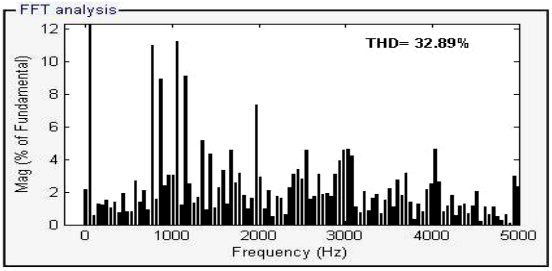


Figure 25. Inverted Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

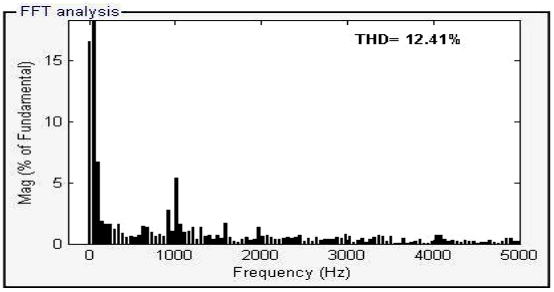


Figure 21. Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

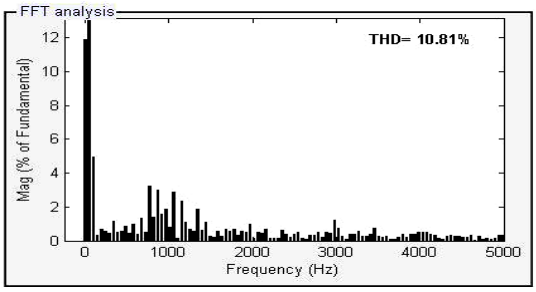


Figure 26. Inverted Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

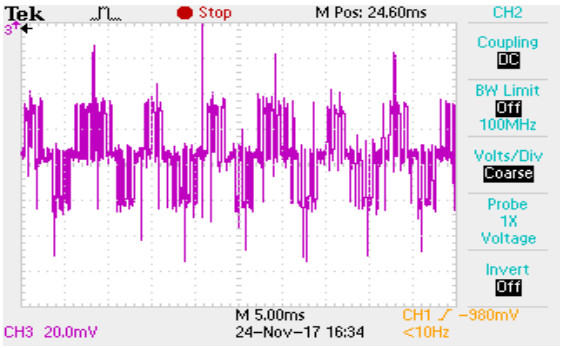


Figure 22. Phase Shifted Control Scheme at M_i=0.81: Common mode voltage :SVPWM

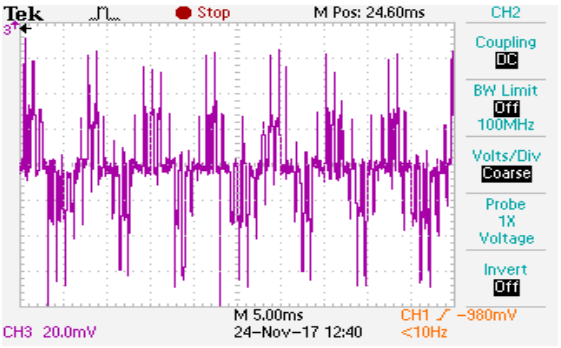


Figure 27. Inverted Phase Shifted Control Scheme at M_i=0.81: Common mode voltage: SVPWM

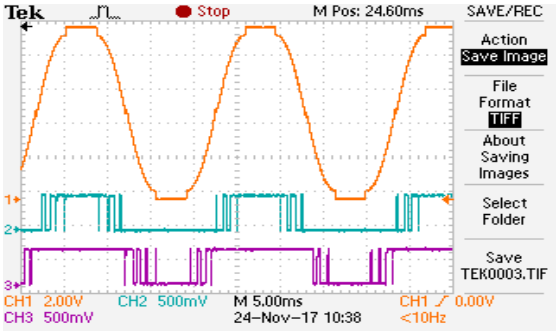


Figure 28. Common Carrier Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II: DPWM

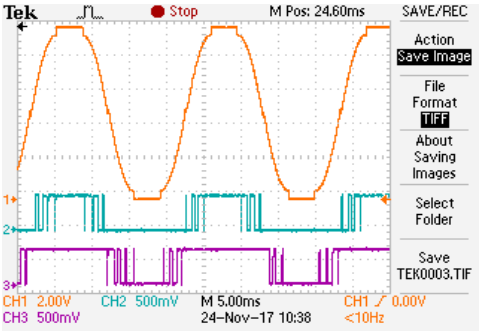


Figure 33. Inverted Carrier Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II :DPWM

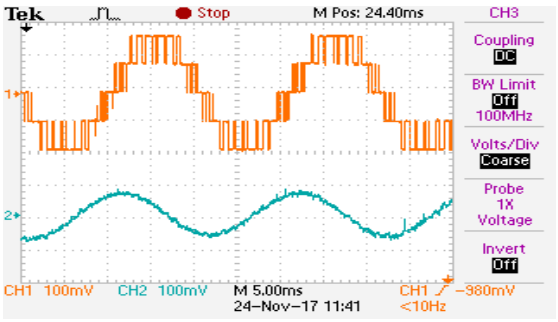


Figure 29. Common Carrier Control Scheme at M_i=0.81: Line Voltage, Stator Current: DPWM

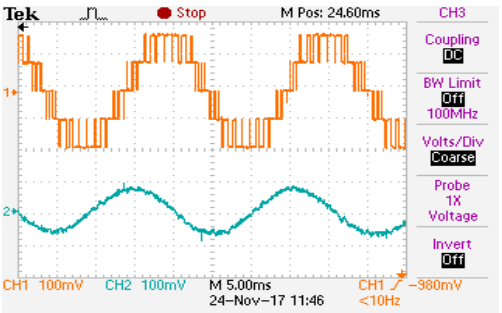
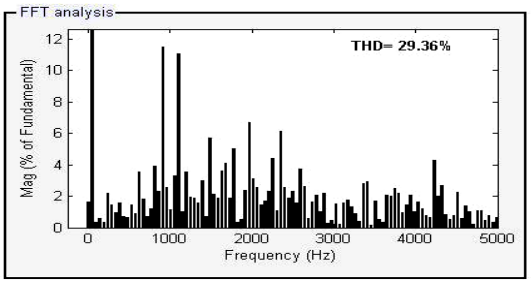


Figure 34. Inverted Carrier Control Scheme at M_i=0.81: Line Voltage, Stator Current: DPWM



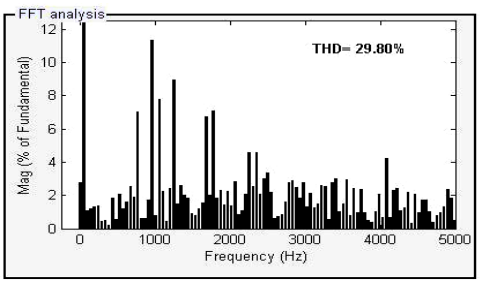


Figure 30. Common Carrier Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

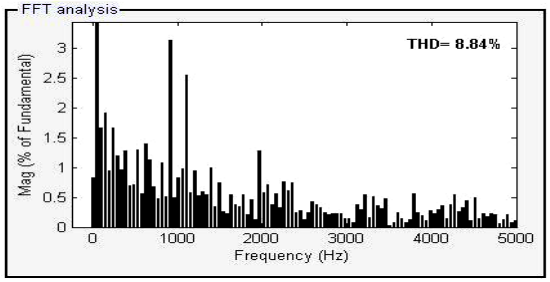


Figure 31. Common Carrier Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

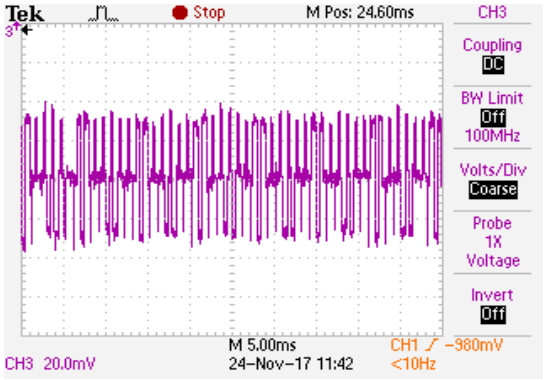


Figure 32. Common Carrier Control Scheme at M_i=0.81: Common mode voltage :DPWM

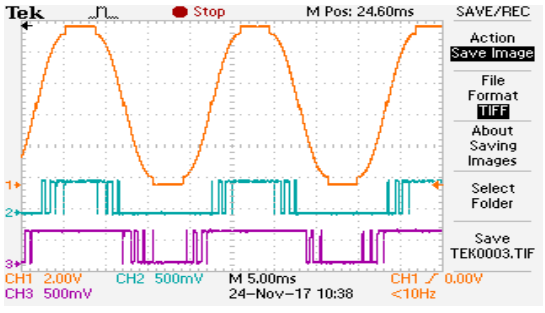


Figure 38. Phase Shifted Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II :DPWM

Figure 35. Inverted Carrier Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

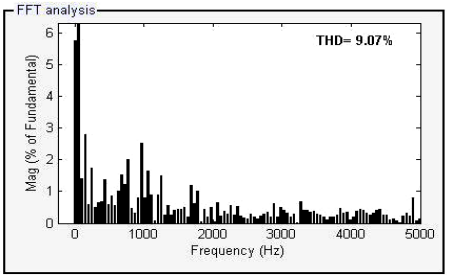


Figure 36. Inverted Carrier Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

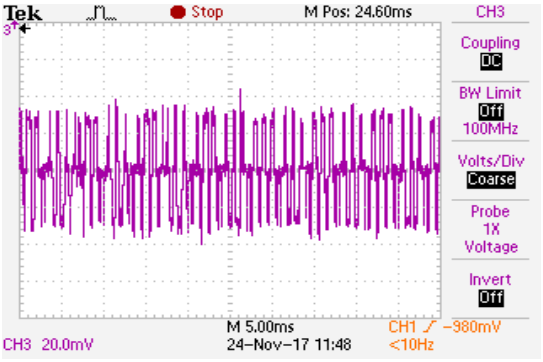


Figure 37. Inverted Carrier Control Scheme at M_i=0.81: Common mode voltage: DPWM

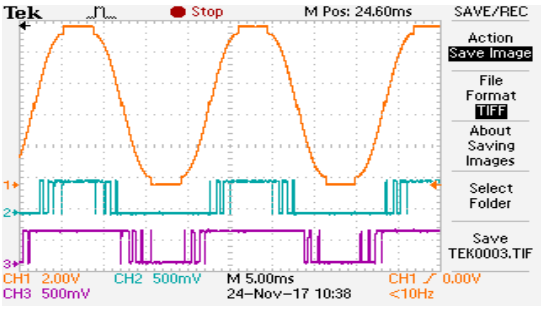


Figure 43. Inverted Phase Shifted Control Scheme at M_i=0.81: Modulating Signal, Pulses for Inverter-I & II: DPWM

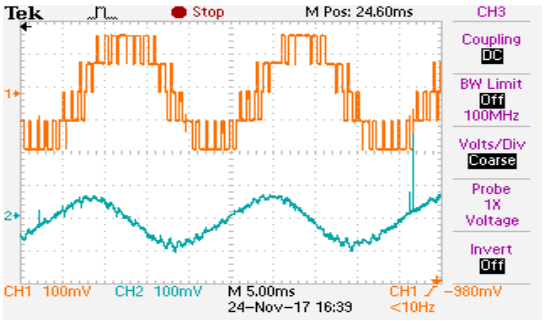


Fig. 39. Phase Shifted Control Scheme at M_i=0.81: Line Voltage and Stator Current :DPWM

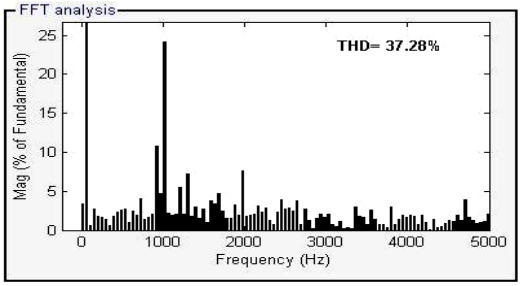


Figure 40. Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

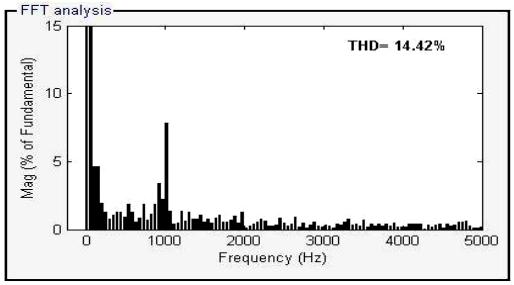


Figure 41. Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

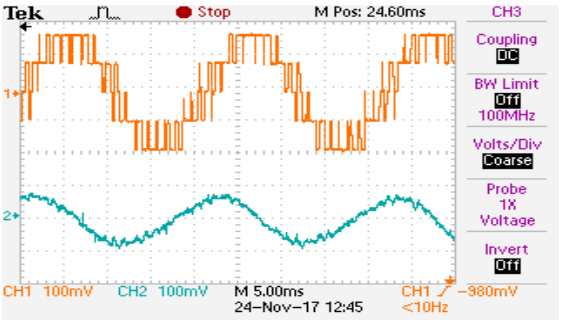


Figure 44. Inverted Phase Shifted Control Scheme at M_i=0.81: Line Voltage and Stator Current: DPWM

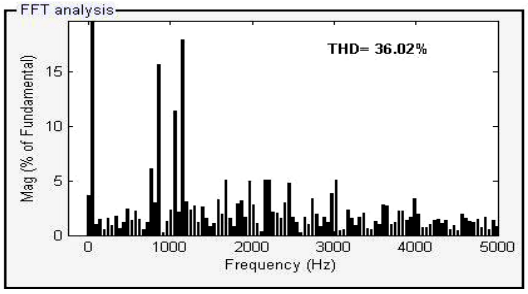


Figure 45. Inverted Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of line Voltage along with THD

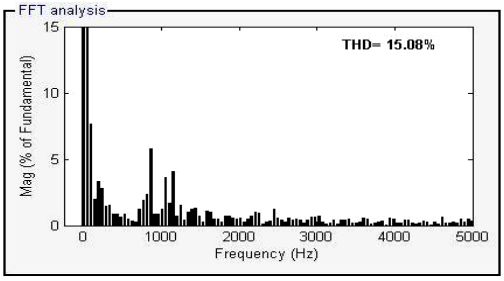


Figure 46. Inverted Phase Shifted Control Scheme at M_i=0.81: Harmonic distortion of stator current along with THD

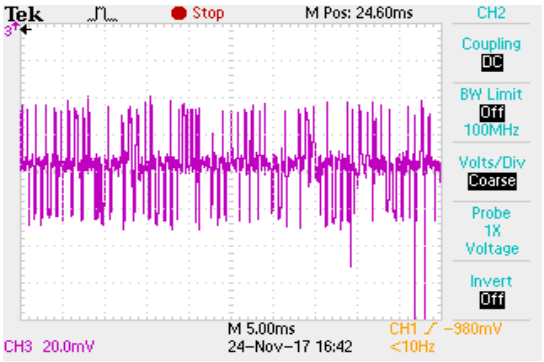


Figure 42. Phase Shifted Control Scheme at M_i=0.81: Common mode voltage :DPWM

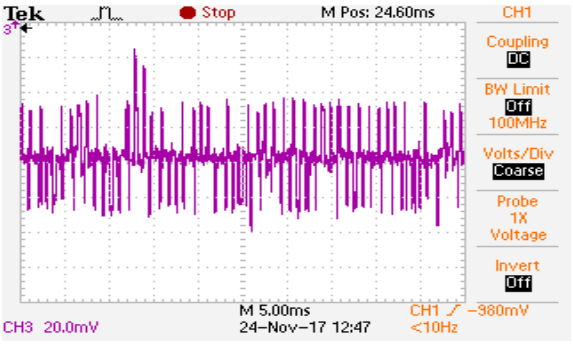


Figure 47. Inverted Phase Shifted Control Scheme at M_i=0.81: Common mode voltage: DPWM

From the experimental results it is observed that with discontinuous modulating signal, the switching of inverter has been reduced as well as its switching losses, as DPWM algorithm clamp for a total period of 120 degrees in each fundamental cycle, the switching losses can be reduced to 33.33%.

As the proposed inverter configuration is capable of generating three level output it is observed in that the effective pole voltage with different PWM algorithms contains three level (0 ,Vdc/2 and Vdc) for an input DC voltage of 540V. Figure 8 to Figure 47 shows eualvation of four various multi carrier control schemes and experimental results shows that common carrier based conventional SVPWM algorithm causes a higher common mode voltage of 2Vdc/3 to -2Vdc/3 (i.e 180Volts to -180Volts) shown in figure 12, which causes motor bearing currents effecting motor performance. However experimental results validates that by using proposed inverted carrier control scheme common mode voltage is reduced from 2Vdc/3 to 2Vdc/6 (i.e 180Volts to 90 Volts). Therefore, the CMV is reduced by 50% with the discontinuous modulating signal based inverted carrier control schemes. The FFT analysis was carried out for the line votage and phase current and the total harmonic distortion (THD) for various control schems is presented and it is observed that among various control schemes, inverter carrier control scheme minizes common mode voltgage with fewer harmonic distortions.

5. CONCLUSION

This paper reviews multi carrier based simplified discontinuous PWM techniques for cascaded three level inverter fed v/f controlled induction motor drive. Space vector approach requires angle and sector information which increases complexity of the algorithm burden on the processor for program execution, but whereas by using carrier comparison approach, the same modulating control signals have been obtained without calculating angle and sector. This can be achieved by adding a zero sequence signal to the sinusoidal reference signals. In this paper four various multi carrier control schemes have been evaluated and experimental results are presented. From the results it is concluded that common carrier control scheme gives fewer harmonic distortion but gives higher common mode voltage 2Vdc/3 which causes motor bearing currents effecting motor performance. More over the proposed later schemes reduce higher common mode voltage from 2Vdc/3 to 2Vdc/6 with less harmonic content. Finally it can concluded that among all the four control schemes inverted carrier control scheme gives lesser harmonic with reduced common mode voltage. This paper also concludes that continuous PWM algorithm give continuous pulse pattern which causes in the increment of switching losses of the inverter, where as DPWM algorithms clamp to either positive dc bus or negative dc bus for a total period of 120^o in every fundamental cycle. Hence, the DPWM algorithms reduce the switching losses of the inverter by 33.33% along with common mode voltage reduction.

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