International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 9, No. 1, March 2018, pp. 231~239
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v9.i1.pp231-239

Performance Analysis of H-bridge and T-Bridge Multilevel Inverters for Harmonics Reduction

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Article Info

Article history:

Received Aug 3, 2017
Revised Jan 5, 2018
Accepted Jan 19, 2018

Keyword:

Cascaded multilevel inverter
H-bridge
Pulse Width Modulation (PWM)
T-bridge
Total harmonic distortion (THD)

ABSTRACT

This paper deals with the design of cascaded 11 level H- bridge inverter. It includes a comparison between the 11 level H-bridge and T-bridge multilevel inverter. The cascaded inverter of higher level is a very effective and practical solution for reduction of total harmonic distortion (THD).These cascaded multilevel inverter can be used for higher voltage applications with more stability. As the level is increased the output waveform becomes more sinusoidal in nature. The inverter is designed using multicarrier sinusoidal pulse width modulation technique for generating triggering pulses for the semiconductor switches used in the device. Through this paper it will be proved that a cascaded multilevel H-bridge topology has higher efficiency than a T-bridge inverter, as whichever source input voltage is provided since input is equal to the output voltage. In T-bridge inverter, the output obtained is half of the applied input, so efficiency is just half as compared to H-bridge. The output waveform is distorted and has higher THD. The simulation is performed using MATLAB /Simulink 2013 software.

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1 INTRODUCTION

Inverters are the electronic devices that convert the direct current power into alternating power by using semiconductor switches like MOSFET, BJT, IGBT, GTO etc. Highly efficient inverters can be used in uninterrupted power supply,high voltage and Medium voltage motor drives, FACTS, tractions, and for harnessing renewable energy like wind, solar etc. but the conventional inverters are very high in cost, their efficiency is poor and they have very high switching losses. These disadvantages can be overcome by using cascaded multilevel inverters and comparison of two PWM techniques [1]. The output waveform of inverter is stepped in nature. Earlier inverters were made up to three levels,but with the advancement and research in the field has led to the development of multilevel inverters of higher orders like 11, 13, 15 and 17. The main advantage of increasing the level is that it eliminates the harmonics and hence is very handy in reducing the total harmonic distortion of the inverter. These inverters can be designed using topologies like diode clamped, cascaded h bridge, flying capacitor topology. Multilevel inverter provides high quality output waveform. The efficiency of these inverters can be enhanced if they are operated at higher switching frequency with lower number of switches in system [2]. Output waveform is generated by using multiple voltage levels that are done by various connections with the load. The various connections with the load is achieved by switching the different MOSFETS at different times. These pulses are generated by many ways, one such way is the sinusoidal pulse width modulation technique. PWM is the process of generation of pulses of constant amplitude. This can be achieved by comparing a carrier wave and the reference wave. The reference wave is of lower frequency and SPWM has a sine wave as reference and a carrier wave of higher frequency. Usually saw tooth or triangular waveform can serve as the carrier signal. When these waves are

passed through some logic comparator constant amplitude pulses are generated, that are used for triggering the semiconductor power switches. The lower order harmonics are eliminated using Artificial Bee Colony (ABC) algorithm with reduced number of switches in the cascaded multilevel inverter proposed [3]. The equal area criterion and harmonics injection are proposed for realizing the two level and multilevel inverter [4]. Total harmonics distortion is reduced by single phase multilevel inverter using various pulse width modulation techniques [5].

In cascaded inverter many single full bridge inverter each having its own dc source are connected in series. This dc voltage can be obtained by using dc battery or renewable sources on the input side. Each of the power switch conduct for a cycle of 180 degrees. The stress on each switch is reduced because of the series connection. Series connection of Two H Bridge inverters is proposed with modified PWM technique, switching losses are reduced with less number of switches [6-7].The emergence of multi-level technology in recent times has served to play an important role in the area of high power medium voltage energy control. This paper presents aa cascaded multilevel inverter which is used to reduce total harmonic distortion. A cascaded multilevel inverter consists of series CB Bridge (single phase, full bridge) inverter units. In order to improve the high power high quality applications of the multilevel topology, the number of switches have been reduced. The proposed method not only produces the variable AC voltage without harmonics but also reduces the no of switches. The simulation has been carried out using mat lab Simulink software [8].This paper presents single-phase cascaded H-Bridge Inverter with minimum number of power electronics devices. Each cell of the proposed inverter consists of 4 unidirectional switches and single bidirectional switch. To generate a multilevel output Single carrier and multicarrier PWM method is used. The proposed multilevel inverter is also compared with conventional symmetrical CHB, Asymmetrical CHB with binary and triple configurations. The comparison is carried out on the basis of number of components, number of DC sources, number of Balancing capacitors, Switching and conduction losses. The proposed Cascaded H-Bridge Inverter is then simulated using MATLAB/SIMULINK and is implemented in hardware using SPARTAN3A DSP. [9]

Despite of cascaded H bridge multilevel inverter structure allowing modularized circuit layout and packaging, it still had the drawback of getting prone to high switching losses due to high switching frequency. This problem could only be rectified by either reducing the number of semiconductor switches or decreasing the number of switching per cycle. This paper presents a 11 level cascaded H bridge inverter feeding RL load, which overcomes the fore said drawbacks along with the advantage of reduced switching losses and lesser harmonic distortion. The proposed asymmetrical H bridge inverter uses lesser number of switches for switching [10]. The unequal voltage sources can help in shaping the inverter output voltage. With proper switching, number of levels can be increased thus reducing the harmonic distortion. In this paper a new topology for multilevel inverter ispresented for the reduction of total harmonic distortion, reduction in switching losses and higher voltage capability by increasing the number of levels using cascaded H bridge technology. It includes design and simulations of 11 level Cascaded H-Bridge and T-bridge Multi-Level inverter using MATLAB SIMULINK software, and comparison of THD level in both the cases. Output voltage levels are produced using multicarrier sinusoidal pulse width modulation technique. Waveform becomes more sinusoidal on increasing the number of levels.

In this paper,chapter II describes about the proposed eleven levels cascaded h bridge inverter. Chapter III delineates the simulation circuits and results of five level, eleven level H Bridge and T bridge inverter. Chapter IV explains about hardware implementation of the project and THD compared with T bridge inverter. Finally it is concluded in Chapter IV.

2 PROPOSED ELEVEN LEVEL CASCADED H-BRIDGE INVERTER

The cascaded multilevel inverters have many advantages over the conventional inverters that use diodes and flying capacitors. Some of the main disadvantages of other topologies like diode clamped and flying capacitor is the charging and discharging of capacitors. The output voltage in these topologies is half of the applied dc input. These inverters have a very low efficiency, i.e. half of H –bridge inverter. Series cascading reduces the stress on individual switches. There is large reduction in noise and electromagnetic interferences. The efficiency of these inverters can be further enhanced by increasing the operating frequency. The proposed model is a type of multilevel inverter designed by the cascading the 5 H-bridge each having its own DC supply .The number of output voltage level in an inverter is given by the equation: N= (2*S+1) where, N= number of levels;S= number of independent dc sources.

So, for an 11 level inverter the number of sources required is five. The inverter is a symmetrical type. The inverter is symmetrical as all the five voltage sources are of equal voltage. The term cascading means that output of the first block is fed as input to the second block. Hence, by combining the various dc

output levels, a stepped output is generated having various dc levels. The number of levels in positive cycle and negative cycles are equal.so, for an eleven level cascaded H –bridge inverter the DC levels are +v,+2v,+3v,+4v,+5v, 0,-v,-2v,-3v,-4v,-5v.The input supply can be provided by using DC supply or DC voltages generated by a step down transformer, and then a diode bridge rectifier to get a pulsating DC and then a filter circuit to eliminate the ripples. This topology is very helpful in harnessing energy from different sources like wind, solar etc. The diagram consists of 5 h bridge and each bridge consists of 4 switches, so total number of switches used is 20 (S1, S2, S3, S4, S5, S6….S19, S20).These switches conduct in various combinations to give nearly sinusoidal waveforms.

2.1. PWM Technique

PWM is process of generating constant amplitude gate pulses which are obtained on comparing a reference signal of fundamental frequency with high frequency carrier wave. Here sinusoidal PWM is done. Thecarrier is a triangular wave and has a higher frequency than the reference signal. Constant amplitude gate pulse is generated by modulating the duty cycle. The required pulse is generated when the reference and carrier waves are fed into comparator and based on the logic given, output is produced. Figure 1 shows the process of generating multicarrier sinusoidal pulse width modulation.

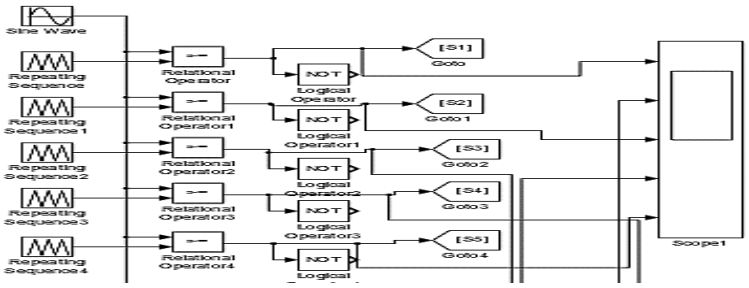

Figure1. Multicarrier SPWM

Table1. Switching Sequence

LEVEL	SWITCH STATES																				OUTPUT VOLTAGE
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	
5	✓	✓			✓	✓			✓	✓			✓	✓			✓	✓			5Vdc
4	✓	✓			✓	✓			✓	✓			✓	✓				✓		✓	4Vdc
3	✓	✓			✓	✓			✓	✓				✓		✓		✓		✓	3Vdc
2	✓	✓			✓	✓				✓		✓		✓		✓		✓		✓	2Vdc
1	✓	✓				✓		✓		✓		✓		✓		✓		✓		✓	Vdc
0		✓		✓		✓		✓		✓		✓		✓		✓		✓		✓	0
-1			✓	✓		✓		✓		✓		✓		✓		✓		✓		✓	-Vdc
-2			✓	✓			✓	✓		✓		✓		✓		✓		✓		✓	-2Vdc
-3			✓	✓			✓	✓			✓	✓		✓		✓		✓		✓	-3Vdc
-4			✓	✓			✓	✓			✓	✓			✓	✓		✓		✓	-4Vdc
-5			✓	✓			✓	✓			✓	✓			✓	✓			✓	✓	-5Vdc

The table 1 depicts the various combinations of switching for generating various output DC levels.

3 SIMULATION RESULTS AND DISCUSSION

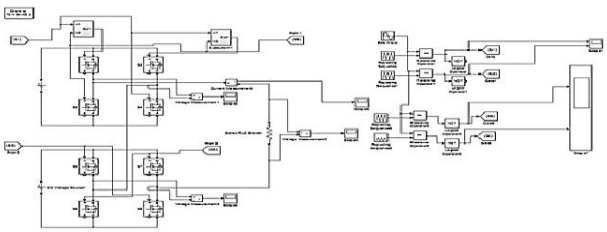

Figure 2. Five Level Cascaded H Bridge Inverter

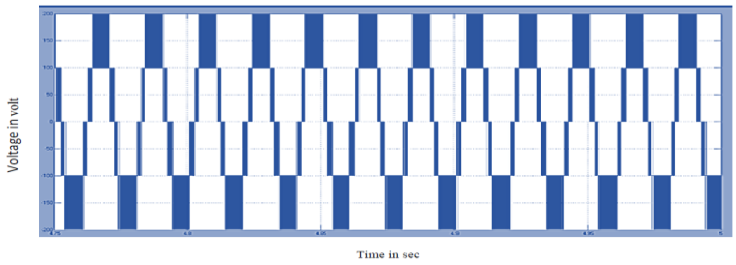

Figure 3.Output Voltage of Five Level Inverter

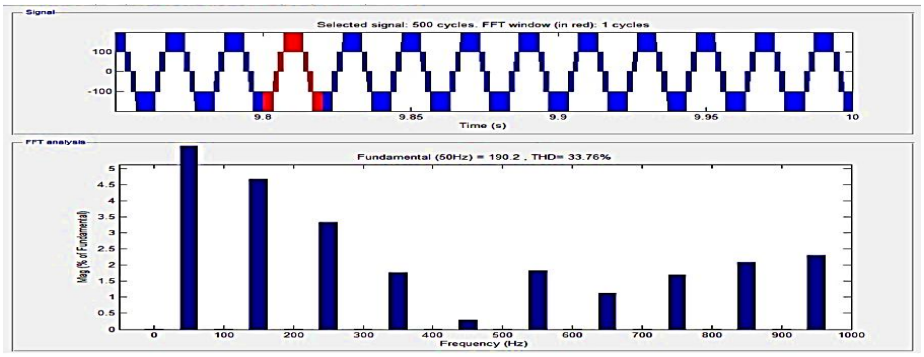

Figure 4. THD of Five Level Inverter

The output voltage of five level inverter is generated in matlab Simulink software is demonstrated in figure 2. Figure 3 shows the graph is plotted between output voltage and time. The output is stepped and consists of 5 levels .From the FFT analysis of five level inverter the total harmonic distortion is 33.76% is shown in Figure 4.

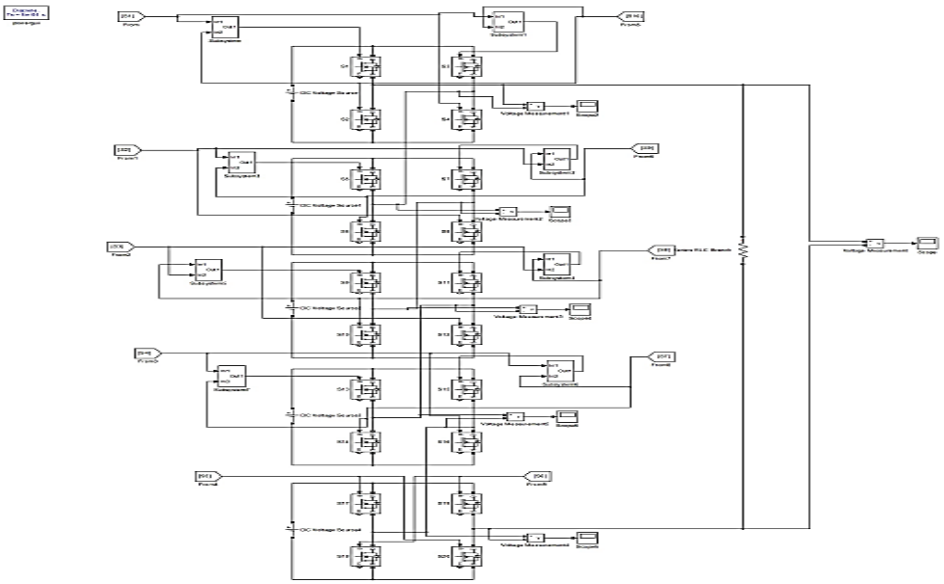

Figure 5. Eleven Level Cascaded H Bridge Inverter

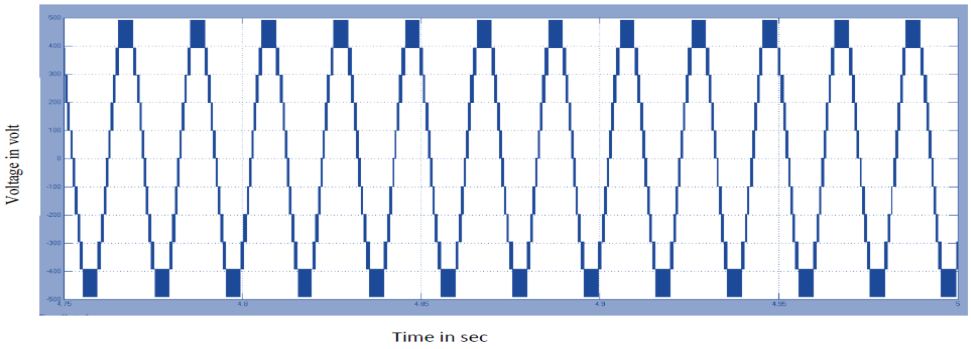

Figure 6. Output Voltage without Filter

The output voltage of eleven level inverter is generated in matlab Simulink software is demonstrated in figure 5. The simulation is carried out for a 11 level inverter and output so obtained is stepped. The graph is plotted between output voltage and time on x axis. The output waveform is generated using matlab Simulink it is demonstrated in Figure 6.

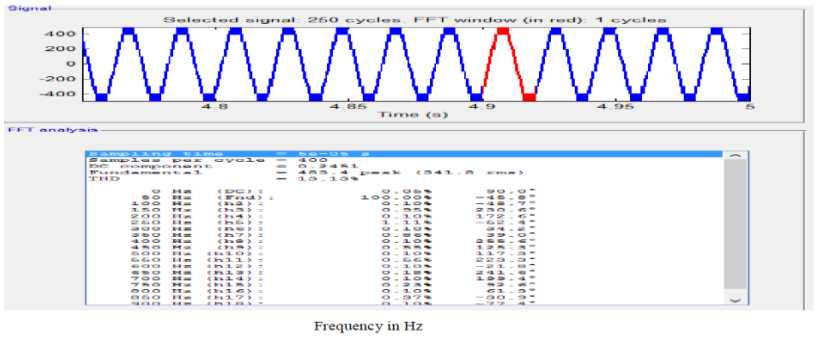

Figure 7. Total Harmonics Distortion without Filter

Since voltage source is of 100 V each, the peak voltage achieved is 500 V. the total harmonic distortion noted for this case is 13.13%. In this type of inverter 3rd, 5th, and 9th harmonics are almost negligibleis depicted in figure 7.

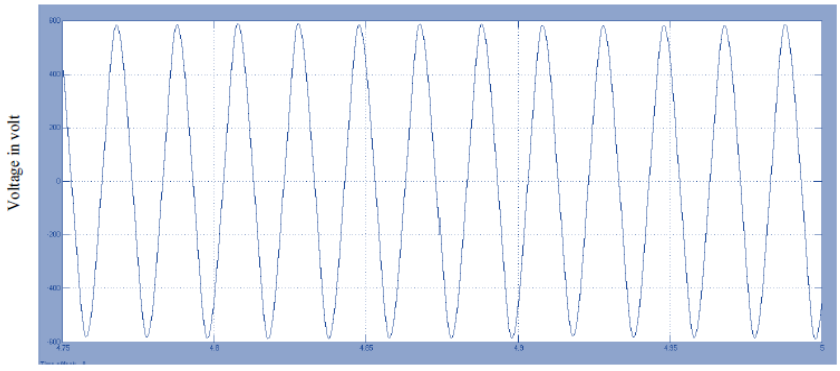

Figure 8. Output Voltage Waveform with Filter

Using filter, a reduction in higher order harmonic problems can be observed, while using a filter in the inverter output side of a three phase will lead toa reduction inharmonics present at the inverter. A pure sinusoidal supply can be given to the drive system by the use of adesigned filter is confirmed in figure 8.

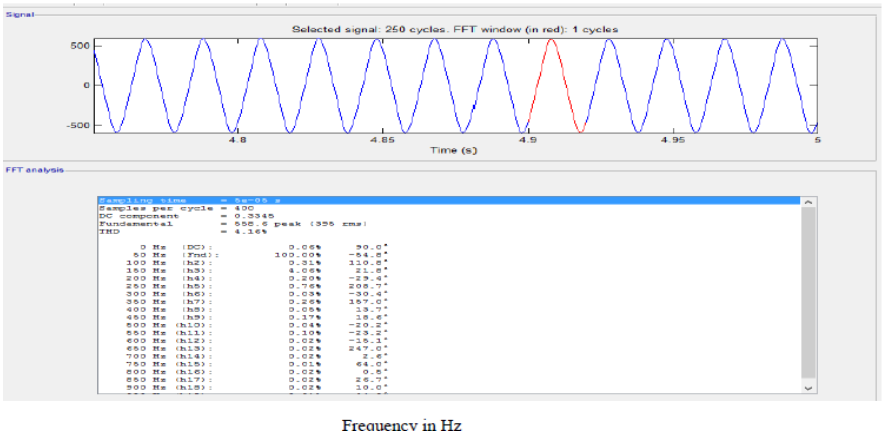

Figure 9. Total Harmonics Distortion with Filter

When a filter is used to determine the total harmonic distortion, a sinusoidal waveform can be achieved from a stepped waveform. The total harmonic distortion reduces below 5% (4.16% precisely). Thus reduction in the level of distortion is in accordance with IEEE standards it is demonstrated in figure 9.

3.1 T BRIDGE INVERTER

These inverters are best suited for low voltage applications. T-bridge inverter hasfewer conduction losses as current is shared between the switches. Here filter ripple frequency is twice the switching frequency due to which less amount of electromagnetic material is required.

Another very important advantage of T-bridge inverter is that it doesn't have diodes and at a time number of conducting switches are less. So, it reduces cost and gives greater efficiency. Simulation of 11 level T type inverter is proved in figure 10.

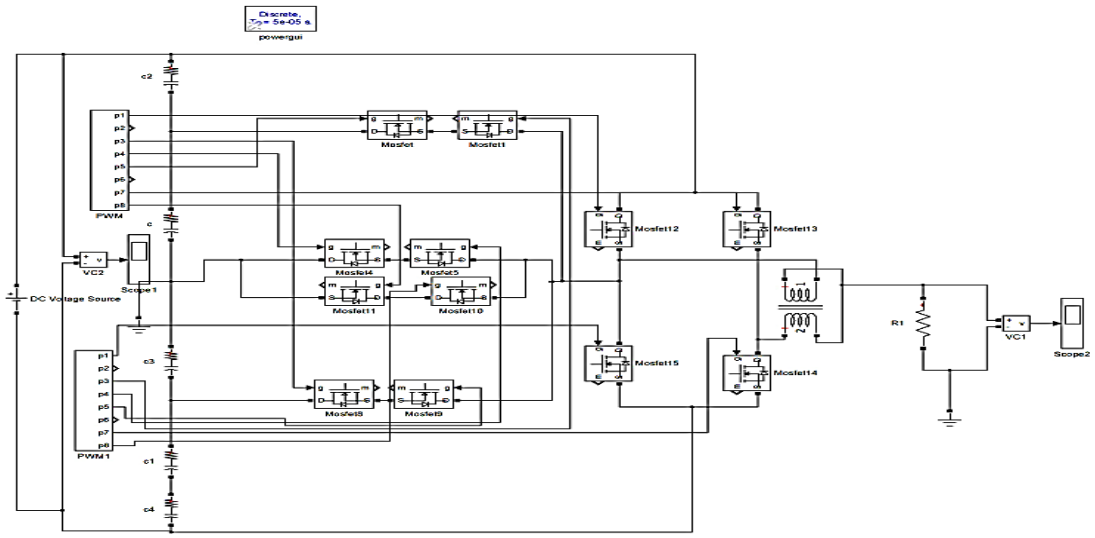

Figure 10.Simulation Diagram for 11 Levels T Type Inverter

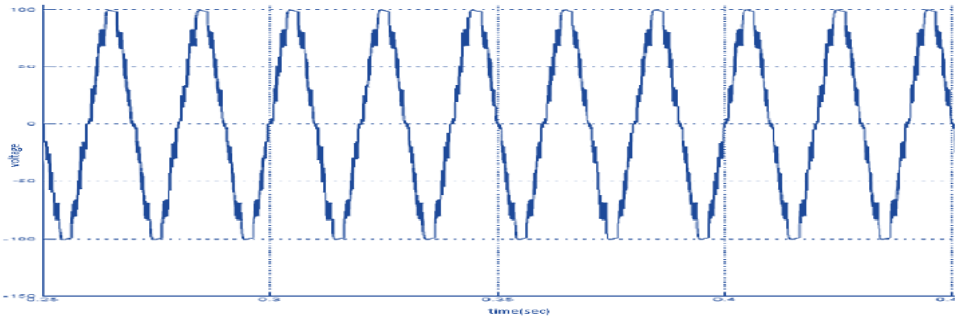

Figure 11. Output Voltage of T bridge inverter

From the simulation results of11 level T type inverter with its output waveformand FFT analysis it has less electromagnetic distortion and less conduction losses due to sharing of current among switches output voltage of t bridge inverter shown in figure 11.

The T-type inverter produces heavily distorted output waveform. The THD component is very high. Even on using suitable filters the THD is near 12%. Whatever input voltage is given only half of that is obtained at the output. It has a big limitation and can only give half of applied voltage. On looking at the FFT analysis to find the THD we can see that multiples of fundamental wave (harmonics) like 3rd, 5th, 9th are present, and can further raise many other power quality issues it is proved in figure 12.

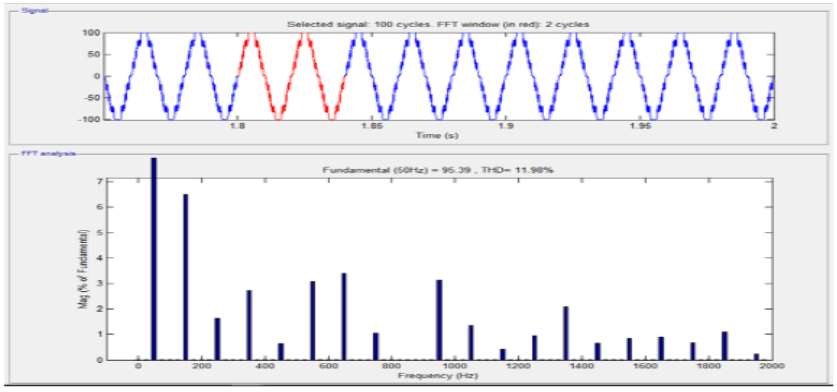

Figure 12. THD of T bridge inverter

The simulation of a 5, 11 level inverter and a conventional T bridge inverter is carried out using mat labSimulink. The outputs were compared and hence it was concluded that a 11 level cascaded H bridge inverter has reduced harmonics.The reduced THD in the conventional was found to be 5.76% [10]and 4.6%, where as in the proposed configuration the THD is 4.16%.

Table 2:Comparison of T and H Bridge Inverter

H-BRIDGE	T-BRIDGE
1) The maximum output voltage is equal to the supplied input. 2) Efficiency is high as compared to T Bridge. 3)THD of system for 5 level is13.13% and for 11 level h bridge with filter is less than 5%.(within IEEE standards) 4)Output waveform is sinusoidal with elimination of 3, 5, 7, 9 harmonics.	1)The maximum output voltage is half of the input supplied. 2)Relative Efficiency is only 50 %. 3)THD of the system for T bridge 11 level inverter is 11%. 4)Output waveform is distorted and large number of harmonics are present.

From the simulation results of11 level T type inverter with its output waveformand FFT analysis, it is concluded that a T bridge inverter has less electromagnetic distortion. In addition to this, it also has less conduction losses as it shares the current among switches.

4 HARDWARE DESIGN

The hardware design of the inverter is split into four major parts. These are driver section, microcontroller section, converter section and inverter section. The switching device used is MOSFET IRF840 because of its lower internal resistance and very small propagation delay. The driver circuit consists of optocoupler TLP250, which acts as an amplifier and an interface between different voltage levels. The microcontroller used is DSPIC30F2010 which is a 16 bit microcontroller. It operates at a dc voltage of 5V. So, for providing 5V dc, voltage regulator LM7805 IC is used. The total number of switches used is 9. Out of these 5 switches act as converters and 4 act as inverters. The block diagram is shown in Figure 13.

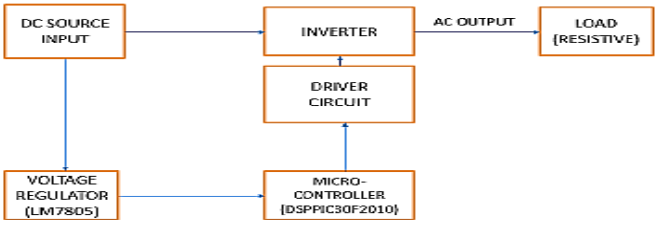

Figure 13. Block Diagram for Hardware Design

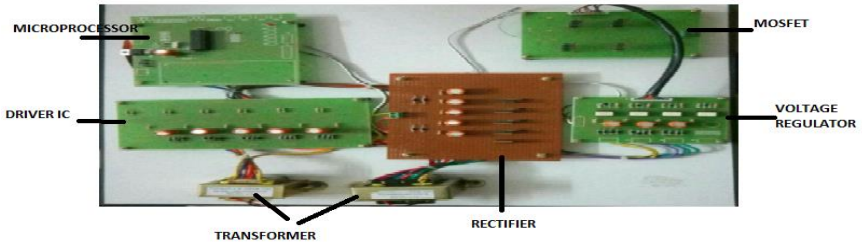

Figure 14. Hardware Design of Eleven level H-Bridge Inverter

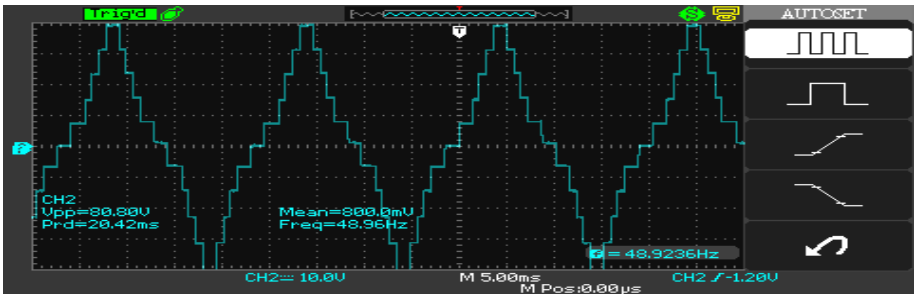

Figure 15. Output voltage of eleven level H-Bridge inverter

Hardware design eleven level H-bridge inverter is confirmed in figure 14. The figure 15 shows the output waveform that is generated from hardware design implementation. The graph is between output voltage and time. The output consists of 11 levels and is stepped.

5. CONCLUSION

H-bridge topology has many advantages when compared to T level. At higher level, it has low total harmonic distortion, reduced stress on switch, and high voltage compatibility. The waveform generated is sinusoidal to a large extent. The efficiency of H-bridge is more than T-bridge as whatever input voltage is applied at input side appears at output, ideally making it twice more efficient. This make it best ideal solution for High voltage dc transmission, Flexible AC transmission system (FACTS), Traction Utility, interface for renewable energy systems.

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