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# Analysis of series/parallel multilevel inverter with symmetrical and asymmetrical configurations

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**ABSTRACT**

Usage of high power and medium voltage applications in domestic and industrial purpose has been increased in the recent years. Also, the penetration of renewable energy sources is increasing rapidly. To make use the renewable energy sources there is a need of using inverters. The basic inverter is conventional two level inverter which produces the square wave output voltage. The major drawback of conventional inverter is it contains more harmonics. Therefore, multilevel inverters have been introduced with staircase output voltage waveform. Lot of multilevel inverter topologies have been developed and cascaded H bridge type is the more frequently used. But, it requires more number of switches for higher output voltage level. In this paper, a novel 7 level asymmetrical multilevel inverter topology is proposed with less number of switches. This proposed topology is compared with already existing topology. The simulation of circuit and result analysis of the circuit is carried out by using Matlab/simulink software. The comparison between existing topology and proposed topology is given. The results are discussed and presented.



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## 1. INTRODUCTION

Country's electrical energy demand is more than the electrical energy generated and at the same time fossil fuel supply is being decreased. Therefore, the research has been started towards alternative energy sources and the outcome is renewable energy sources (RES) [1]-[4]. Solar, wind and fuel cell are the most commonly used renewable energy sources. The power produced from these energy sources is known as distributed generation (DG) [5]-[7]. The DG system can be employed at load centers and therefore, the transmission cost of power will decrease. At the same time, the demand for power electronic converters also has been increased because; the energy generated from renewable energy source is not enough to connect directly to the load or grid. The DC voltage produced from the renewable energy source must be converted to AC to connect it to the grid. For this purpose, inverters are used and the basic inverter is two level inverter. This inverter produces the square wave output voltage which has more harmonic distortion. These harmonics causes for parasitic torques in case of electrical machines and produce more amount of heat losses. Hence to overcome these drawbacks, multilevel inverter topologies have been introduced and developed.

These multilevel inverters have got more attention due to their advantages. The multilevel inverter produces very low harmonic distortion in the output voltage waveform, the rate of rise of voltage (dv/dt) is less and it draws current with low ripple content when used for drives applications. There have been lot of multilevel inverter topologies developed like diode clamed, flying capacitor type and cascaded H bridge (CHB) [8]-[11] multilevel inverter topology. Out of these, the diode clamped and flying capacitor type requires more number of diodes and capacitors respectively and cascaded H bridge type is the most

commonly used. In cascaded H bridge number of levels can be obtained by using the formula 2n+1, here n is the number of H bridges. As the number of levels increased the H bridge count also increases which leads to increase the switching components. Hence, multilevel inverter topology must be optimized in such a way that it should give more number of levels with less components, In this paper, a novel asymmetrical series/parallel multilevel inverter topology has been proposed with less number of switches and is compared with already existing symmetrical series/parallel multilevel inverter topology. The proposed inverter requires 7 switches with two DC voltage sources. The total work is carried out by using Matlab/simulink software and the results are presented. The comparison is also given for existing and proposed topology.

## 2. 7 LEVEL SYMMETRICAL SERIES/PARALLEL CONFIGURATION

Seven level symmetrical series parallel multilevel inverter configuration is shown in Figure 1. In this configuration three DC voltage sources of same magnitude is considered. Eight switches are required to get 7 level output voltage. The switching sequence for 7 level symmetrical configuration is shown in Table 1. By operating the switches in proper manner, the seven level output voltage is obtained.

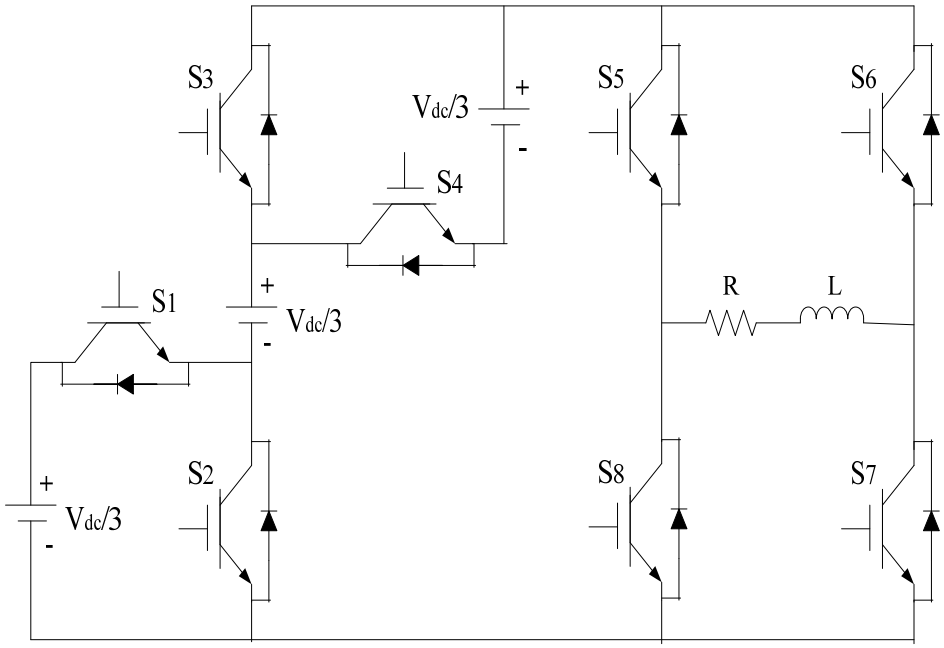


Figure 1. 7 Level symmetrical series/parallel inverter configuration

Table 1. Switching Sequence

| VOLTAGE LEVEL | SWITCHING SEQUENCE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ |
| 0 | OFF | OFF | OFF | OFF | ON | ON | OFF | OFF |
| $V_{DC}/3$ | OFF | ON | ON | OFF | ON | OFF | ON | OFF |
| $2V_{DC}/3$ | OFF | ON | OFF | ON | ON | OFF | ON | OFF |
| $V_{DC}$ | ON | OFF | OFF | ON | ON | OFF | ON | OFF |
| $-V_{DC}/3$ | OFF | ON | ON | OFF | OFF | ON | OFF | ON |
| $-2V_{DC}/3$ | OFF | ON | OFF | OFF | OFF | ON | OFF | ON |
| $-V_{DC}$ | ON | OFF | OFF | OFF | OFF | OFF | OFF | ON |

## 3. 7 LEVEL ASYMMETRICAL SERIES/PARALLEL CONFIGURATION

The asymmetrical series parallel configuration for seven level is shown in Figure 2. In this configuration, two DC voltage sources of different magnitude (Vdc and 2Vdc) are considered. Seven switches are required to generate seven level output voltage. Table 2 gives us the switching pattern for 7 level asymmetrical configuration. By switching ON and OFF the different switches in a proper manner the seven level output voltage is obtained.

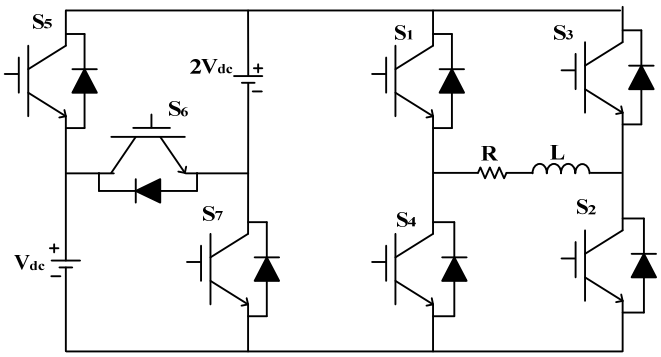


Figure 2. 7 Level asymmetrical series/parallel inverter configuration

Table 2. Switching sequence

| VOLTAGE LEVELS | SWITCHING SEQUENCE | | | | | | |
|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ |
| $3V_{dc}$ | ON | ON | OFF | OFF | OFF | ON | OFF |
| $2V_{dc}$ | ON | ON | OFF | OFF | OFF | OFF | ON |
| $V_{dc}$ | ON | ON | OFF | OFF | ON | OFF | OFF |
| 0 | OFF | ON | OFF | ON | OFF | OFF | OFF |
| $-V_{dc}$ | OFF | OFF | ON | ON | ON | OFF | OFF |
| $-2V_{dc}$ | OFF | OFF | ON | ON | OFF | OFF | ON |
| $-3V_{dc}$ | OFF | OFF | ON | ON | OFF | ON | OFF |

## 4. SIMULATION RESULTS

### 4.1. 7 level symmetrical series/parallel configuration

**Case1: R Load**

The output voltage waveform is shown in Figure 3. The magnitude of voltage is 300 volts. Figure 4 shows the output current wave form.

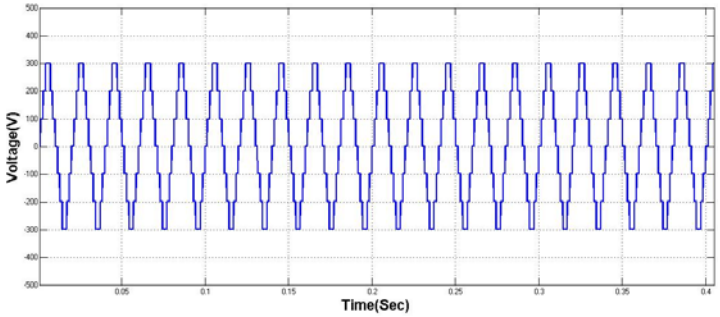


Figure 3. Output voltage

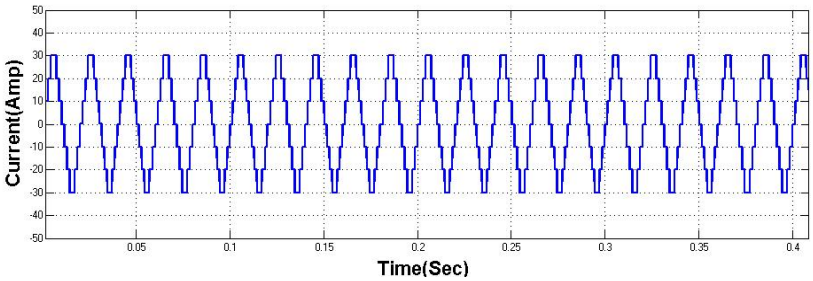


Figure 4. Output current

**Case 2: RL Load**

Output voltage of RL load is shown in Figure 5. The output current of RL load is shown in Figure 6. The total harmonic distortion for output voltage of RL load is shown in Figure 7. The measured value of THD is 30.28%.

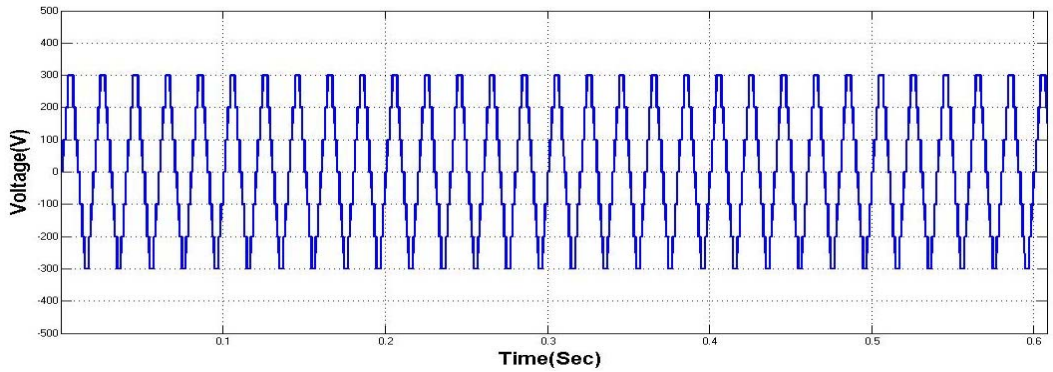


Figure 5. Output voltage

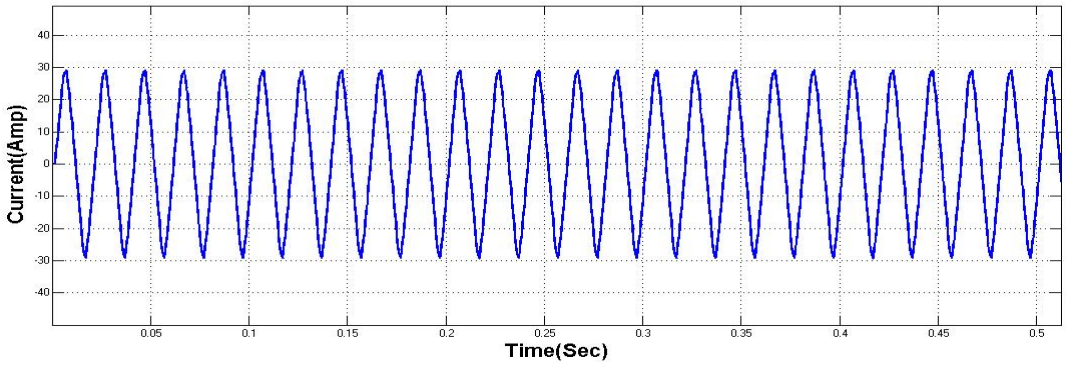


Figure 6. Output current

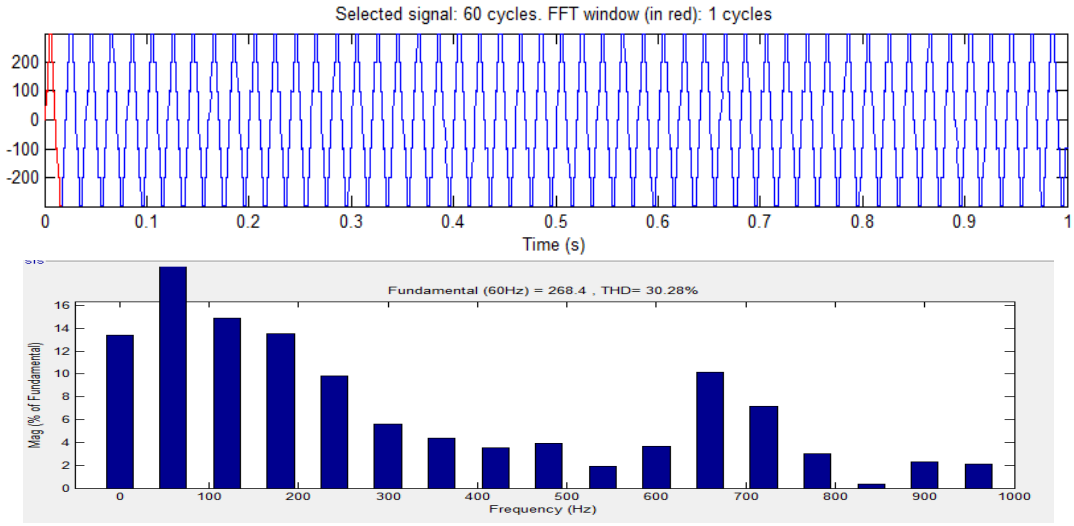


Figure 7. THD of output voltage

### 4.2. 7 level asymmetrical series/parallel configuration

**Case1: R Load**

The output voltage is shown in Figure 8 and the magnitude of voltage is 300 volts. The output current is shown in figure 9. The amplitude of current is 30 amps.

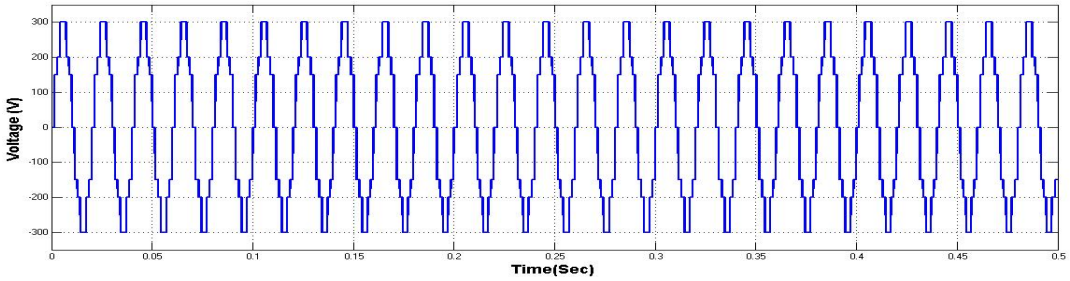


Figure 8. Output voltage

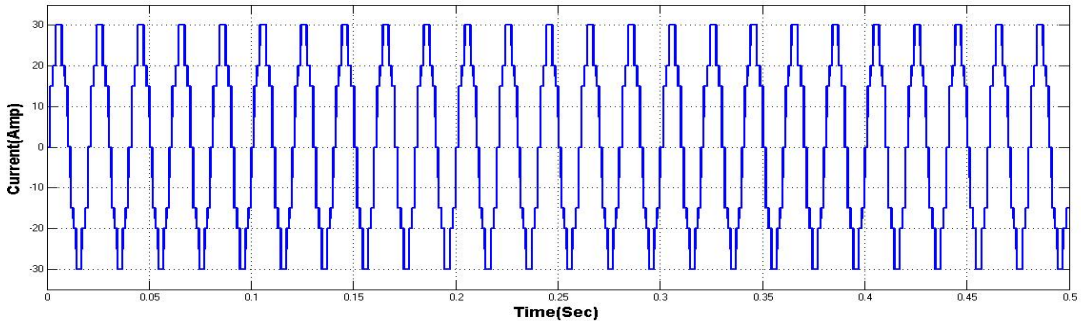


Figure 9. Output current

**Case2: RL Load**

Figure 10 shows the output voltage waveform with a magnitude of 300 volts. Figure 11 shows the output current waveform with a magnitude of 30 amps. The total harmonic distortion is measured for the output voltage and the measured value is 30.26%. The comparison table between symmetrical and asymmetrical series/parallel configuration is shown in Table 3.

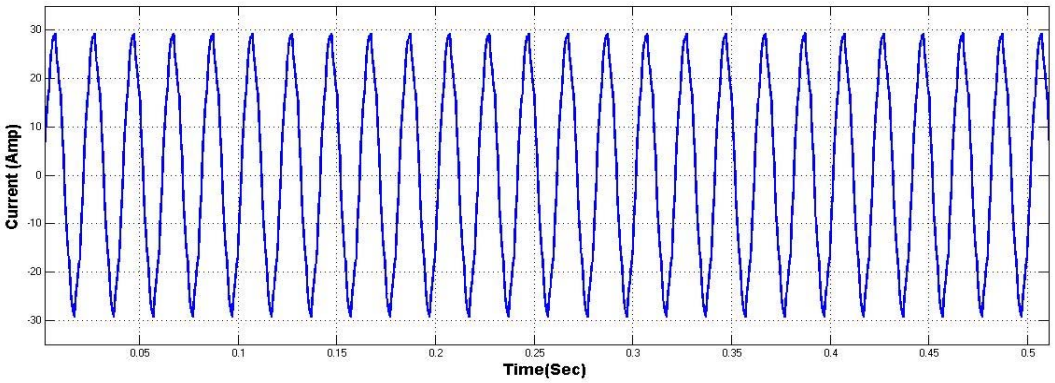


Figure 11. Output current

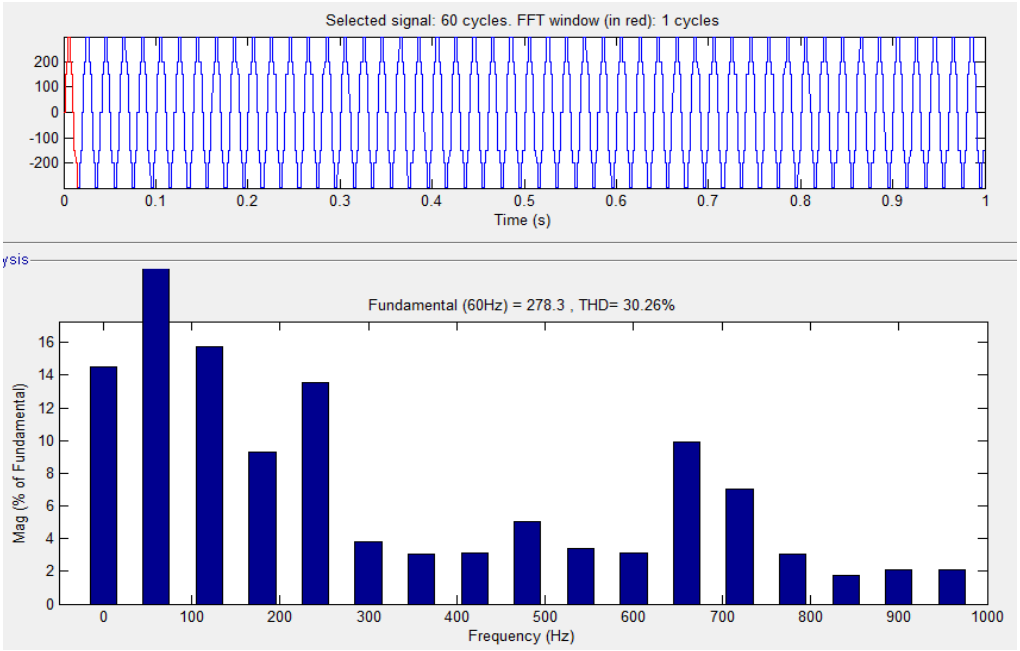


Figure 12. Output voltage THD

Table 3. Comparison Table

| Configuration | Number of switches | Number of gate driving circuits | Number of extra diodes | Number of voltage sources |
|---|---|---|---|---|
| Symmetrical Series/parallel | 8 | 8 | Nil | 3 |
| Asymmetrical Series/parallel | 7 | 7 | Nil | 2 |

## 5. CONCLUSION

In conclusion, it is firmly concluded that the asymmetrical series/parallel multilevel inverter configuration requires 7 power semiconducting switches, 7 gate driver circuits and only two DC voltage sources which are less when compared to symmetrical series/parallel multilevel inverter configuration. In this paper, both symmetrical and asymmetrical series/parallel configurations are explained and analysis is done. The total work is carried out by using Matlab/simulink software. The analysis is done for both resistive and resistive-inductive load. The seven levels of output voltage has been obtained with a magnitude of 300 volts and a nearly sinusoidal waveform for RL load is obtained with a magnitude of 30 amps. The total harmonic distortion for output voltage is measured. As the voltage levels are same the THD for both the configurations has got same value of 30.26%.

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