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Development of Compact Pulse Generator with Adjustable Pulse Width for Pulse Electric Field Treatment Technology

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ABSTRACT

The pulse generator which has been implemented in the pulse electric field (PEF) treatment system for food processing is worth to be highlighted and improved. It is parallel with the advancement in semiconductor technology, which offers robust and accurate devices. This research is an effort to produce a low cost, compact and reliable pulse generator as well as equipped with a pulse width modulation (PWM) method for wide selection of frequency and duty cycle. The result shows that the simulation process has proven the theoretical concept to be right and yields the desired outcome based on the designed values. Then, the actual printed circuit board (PCB) has been fabricated to obtain practical results which intended to be compared with the simulation outcomes. Concerning the frequency and its duty cycle, both parameters can be altered without affecting each other. It means by changing the frequency, duty cycle remains the same and vice versa. Thus, this proposed pulse generator achieves its objective and fits to be implemented in PEF treatment technology. It also can replace the conventional pulse forming network (PFN) which is bulky and costly.

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1. INTRODUCTION

The advancement in semiconductor technologies have driven the research towards the production of precise and robust electronic components. This will benefit the researchers in particular area such as power electronic to innovate an existing equipment to be more up-to-date in coping with the current demand. It also helps to acquire compact and light devices that easy to be mobilised if wanted. For that reason, it is worth to improve the pulse generators in pulsed electric field (PEF) treatment technology as it will help to improve its efficiency in producing accurate output.

PEF is a nonthermal method which uses short pulses of electricity (microseconds to milliseconds) and intensity in the order of 10 – 80 kV/cm to inactivate the food borne pathogens and spoilage microorganisms, while greatly in preserving the quality attributes of the food [1-3]. Minimum detrimental changes on the physical properties (e.g. flavour, colour and nutritional values) are obtained via this technique as the heat is maintained at ambient and slightly above ambient [4, 5]. Therefore, the food with fresh-like look and healthy is possible to be acquired.

Typical components comprised in complete PEF treatment technology are pulse generator, a fluid handling system, treatment chamber, high voltage supply and control and monitoring system [6-8]. However, the pulse generator is highlighted as a main topic of discussion as it owns a capability to generate various pulse shape (e.g. exponential decay, square, bipolar fashions and oscillatory) [9, 10]. The studies that have been done by the researchers around the globe have shown that square pulses are superior to the exponent

decay, while the oscillatory shape is still in question [11, 12]. Figure 1 shows the preview picture of complete PEF system which has been practiced by the fellow researchers.

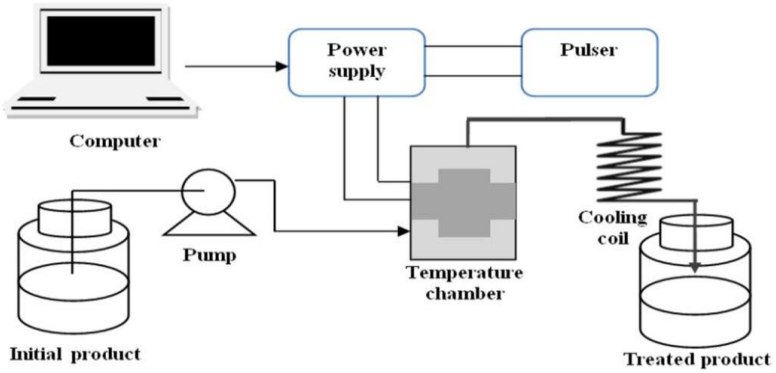


Figure 1. A complete PEF treatment system for continuous type treatment chamber [1]

2. SYSTEM DESIGN

The first step in the making of this pulse generator is shaping its objective, then followed by the next step which is to discover appropriate devices. The third step is to design the circuitry system that parallels with the set objectives and after the design process completed, it moves to the simulation step for testing purpose and record the output. After all the steps have been fulfilled and satisfied with the result generated, it is time to fabricate the circuit and produce the final product.

2.1. Objective

The objective of this study was to develop a compact and low-cost pulse generator which equipped with PWM method that can be operated using 5 VDC supply. In addition, the frequency and duty cycle of its output (monopolar square pulse) can be altered independently; the frequency can be adjusted up to 3 MHz and duty cycle can be changed in the range of 10% - 90% of full cycle.

2.2. Appropriate devices

There are many ways to produce pulse generators, however specifications, size and price make them different from each other. To produce a monopolar square pulse shape, 555-timer IC, LCM555 by Texas Instruments was selected as it can yield stable and steady output signal. The frequency can be adjusted as high as 3 MHz and suitable to be implemented as a pulse generator. It also owns a capability to perform in two modes operation; monostable and astable. The size of the product was small enough (10.16 mm × 10.92 mm) and make the operating circuit compacted to a reasonable dimension by using through-hole component.

2.3. Circuit design

A single 555-timer IC has a limitation where the frequency of its output cannot be altered without affecting the duty cycle or vice versa. This is the drawbacks that need to be solved so that the use of the PWM method can be successfully implemented in the pulse generator. To clear this issue, two units of 555-timer IC were suggested. For better clarification, the construction of the pulse generator is consisted of two parts; the first part is called as a frequency provider and the second part are known as a duty cycle adjuster.

Since 555-timer can be operated in astable mode (as shown in Figure 2), the Trigger and Threshold terminals are connected so that the device can trigger itself and free run as a multivibrator. To charge the external capacitor, the currents need to flow through R_A and R_B from V_S while for the discharge process, the currents flow from the external capacitor and sink to the Discharge terminal via R_B. In this mode of operation, the charges and discharges voltage of the capacitor is between 1/3 V_S and 2/3 V_S.

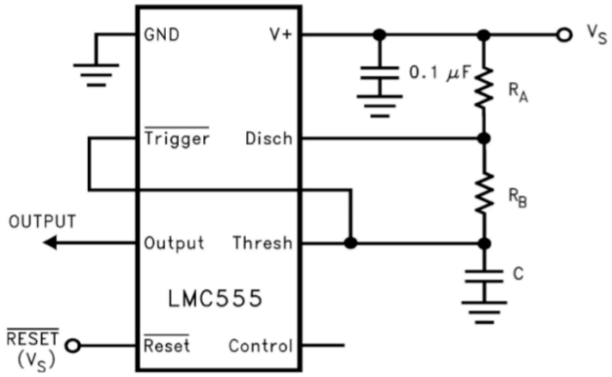


Figure 2. 555-timer circuit configuration in astable mode [13]

As the device triggered itself due to the signal which connected to the Trigger terminal, it is very useful to set it as a frequency provider. The duty cycle of this output was set to 90% to ensure the duty cycle of the pulse generator's final signal can be varied up to 90% (max) of a full cycle. In the device datasheet, it provides a set of equations to determine frequency and duty cycle, which depend on the value of resistors and external capacitor that will be used to adjust the charging and discharging times.

The charge and discharge time are given by:

$$t_c = 0.693(R_A + R_B)C \quad (1)$$

$$t_d = 0.693(R_B)C \quad (2)$$

Thus, the total period and frequency are defined as:

$$T = t_c + t_d = 0.693(R_A + 2R_B)C \quad (3)$$

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

The percentage of duty cycle, as a fraction of total period that the output is high, is:

$$D = \left(\frac{R_A + R_B}{R_A + 2R_B} \right) \times 100 \quad (5)$$

For the second part of the 555-timer IC, it was set to work as a duty cycle adjuster and received a signal on its Trigger terminal from frequency provider's output. This mode of operation is known as monostable and only drive the output high upon application of a negative trigger pulse signal of less than 1/3 V_S. To synchronize its frequency to be equal for both parts, they must share the same value of external capacitor. Figure 3 depicted the LMC555 IC in monostable mode, it consists of one unit of resistor and capacitor only. Noted that in the discharge process, the currents are sink directly to the Discharge terminal.

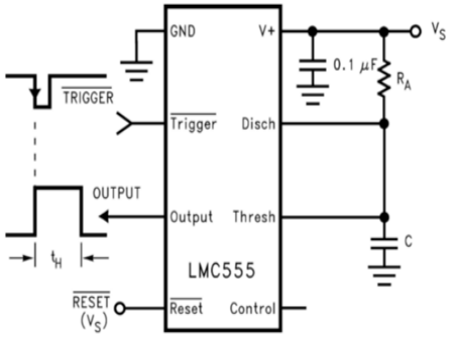


Figure 3. 555-timer circuit configuration in monostable mode [13]

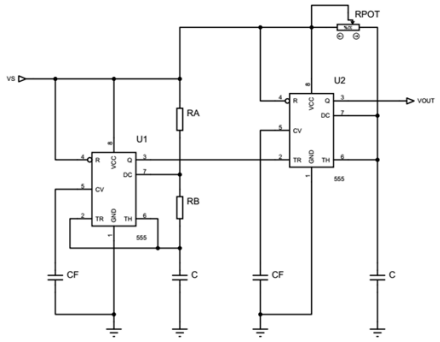


Figure 4. A complete circuit that comprise both parts to form a whole pulse generator

The voltage across the capacitor is increased in exponential order as it is being charged by V_S via R_A. During this time, the output remained high and at the end of which time the voltage equals 2/3 V_S, the capacitor starts to discharge and drive the output to its low state. To ensure it can perform as a duty cycle adjuster, one of the passive components is made variable. However, the resistor in the circuitry system was set to be variable so that it can be adjusted to a specific value to get the desired result. For this mode of operation, R_A and external capacitor are related to each other as depicted in equation (6).

The time when the output stays high is given by:

$$t_h = 1.1 \times R_A \times C \tag{6}$$

Figure 4 shows the complete circuit of the pulse generator that has been designed by using Proteus 8.5 software. The design comprises for both parts; frequency provider and duty cycle adjuster. As can be seen, the output of the first part is directly connected to the Trigger terminal of the second part to form a complete pulse generator. The aim is to embed the PWM method to achieve the capability of altering the frequency and duty cycle independently.

3. RESULTS AND ANALYSIS

In this section, the obtained results are discussed in details so that good comprehension about the circuit mechanisms and its performances can be harvested. To achieve such objectives, the results are represented in several of subsection as follows.

3.1. Calculation results

Before fabricating the actual circuit, simulation process needs to be completed in the first place so that the development cost can be reduced and lowering the human error in designing the circuit. The simulation parameters such as the value of passive components are prerequisite to be determined so that simulation process can be done easily. For that purpose, equation (1) – (6) were executed to obtain those values. All the calculated values are shown in Table 1 and Table 2 respectively.

Table 1. Calculated values for R_A, R_B and C in Frequency Provider part

Frequency, *f* (Hz)	Duty cycle, *D* (%)	R_A (Ω)	R_B (Ω)	*C* (F)
100	91.7	120 k	12 k	0.1 µ
10 k	91.7	120 k	12 k	0.001 µF

Table 2. Summary of the calculated values for both parts

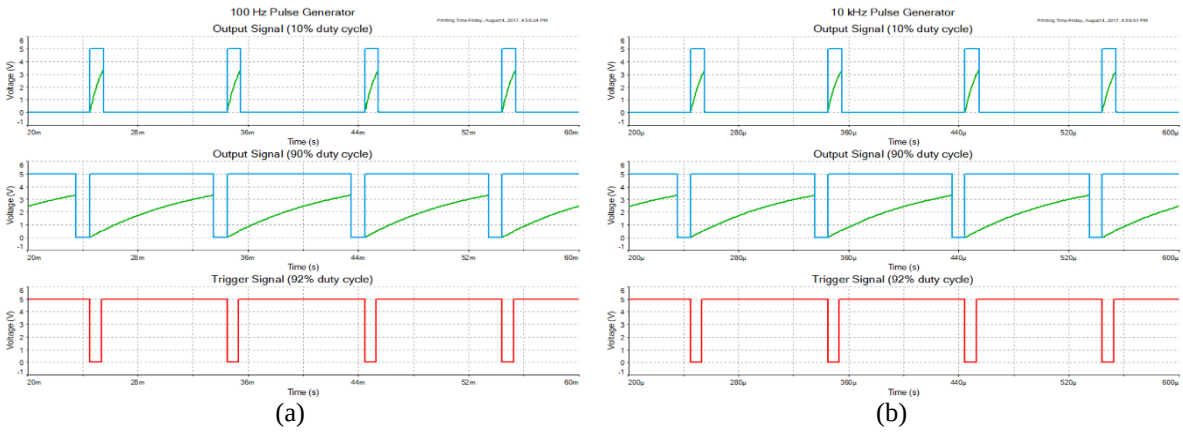
Passive Component	Mode	
	Astable	Monostable
R_A (Ω)	120 k	-
R_B (Ω)	12 k	-
C (F)	0.1 µ/0.001 µ	0.1 µ/0.001 µ
$R_{A(pot)}$ (Ω)	-	0 - 100 k

* $R_{A(pot)}$ is made variable to adjust the duty cycle

Note that in calculation result, $R_{A(pot)}$ was set to 100 kΩ to establish a smooth duty cycle alteration which enables it to reach approximately more than 90% of the full cycle. Then, these parameters were tested in the simulation process for further analysis to prove the concept of the proposed method.

3.2. Simulation results

Simulation process was done by using National Instruments (NI) Multisim 14.0 software. A complete circuit of pulse generator as shown in Figure 4 was tested with the parameters that have been computed in Table 1 and Table 2. Based on the simulation results, the proposed circuit was successful in generating the desired output. It means, the theoretical concept of this pulse generator has been proved right. Thus, an attempt to embed PWM method was successfully implemented. Figure 5 (a) and (b) displays the simulation result for 10% and 90% duty cycle of each frequency.



(a) (b)

Figure 5. The simulation result for (a) 100 Hz and (b) 10 kHz respectively. The exponent pulse shape indicates the voltage across the external capacitor

3.3. Simulation results

The printed circuit board (PCB) of pulse generator circuitry was fabricated using the Proteus 8.5 software. The 3D visualization image is shown in Figure 6 and was made in a single layer only. Both 555-timer ICs were arranged side by side to reduce the copper length that connects the trigger signal from frequency provider to the duty cycle adjuster, thus, reduces the loss.

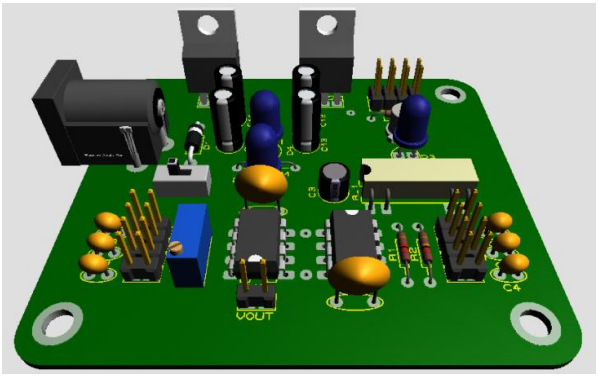


Figure 6. 3D visual image of PCB generated using Proteus 8.5 software

3.4. Experimental results

The actual PCB is shown in Figure 7 and was supplied with 5 VDC using voltage regulator 7805. It also equipped with relay and controlled by 2N2222A transistor intended to cutoff the power supply. The results obtained from practical test show good agreement with simulation results. All determined values in Table 1 and Table 2 were implemented in the real test. The cost of development is extremely low as it does

not need a sophisticated device, just an ordinary passive component that can be easily obtained from the local market.

Figure 7. A complete fabrication of pulse generator PCB

LeCroy Wavejet 354A digital oscilloscope which equipped with 4 channels and supporting band up to 500 MHz was used to measure the pulse generator output. Figure 8 (a) and (b) shows the experimental result for 100 Hz, while (c) and (d) displays the practical result for 10 kHz. As clearly be seen, the frequency is identically similar for both parts. This is the result of sharing the same value of external capacitor used in frequency provider and duty cycle adjuster.

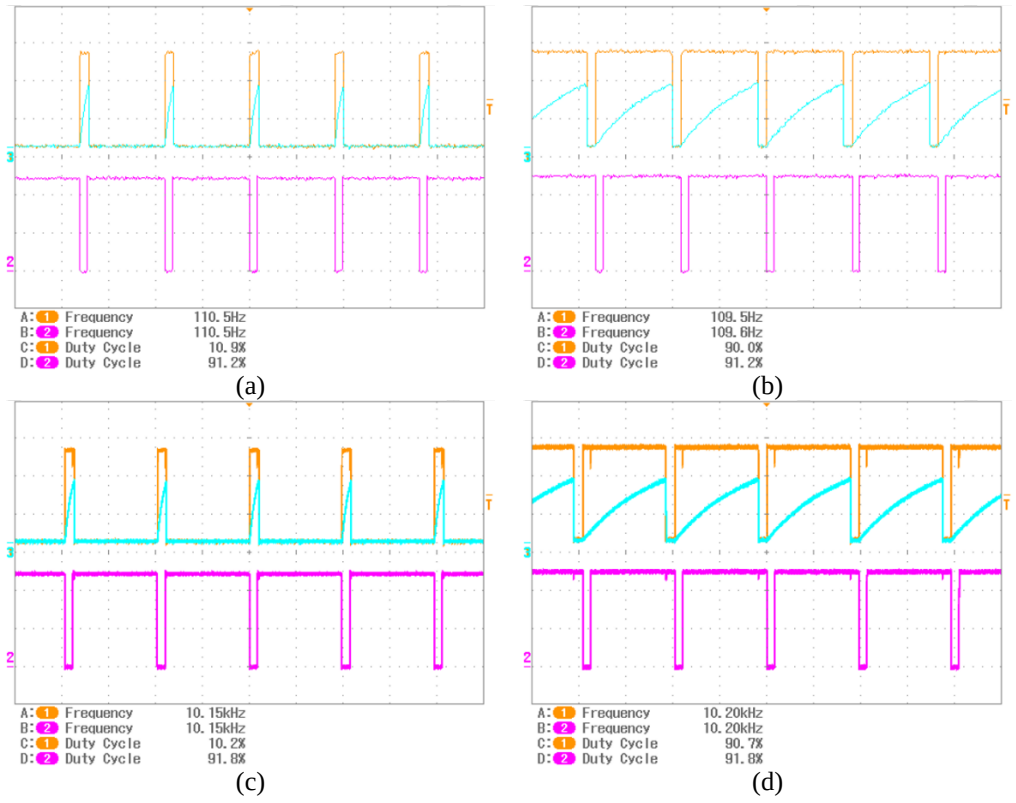


Figure 8. Practical results of pulse generator. (a) 10% duty cycle with 100 Hz, (b) 90% duty cycle with 100 Hz, (c) 10 % duty cycle with 10 kHz and (d) 90% duty cycle with 10 kHz

Both parts were behaving in their mode of operation respectively. In astable mode, the frequency provider was successfully delivered desired output. A signal with a frequency of approximately 100 Hz and 10 kHz were obtained, while duty cycle for both signals was around 90% of the full cycle. The slight difference in both frequency and duty cycle from the computed values was due to the passive components used in the circuitry system. Each component used have its own tolerance of 5% to 10%, which is still in the acceptable range.

The pulse width of the output signal was adjusted according to the PWM method by altering the value of $R_{A(pot)}$ without affecting its frequency. Based on equation (6), the time when the output stays high can be made longer if the value of R_A is high and vice versa. Practical results have shown that the pulse act as expected and in parallel with the simulation results. This proves that the concepts practiced are accurate. As for the duty cycle, it can be altered slightly lower than 10% and slightly higher than 90% of the full cycle before it starts to fail.

4. CONCLUSION

As the simulation and practical results are comparable to each other, the proposed method in producing compact, low-cost and embedded with PWM technique is successfully achieved. This clock signal of 555-timer is TTL and CMOS compatible and suitable to drive any solid-state switches for high-voltage switching that intended to be applied in PEF treatment technology. Therefore, it can replace the traditional pulse forming network (PFN) and improve the performance of the PEF system in inactivating the microorganisms.

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