

A New Seven Level Symmetrical Inverter with Reduced Switch Count

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ABSTRACT

Multilevel inverters offers less distortion and less electro-magnetic interference compared with other conventional inverters and hence, it can be used in many industrial and commercial applications. This paper analyze the performance of the modified single phase seven level symmetrical inverter using minimum number of switches. The proposed topology consists of six switches and two dc sources, and produces seven level output voltage waveform during symmetric operation. The cost and size of the propsoed inverter minimum as it uses minimum number of components, The performance of the proposed multilevel inverter is analysed for different switching angles and the corresponding simulation results are presented. The simulation of the proposed inverter is carried out using MATLAB/Simulink software.

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1. INTRODUCTION

Multilevel inverters plays an incredible role in modern power electronics [1]. Generally, the dc sources used in the multilevel inverter includes photovoltaic, capacitors and batteries [2]. They are classified into two groups such as symmetric inverter, where the all sources have same magnitude and asymmetric inverter, where the voltage sources have different magnitude [3]. The various advantages of multilevel inverters over conventional two level inverter includes low distortion, minimum switching losses high power quality, minimum peak inverse voltage (PIV) and low dv/dt stress [4-5]. However, it requires greater amount of power electronic components and gate driver circuits to achieve higher output levels [6]. The most popular commercial topologies of multilevel inverters includes neutral point clamped, flying capacitor and cascaded H-bridge inverters [7-9]. The CHB inverter is more modular and can be easily expandable for greater number of steps in the output voltage. It requires less switching components as compared with other inverters to achieve same levels of output. The number of level in the output voltage waveform can be increased simply by adding the required number of different dc sources [10]. Nowadays, many researchers have proposed new inverter topology with modified control techniques to improve their performance.

This paper presents a new symmetric type inverter with reduction in switch count. It consists of three voltage sources and six switches which generate seven level output waveform during symmetric operation. Different modes of operation of the inverter is explained in Section II. Different methods of calculating the switching angles are presented in Section III. The simulation results are discussed in Section IV. The conclusion was given in Section V.

2. PROPOSED INVERTER TOPOLOGY

The schematic diagram of the proposed inverter circuit is shown in Figure 1. It can produce 7-level output voltage during symmetrical case of operation. In the proposed inverter, the magnitude of the sources is same and hence the name "symmetry".

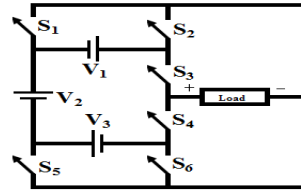


Figure 1. Proposed Multilevel Inverter

The different operating levels of the presented inverter topology is shown in Figure 2. In level - 0, zero voltage is obtained with the switches S_2 and S_3 or S_4 and S_6 are ON and the other switches are OFF. The positive level -1 voltage is obtained with the ON state switches are S_1 and S_3 and other switches were OFF. The positive level-2 voltage V_1+V_2 is obtained with the switches S_3 and S_5 ON. During the positive level - 3, the switches S_3 and S_6 are ON and the voltage $V_1+V_2+V_3$ is obtained across the load. During the negative level - 1, the voltage $-V_3$ is obtained across the load. During this level, the switches S_4 and S_5 are ON. During the negative level - 2, the voltage $-(V_3+V_2)$ is obtained with the switches S_1 and S_4 ON. During the negative level - 3, the voltage $-(V_1+V_2+V_3)$ is obtained across the load with the switches S_2 and S_4 ON. The comparison for different topologies of multilevel inverter are given in Table 1.

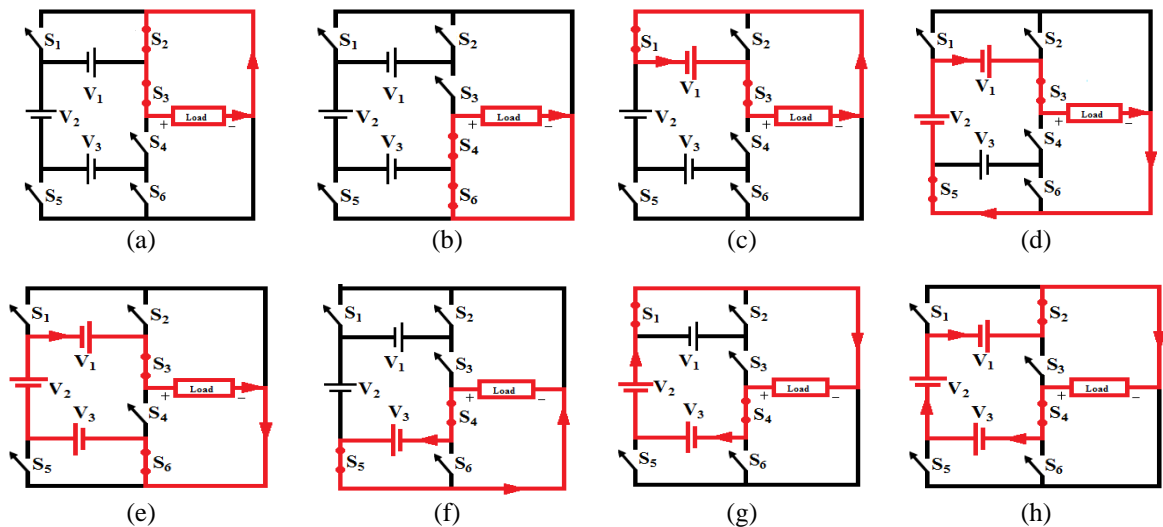


Figure 2. Operating Modes (a) Positive Level 0 (b) Negative Level 0 (c) Positive Level 1 (d) Positive Level 2 (e) Positive Level 3 (f) Negative Level 1 (g) Negative Level 2 and (h) Negative Level 3

Table 1. Comparison of Different Multilevel Inverter Topologies

Inverter	Number of Sources (N_{dc})	Number of Switches (N_S)	Number of level (N)	Ratio (N_{dc} / N)	Ratio (N_S / N)
Cascaded	3	12	7	0.4286	1.7143
Ref. [11], [12]	3	8	7	0.4286	1.1428
Ref. [13]	3	10	7	0.4286	1.4286
Ref. [14]	3	16	7	0.4286	2.857
Ref. [15]	3	9	7	0.4286	1.2857
Ref. [16]	3	7	7	0.4286	1
Proposed	3	6	7	0.4286	0.8571

For the proposed inverter, the ratio of the number of sources to the level is 0.4286 which is equal to CHB and other presented inverter topologies. However the ratio of the number of switches to output level is 0.8571 which is less than that of other inverter topologies. Therefore, it is clear that this inverter topology uses minimum amount of switches to achieve 7-level voltage waveform.

3. SWITCHING ANGLE CALCULATION

The angles corresponding to the period 0 to 90° are called as main switching angles and are calculated using the following different methods [17-19].

Method - 1

The averagely distributed switching angles over the range 0–90° are determined by,

$$\theta_i = i \frac{180^0}{N} \text{ where, } i = 1, 2, 3, \dots, \left(\frac{N-1}{2}\right)$$

Method - 2

Here, the key switching angles are determined by,

$$\theta_i = i \frac{180^0}{N+1} \text{ where, } i = 1, 2, 3, \dots, \left(\frac{N-1}{2}\right)$$

Method - 3

In this method, the main angles are determined by,

$$\theta_i = \sin^{-1}\left(\frac{2i-1}{N-1}\right) \text{ where, } i = 1, 2, 3, \dots, \left(\frac{N-1}{2}\right)$$

where, N = Number of output levels.

This method gives better output voltage waveform compared with other methods. The switching pulses obtained using the different methods are shown in Figure 3. The different switching states are given in Table 2.

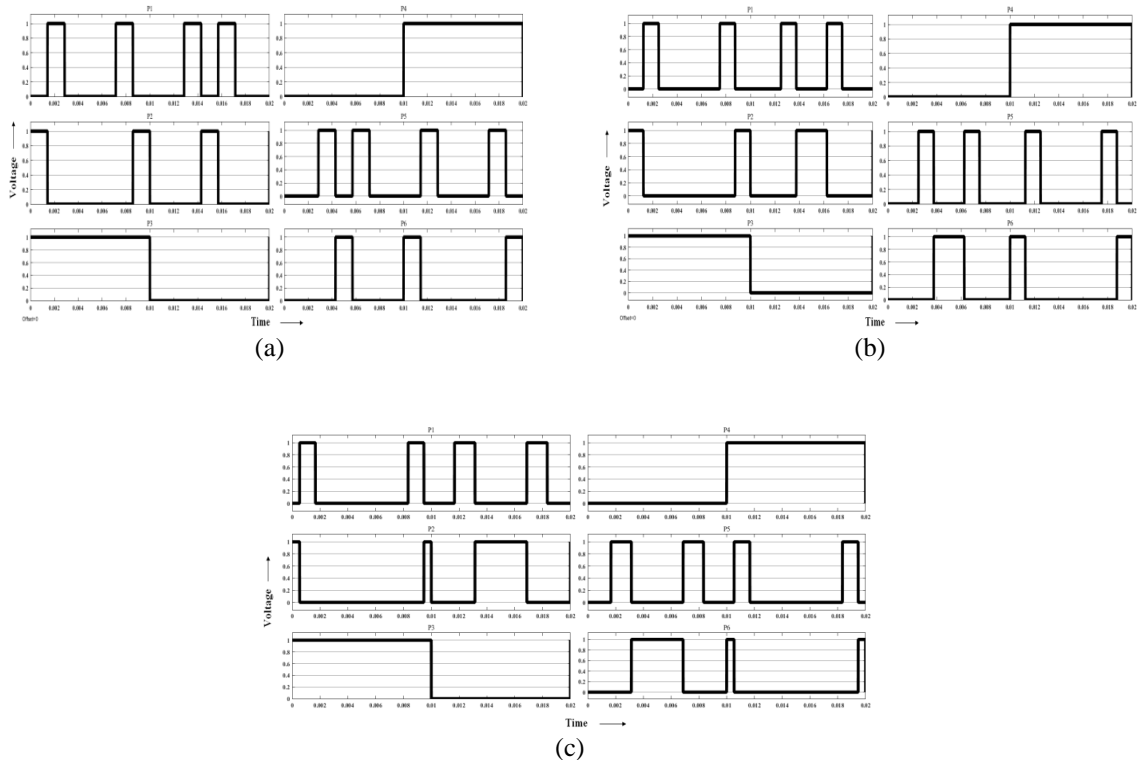


Figure 3. Switching Pulses (a) Method - 1 (b) Method - 2 and (c) Method - 3

Table 2. Switching States For Different Modes of Operation

Mode	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	Output
Positive Level-0	0	1	1	0	0	0	0
Positive Level-1	1	0	1	0	0	0	V ₁
Positive Level-2	0	0	1	0	1	0	V ₁ +V ₂
Positive Level-3	0	0	1	0	0	1	V ₁ +V ₂ +V ₃
Negative Level-0	0	0	0	1	0	1	0
Negative Level-1	0	0	0	1	1	0	-V ₃
Negative Level-2	1	0	0	1	0	0	-(V ₃ +V ₂)
Negative Level-3	0	1	0	1	0	0	-(V ₃ +V ₂ +V ₁)

4. RESULTS AND DISCUSSION

This section presents the simulation results of the developed symmetrical 7-level inverter. The magnitude of the sources are taken as V₁ = V₂ = V₃ = 60 V. The maximum voltage obtained as 240 V (i.e., V₁+V₂+V₃). Figure 4 shows the seven level voltage obtained for different switching methods. The FFT analysis of the 7 level voltage waveform for are given in Figure 5.

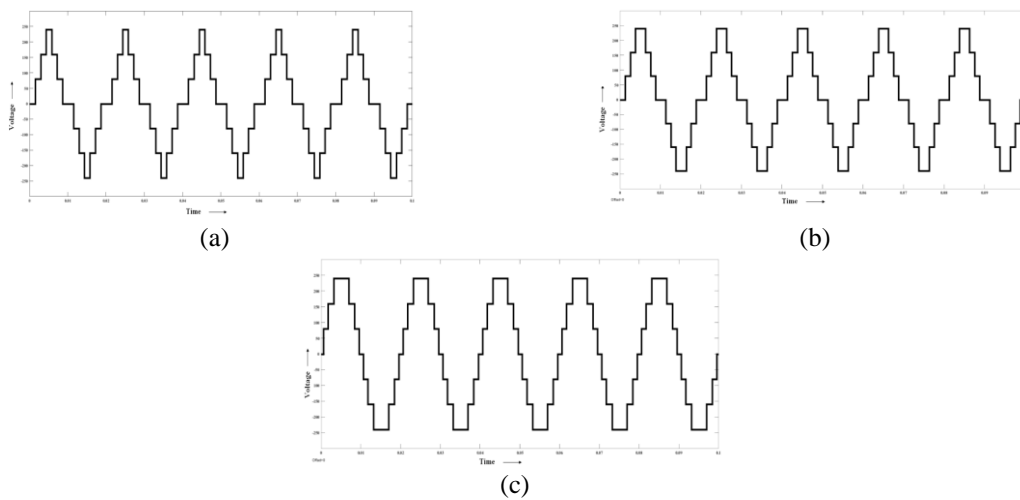


Figure 4. Output Voltage (a) Method - 1 (b) Method - 2 and (c) Method - 3

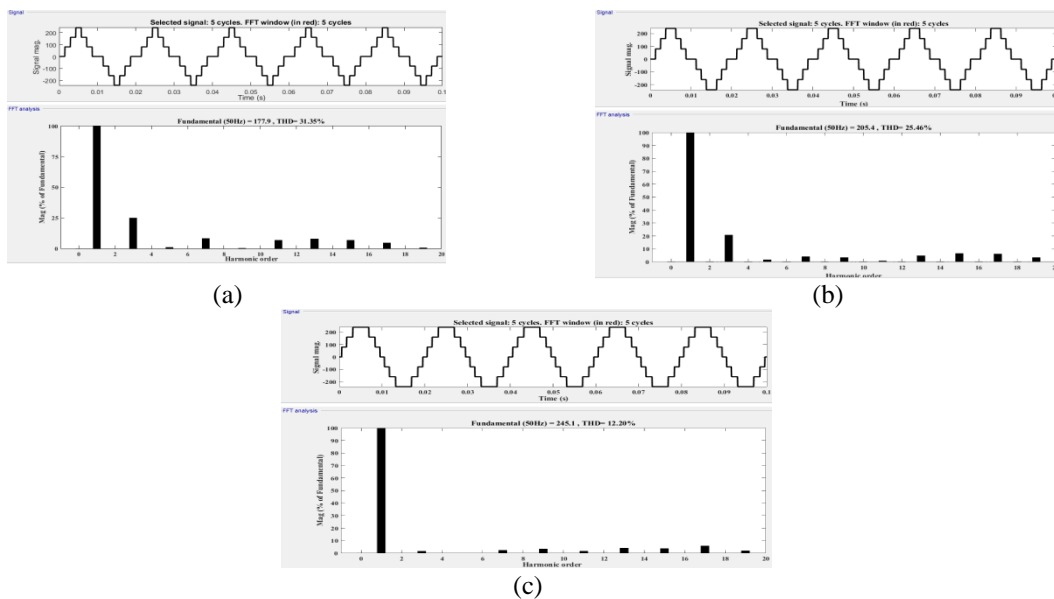


Figure 5. FFT Analysis (a) Method - 1 (b) Method - 2 and (c) Method - 3

The simulation result shows that the harmonic content for the switching method - 3 is less when compared with the method-1 and method -2. The results are given in Table 3.

Table 3. Comparison of Total Harmonic Distortion

Method	THD (%)
Method - 1	31.35
Method - 2	25.46
Method - 3	12.20

5. CONCLUSION

This article proposed a new symmetric 7-level inverter topology. This inverter uses three sources to achieve 7-level output voltage. The proposed inverter circuit can be connected in series to generate higher levels. The different methods used to calculate the switching angles are discussed in this paper. The simulation result shows that the switching angles obtained by method - 3 achieves minimum THD as 12.2% compared with other methods.

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