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Novel Switching Design Structure for Three Phase 21-Level Multilevel Inverter Fed BLDC Drive Application

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ABSTRACT

Multilevel Inverters offers eminent solutions to high voltage high power applications due to the association of several devices in a series configuration. This is moderate because of getting superior quality voltage waveform when using multilevel inverters as compared to form two-level inverters. Most of the problems raised in this study are the restriction of many switching devices, which can afford high voltage are preferred in the inverter. Here, a novel multilevel inverter topology with no transformers, less number of switching devices and gate drive circuits are proposed. The proposed inverter topologies can valid more voltage levels with favorable advantages such as less number of switching devices and gate driving circuits and reduce to humble size, agreeable voltage profile. In this paper multilevel converter fed BLDC drive with different voltage levels and simulation analysis is presented. The validity of the proposed three-phase 21-level multilevel inverter fed to BLDC motor drive scheme is verified through Matlab/Simulink Platform.

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1. INTRODUCTION

Voltage Source Inverter (VSI) produces an output voltage with levels either 0, $+V_{dc}$ or $-V_{dc}$ which are read as three level inverters. To achieve high quality output voltage waveform with less amount of ripple current, high-switching frequency along with various Pulse-Width Modulation techniques are required. The switching devices should be used in such a manner as to avoid problems associated with their series-parallel combinations that are necessary to obtain the capability of handling high voltage and currents.

Multi-Level Inverters (MLIs) are mostly used in power industry such as reactive power compensation, drive control and renewable energy sources. It might be an easier to produce high-power, high-voltage inverters with multilevel structure because of the way in which device voltage stresses are controlled in the structure [1], [2]. Increasing number of voltage levels in inverter without the necessity of higher ratings on individual devices can increase the power rating. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without any use of transformers or series-connected synchronized semiconductor switching devices. As number of levels increases, the harmonic content of the output voltage waveform decreases significantly in multilevel inverter [3].

Regular structure of multilevel converter is to synthesize a nearly sinusoidal voltage from several levels of input of DC voltages, typically from capacitor voltage sources [4], [5]. As the number of levels increases, the output waveform has more steps that produce a staircase wave [6] and approaches required output waveform. As the numbers of steps are added to the waveform, the output waveform has reduced

harmonic distortion, approaching zero as the number of levels increases. As number of levels increase the voltage that can be spanned by summing multiple voltage levels also increases. MLIs can be classified as: [7],

a. Diode-clamped multilevel inverter
b. Flying-capacitors multilevel inverter
c. Hybrid Inverters
d. Cascademultilevel inverter.

Advantages of Cascade Multi-Level Inverter (CMLI) requires least number of components to achieve the same number of voltage levels as when compared to diode-clamped and flying-capacitor MLIs [3]. In CMLI optimized circuit layout and packaging are also possible because of each level has the same structure, and there are no extra clamping diodes or voltage-balancing capacitors [8], [9].

In Cascade H-Bridge (CHB) configuration, the number of voltage levels is determined by using expression 2n+1 [4]. 'n' means one full H-bridge inverter. One full H-bridge inverter has 4 switches. The number of levels increases in the cascade H-bridge configuration, then several switches, protection circuit, complexity, place required, and cooling equipment increases [10], [11].

Proposed Single Phase MLI has only 10 switches and can produce voltage levels of 7, 9, 11, 13, 15, 17, 19 and 21, and will reduce the harmonic content whenever the number of output voltage levels are increased [5]. In this paper 17, 19 and 21 level output voltage switching configurations are presented with reduction in harmonic content when the voltage levels increase. Proposed three-phase 21-level multilevel inverter is fed to BLDC motor application.

2. PROPOSED SINGLE PHASE MULTI-LEVEL INVERTER

Operating at fundamental frequency and produces output voltage levels of 7, 9, 11, 13, 15, 17, 19 and 21. The operation of inverter for switching configuration of 17, 19 and 21-levels are presented.

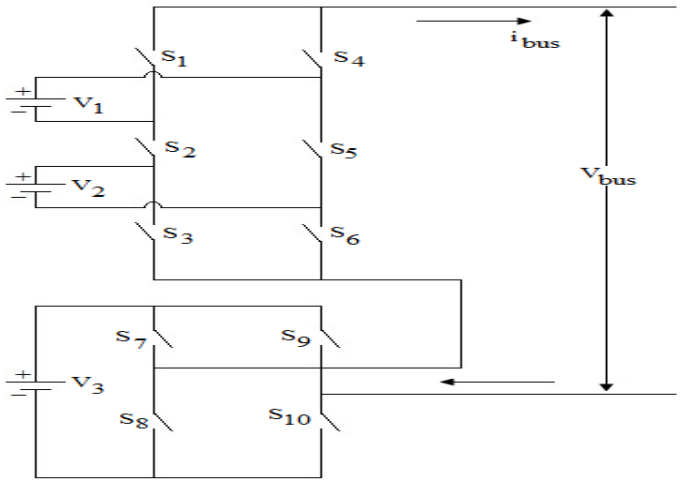

Figure 1. Proposed single phase multilevel inverter

2.1. Proposed Single Phase 17-Level MLI

The proposed single phase17-level MLI has switching configuration as shown in Table 1. Table 1 shows the switching configuration of proposed single phase 17-level MLI. Input Voltages are taken as V_1=100V, V_2=200V, V_3=500V in the proposed MLI. In Table.1, switching states '1' represents the switch is 'ON' and '0' represents the switch is 'OFF'. Figure 2 shows the Output Voltage waveform of proposed Single Phase 17-Level.

Table 1. Switching States of Proposed Single Phase 17-level MLI

Vo	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
8Vs	0	1	0	1	0	1	1	0	0	1
7Vs	1	1	0	0	0	1	1	0	0	1
6Vs	0	1	1	1	0	0	1	0	0	1
5Vs	1	1	1	0	0	0	1	0	0	1
4Vs	1	0	0	0	1	1	1	0	0	1
3Vs	0	1	0	1	0	1	1	0	1	0
2Vs	1	1	0	0	0	1	1	0	1	0
Vs	0	1	1	1	0	0	1	0	1	0
0	1	1	1	0	0	0	1	0	1	0
-Vs	1	0	0	0	1	1	1	0	1	0
-2Vs	0	0	1	1	1	0	1	0	1	0
-3Vs	1	0	1	0	1	0	1	0	1	0
-4Vs	0	1	1	1	0	0	0	1	1	0
-5Vs	1	1	1	0	0	0	0	1	1	0
-6Vs	1	0	0	0	1	1	0	1	1	0
-7Vs	0	0	1	1	1	0	0	1	1	0
-8Vs	1	0	1	0	1	0	0	1	1	0

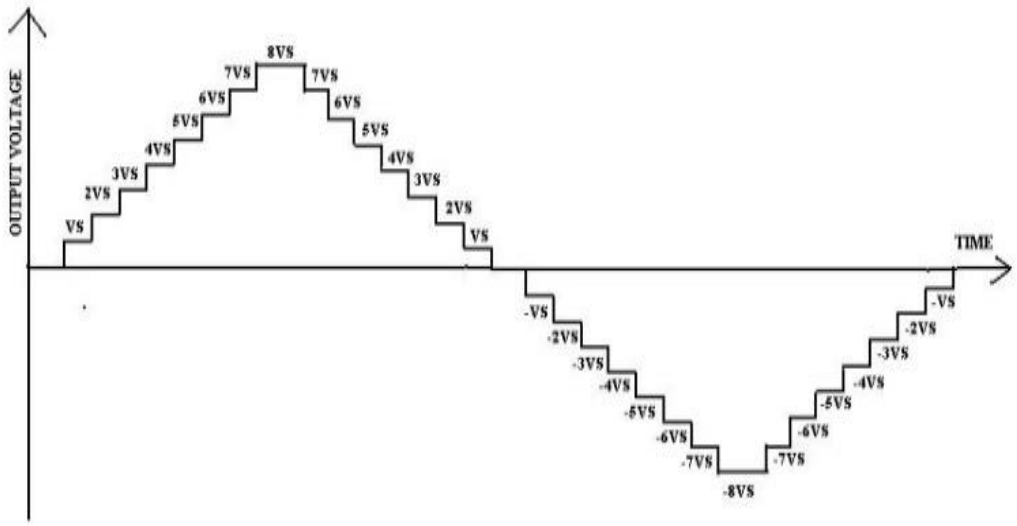

Figure 2. Output Voltage of Proposed Single Phase 17-Level MLI

Table.1 shows the switching configuration of proposed single phase 17-level MLI. Input Voltages are taken as V_1=100V, V_2=200V, V_3=500V in the proposed MLI. In Table.1, switching states '1' represents the switch is 'ON' and '0' represents the switch is 'OFF'. Figure 2 shows the Output Voltage waveform of proposed Single Phase 17-Level.

2.2. Proposed Single Phase 19-Level MLI

The proposed Single Phase 19-level MLI has switching configuration as shown in Table 2. Table 2 shows the switching configuration of proposed single phase 19-level MLI. Input voltages are taken as V_1= 100V, V_2=200V, V_3=600V in the proposed multilevel inverter. In Table 2 the switching states '1' means the switch is 'ON' and '0' means the switch is 'OFF'. Figure 3 shows the Single Phase 19-Level Output Voltage of Newly Proposed MLI.

Table 2. Single phase proposed MLI with 19-level switching states

Vo	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
9Vs	0	1	0	1	0	1	1	0	0	1
8Vs	1	1	0	0	0	1	1	0	0	1
7Vs	0	1	1	1	0	0	1	0	0	1
6Vs	1	1	1	0	0	0	1	0	0	1
5Vs	1	0	0	0	1	1	1	0	0	1
4Vs	0	0	1	1	1	0	1	0	0	1
3Vs	0	1	0	1	0	1	1	0	1	0
2Vs	1	1	0	0	0	1	1	0	1	0
Vs	0	1	1	1	0	0	1	0	1	0
0	1	1	1	0	0	0	1	0	1	0
-Vs	1	0	0	0	1	1	1	0	1	0
-2Vs	0	0	1	1	1	0	1	0	1	0
-3Vs	1	0	1	0	1	0	1	0	1	0
-4Vs	1	1	0	0	0	1	0	1	1	0
-5Vs	0	1	1	1	0	0	0	1	1	0
-6Vs	1	1	1	0	0	0	0	1	1	0
-7Vs	1	0	0	0	1	1	0	1	1	0
-8Vs	0	0	1	1	1	0	0	1	1	0
-9Vs	1	0	1	0	1	0	0	1	1	0

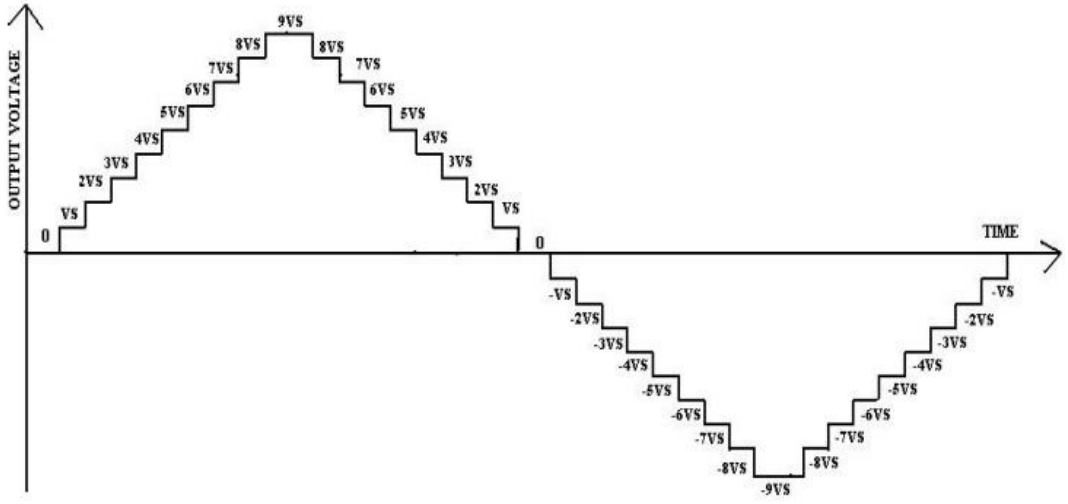

Figure 3. Output Voltage of Proposed Single Phase 19-Level MLI

2.3. Proposed Single Phase 21-Level Multilevel Inverter

21- Level proposed MLI has switching configuration as shown in Table 3. Input voltages are taken as V_1=100V, V_2=200V, V_3=700V. In Table 3, the switching states '1' means the switch is 'ON,' and '0' means the switch is 'OFF'. Figure 4. shows the Single Phase 21-Level Output Voltage of Newly Proposed MLI.

Table 4 shows the comparison of the required number of switches for a single-phase Cascaded H-Bridge configuration and single-phase proposed MLI. In Table 4, proposed single phase MLI has 10 switches which can produce the voltage levels of 7, 9, 11, 13, 15, 17, 19 and 21. The proposed single phase MLI has more advantages when compared to the single phase cascaded H-bridge configuration, reduced number of switching devices, a control circuit, protection circuit, cooling equipment, space requirement and switching losses.

Table 3. Single Phase Newly Proposed MLI of 21-level Switching States

Vo	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
10Vs	0	1	0	1	0	1	1	0	0	1
9Vs	1	1	0	0	0	1	1	0	0	1
8Vs	0	1	1	1	0	0	1	0	0	1
7Vs	1	1	1	0	0	0	1	0	0	1
6Vs	1	0	0	0	1	1	1	0	0	1
5Vs	0	0	1	1	1	0	1	0	0	1
4Vs	1	0	1	0	1	0	1	0	0	1
3Vs	0	1	0	1	0	1	1	0	1	0
2Vs	1	1	0	0	0	1	1	0	1	0
Vs	0	1	1	1	0	0	1	0	1	0
0	1	1	1	0	0	0	1	0	1	0
-Vs	1	0	0	0	1	1	1	0	1	0
-2Vs	0	0	1	1	1	0	1	0	1	0
-3Vs	1	0	1	0	1	0	1	0	1	0
-4Vs	0	1	0	1	0	1	0	1	1	0
-5Vs	1	1	0	0	0	1	0	1	1	0
-6Vs	0	1	1	1	0	0	0	1	1	0
-7Vs	1	1	1	0	0	0	0	1	1	0
-8Vs	1	0	0	0	1	1	0	1	1	0
-9Vs	0	0	1	1	1	0	0	1	1	0
-10Vs	1	0	1	0	1	0	0	1	1	0

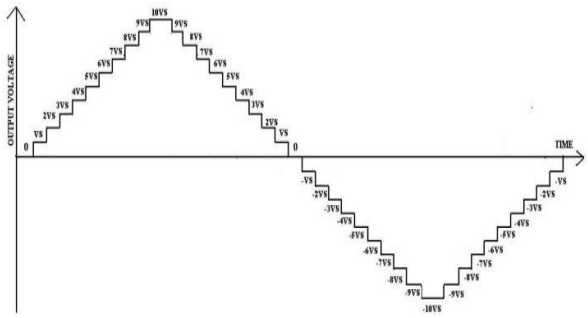

Figure 4. Output voltage of single phase 21-level proposed MLI

Table 4. Number of Switches Required to the Single-phase CHB and Single Phase Proposed MLI

OUTPUT VOLTAGE LEVELS	NUMBER OF SWITCHING DEVICES	
	SINGLE PHASE CASCADED H-BRIDGE MLI	SINGLE PHASE NEWLY PROPOSED MLI
7 LEVEL	12	10
9 LEVEL	16	10
11LEVEL	20	10
13 LEVEL	24	10
15 LEVEL	28	10
17 LEVEL	32	10
19 LEVEL	36	10
21 LEVEL	40	10

3. PROPOSED THREE PHASE MLI

Proposed three phase MLI has 30 switches for three phases. Each phase consists of 10 switches. The phase to phase voltage delay angle is 120 degrees (R-Y is 120^o, Y-B is 120^o, B-R is 120^o). Figure 5. shows the Proposed Three Phase Multilevel Inverter Fed Brushless DC Motor, which consist of 30 switches (each phase 10 switches) and 9 voltage sources. Table 5 shows the number of switches required for three-phase Cascaded H-Bridge configuration and proposed three-phase MLI. The proposed three-phase MLI produces output voltage (phase to neutral) levels of 7, 9, 11, 13, 15, 17, 19 and 21. The advantages of three-phase proposed MLI are less number of switches, complexity, protection circuit, cooling requirement, a control circuit, switching losses and space requirement reduces compared to the three-phase cascaded H-bridge configuration.

Typical commercial & residential applications attend to employ formal drive technologies, like brushed DC motors as well as single-phase Induction motors. Nevertheless, these machines are differentiated by high maintenance and low efficiency respectively. Among the several machine formations available, BLDC machines are deliberate as robust contenders [3], [7]. Three-phase BLDC drive is normally implemented by using a power electronic converter design of Metal Oxide Semiconductor Filed Effect Transistor (MOSFET) or Insulated Gate Bipolar Transistor (IGBT) and maintain 120^o electrical angle for every phase for conduction [4]. Fig.5 shows a structure of three phase star connected drive along with individual commutation phase energizing sequence with respect to angle, like AB; AC; BC; BA; CA; CB. However, two phases will be conducting at a time, leaving the third phase which should be null. Maximum torque will be generated with the converter when commutated for every 60^o, so the armature current will be in phase with back EMF (E_b) [5], [8].

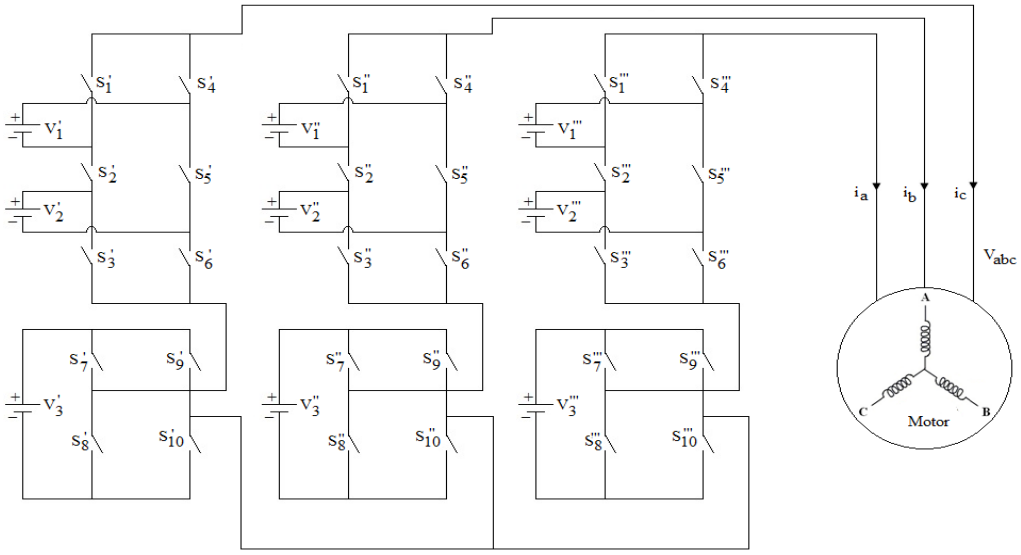

Figure 5. Proposed three phase MLI fed BLDC motor

Table 5. Number of Switches Required for the 3-phase CHB and Proposed 3-phaseMLI

OUTPUT VOLTAGE LEVELS (PHASE TO NEUTRAL VOLTAGE)	NUMBER OF SWITCHING DEVICES	
	3-PHASE CASCADED H-BRIDGE MLI	3-PHASE PROPOSED MLI
7 LEVEL	36	30
9 LEVEL	48	30
11LEVEL	60	30
13 LEVEL	72	30
15 LEVEL	84	30
17 LEVEL	96	30
19 LEVEL	108	30
21 LEVEL	120	30

4. RESULTS

Modeling & Simulation is carried out for the following proposed Multi-level Inverters

1. Single Phase 17-Level Multilevel Inverter
2. Single Phase 19-Level Multilevel Inverter
3. Single Phase 21-Level Multilevel Inverter
4. Three Phase 21-Level Multilevel Inverter with BLDC Drive using less number of switching devices.

Figure 6 shows the Matlab/Simulink Model of Proposed Single Phase MLI using Matlab/Simulink Software Package. Figure 7 shows output voltage of proposed single-phase 17-level MLI. Figure 8 shows the THD of the 17-level output voltage of proposed single-phase MLI and can be observed that the total harmonic distortion is 13.93%. Figure 9 shows the 19-level output voltage of proposed single-phase MLI. Figure 10 shows the THD of the 19-level output voltage of proposed single-phase MLI and can be observed that the THD is 13.67%. Figure 11 shows the 21-level output voltage of proposed single phase MLI. Figure

12 shows the THD of the 21-level output voltage of proposed single-phase MLI ad can be observed that the total harmonic distortion is 12.65%. Figure 13 shows the Simulink Model of Proposed Three Phase 21-Level MLI Fed BLDC drive using Matlab/Simulink Software Package with less number of the switching device. Figure 14 shows the 21- level output voltage of newly proposed three-phase MLI fed BLDC drive. Figure 15 shows the stator current (Is_{abc}), electromotive force (E_b), respectively of proposed three-phase 21-level MLI fed BLDC drive. Figure 16 shows the Speed (N) and Electromagnetic Torque (T_e) respectively of proposed Three Phase 21- level MLI fed BLDC drive. At 0.06 sec the speed of the drive has attained steady state and the electromagnetic torque is stale from 0.04 sec.

Case 1: Single Phase 17-Level MLI

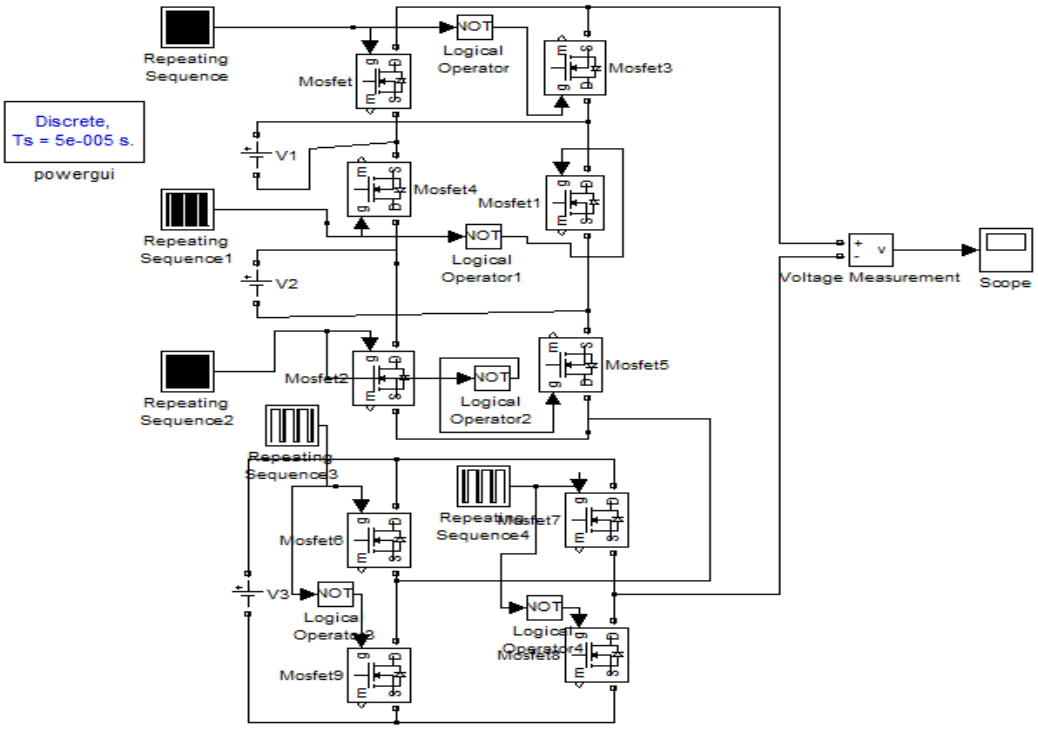

Figure 6. Simulink model of proposed single phase 17-level MLI

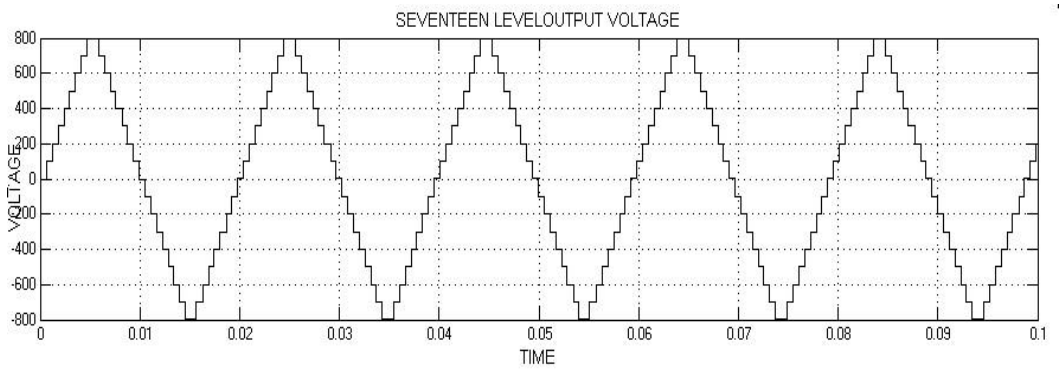

Figure 7. Output voltage of proposed single-phase 17-Level MLI

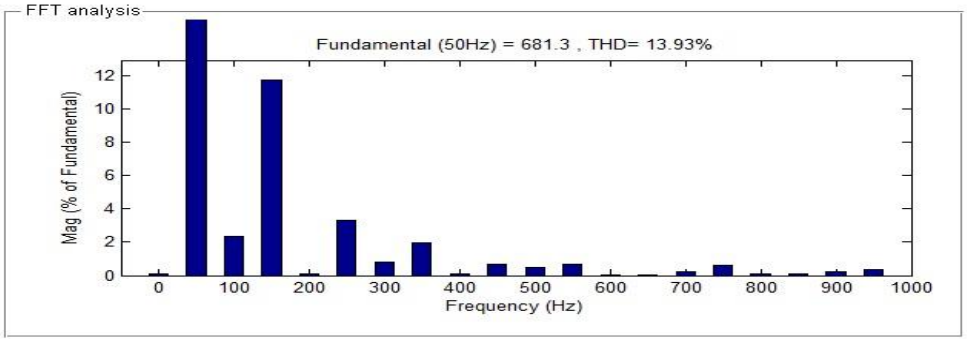

Figure 8. THD of 17-level output voltage of proposed single-phase MLI

Case 2: Proposed Single Phase 19-Level MLI

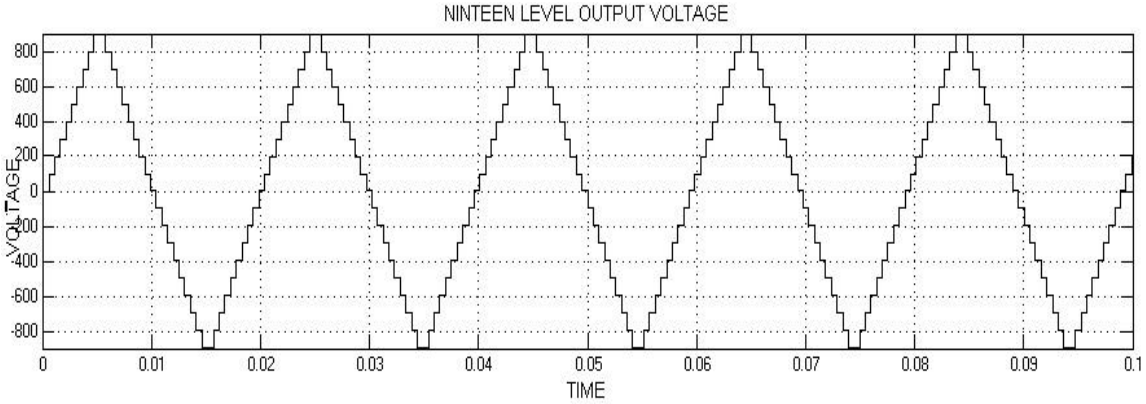

Figure 9. 19-level output voltage of proposed single-phase MLI

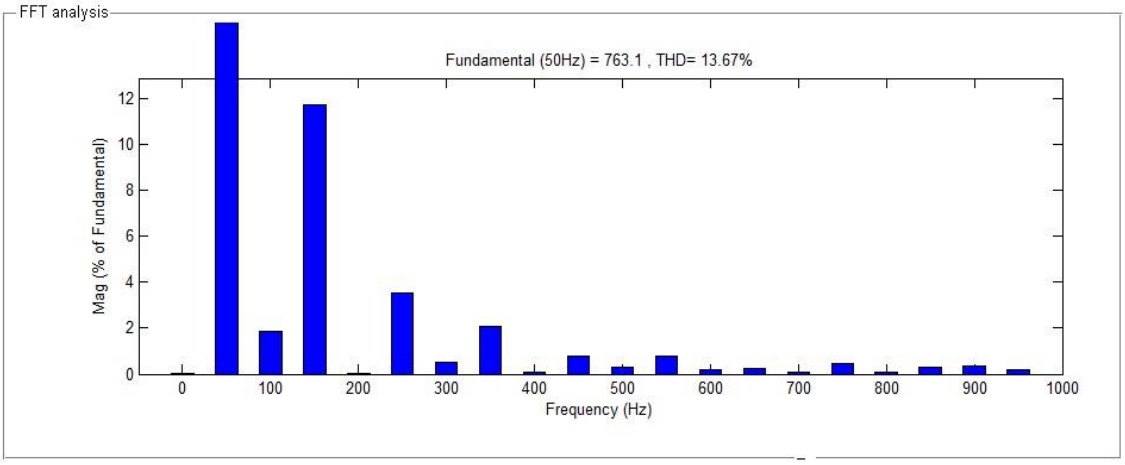

Figure 10. THD of proposed 19-level single-phase MLI

Case 3: Proposed Single Phase 21-Level Multilevel Inverter

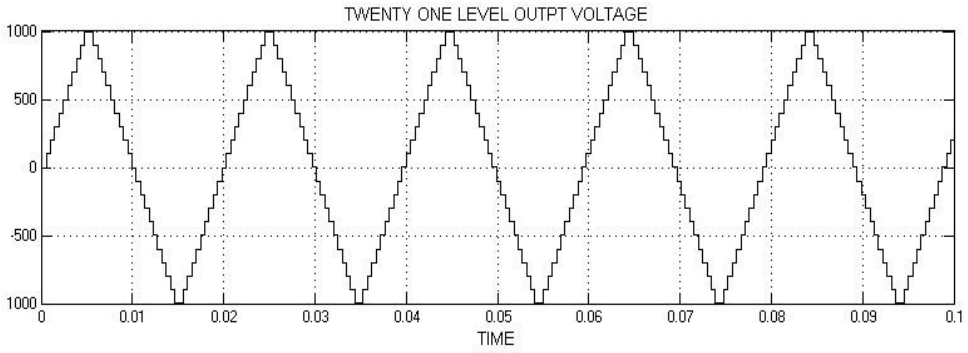

Figure 11. 21-level output voltage of proposed single-phase MLI

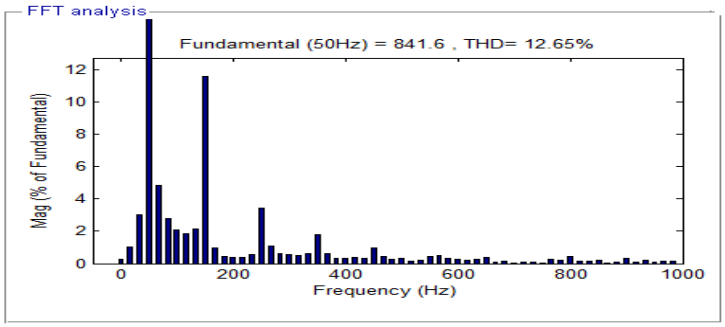

Figure 12. THD of 21-level output voltage of proposed single-phase MLI

Case 4: Proposed Three Phase 21-Level Multilevel Inverter Fed BLDC Drive

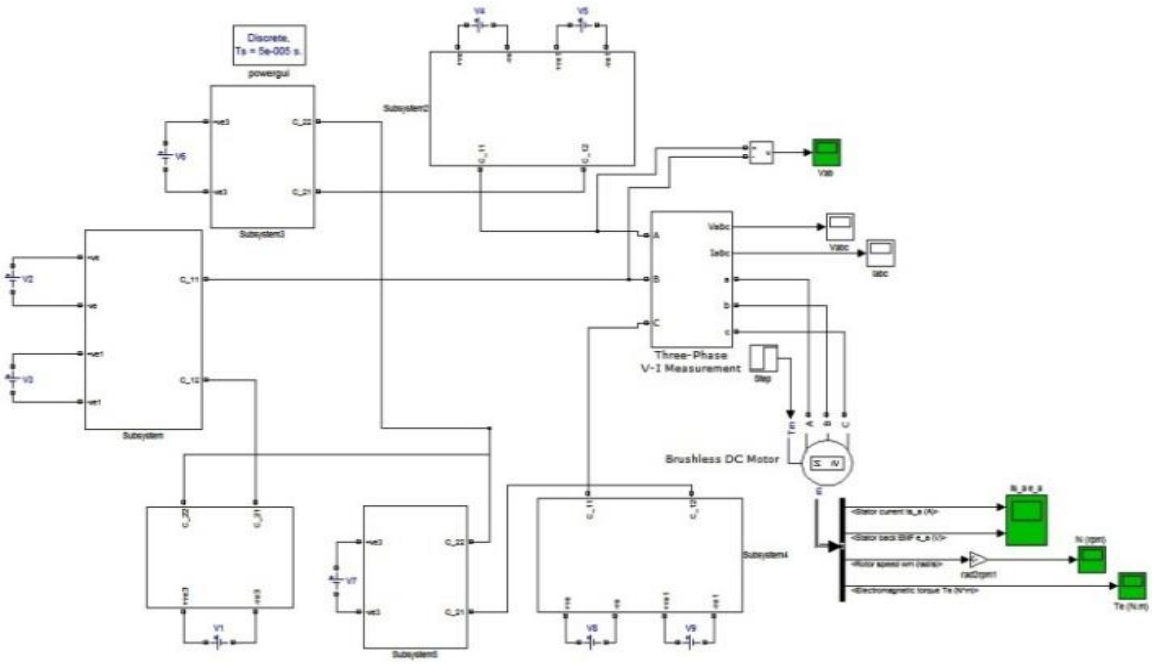

Figure 13. Simulink model of proposed three phase 21-level multilevel inverter fed BLDC drive

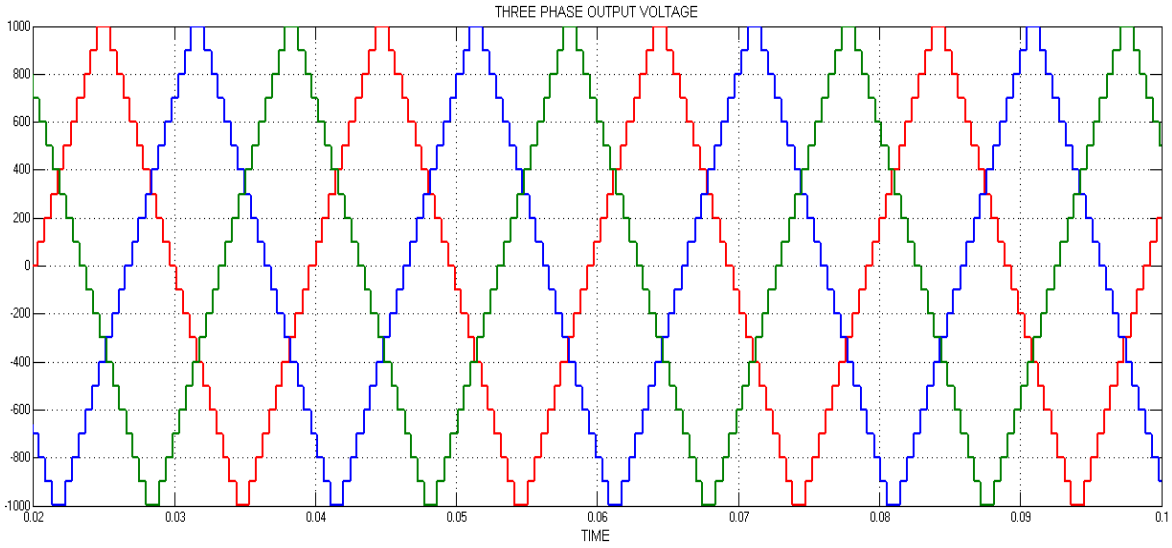

Figure 14. 21-level output voltage of proposed three-phase MLI

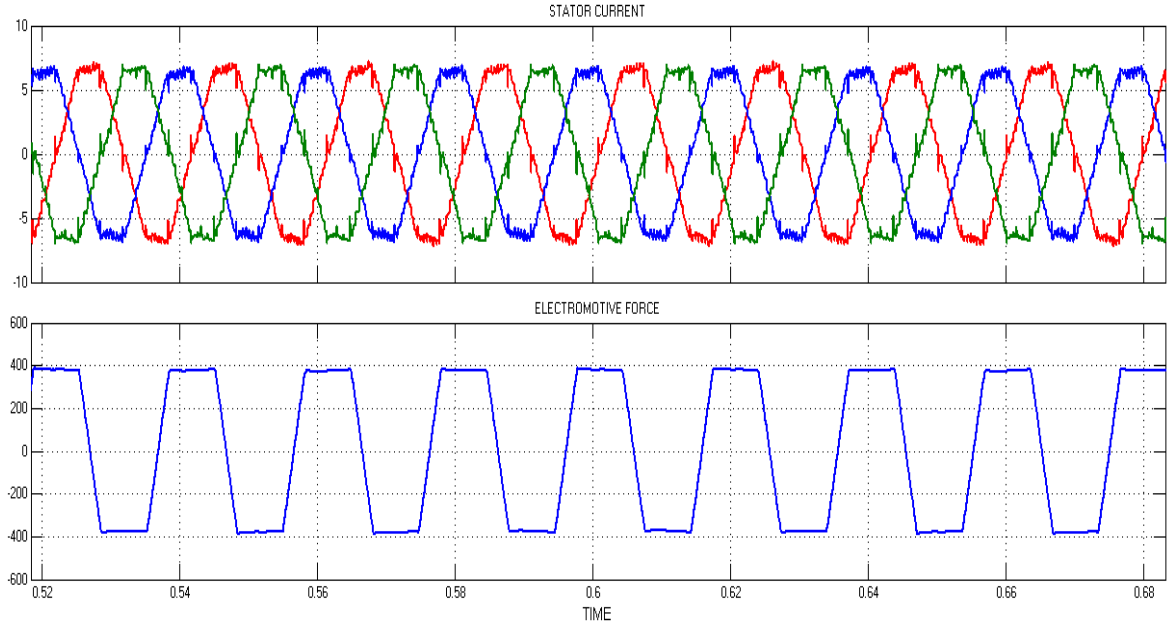

Figure 15. Stator current (Is_{abc}), electromotive force (Eb)

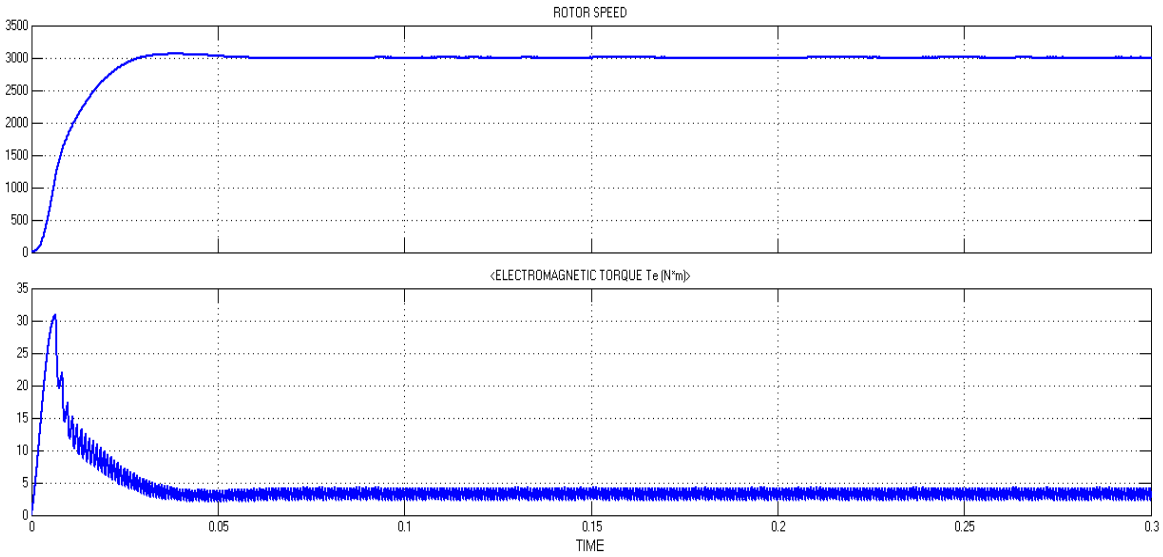

Figure 16. Speed (N), electromagnetic torque (T_e) of BLDC drive

5. CONCLUSION

Nowadays, several industrial applications are a dependency on multilevel converter topologies because of expressive attention due to their low electromagnetic interference, mechanically high reliability and high efficiency. This paper evaluated an abrupt analysis of newly proposed three-phase 21-level multilevel inverter configuration and applied to BLDC drive application owing to minimize torque ripples. Here the intention is simply to provide good quality of output voltage with low THD with the evolution of proposed multilevel converter topologies.

REFERENCES

[1] E.Babaei, C. Buccella, M. Saeedifard. "Recent Advances in Multilevel Inverter and their Applications: PartI", *IEEE Transactions on Industrial Electronics*, Vol. 63, No. 11, Nov 2016, pp 7145-7147.

[2] E.Babaei, C. Buccella, M. Saeedifard. "Recent Advances in Multilevel Inverter and their Applications: Part II", *IEEE Transactions on Industrial Electronics*, Vol. 63, No. 11, Nov 2016, pp 7777-7779.

[3] Asha Gaikwad, Pallavi AppasoArbune. "*Study of Cascaded H-Bridge Multilevel Inverter*", International Conference on Automatic Control and Dynamic Optimization Techniques, Pune, 9th – 10th Sept. 2016

[4] B. PhaniTeja, V. Srikanth Babu, T. Suresh Kumar. "Modelling of Static VAR Compensator employing a cascaded H-BridgedMultilevel Converter" *International Journal of Applied Engineering Research*, Vol. 10, No. 16, 2015, pp: 37057-37062.

[5] R. Uthirasamy, U. S. Ragupathy, R. Naveen."Structure of 15-Level Sub-Module Cascaded H-Bridge Inverter for Speed Control of AC Drive Applications", *International Journal of Power Electronics and Drive Systems*, Vol 5 No 3, 2015 pages 404-414

[6] Chinnapettai Ramalingam Balamurugan, S.P. Natarajan, V. Padmathilagam, T.S. Anandhi."Design of A New Three Phase Hybrid H-bridge and H-Type FCMLI for Various PWM Strategies", *International Journal of Advances in Applied Sciences*, Vol 4 No 3, 2015

[7] SurosoSuroso, Toshihiko Noguchi."A Single-Phase Multilevel Current-Source Converter using H-Bridge and DC Current Modules", *International Journal of Power Electronics and Drive Systems*, Vol 4, 2014 165-172

[8] Pritha Agrawal, Satya Prakash Dubey,Satyadharma Bharti. "Comparative Study of Fuzzy Logic Based Speed Control of Multilevel Inverter fed Brushless DC Motor Drive", *International Journal of Power Electronics and Drive Systems*, Vol 4 No 1, 2014 pages 70-80

[9] Mulukutla Venkata Subramanyam, P.V.N. Prasad, G.Poornachandra Rao."Fuzzy Logic Closed Loop Control of 5 level MLI Driven Three phase Induction motor", *International Journal of Power Electronics and Drive Systems*, Vol 3 No 2, 2013 pages 200-208

[10] K.N.V Prasad, G.Ranjith Kumar, T. Vamsee Kiran, G. Satyanarayana. "*Comparison of different topologies of Cascaded H-Bridge Multilevel Inverter*", International Conference onComputer Communication and Informatics, pp.1-6, 4th – 6th Jan. 2013.

[11] K.N.V. Prasad, G.Ranjith Kumar, Y.S. Anil Kumar, G. Satyanarayana. "*Realization of cascaded H-bridge 5-Level multilevel inverter as Dynamic Voltage Restorer*", International Conference onComputer Communication and Informatics,4th – 6th Jan. 2013.

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