A simple switching on-time calculation revision in multilevel inverter-space vector modulation to achieving extended voltage boundary operation

Bharatiraja C.¹, R.K. Pongiannan², Adedayo Yusuff³, Mohd Tariq⁴, Telugu Maddileti⁵, Tharwinkumar⁶

^{1,2,6} Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, India
 ^{1,3} Department of Electrical Engineering, University of South Africa, South Africa
 ⁴ Department of Electrical Engineering, Aligarh Muslim University, India
 ⁵ Sreenidhi Institute of Science and Technology, India

Article Info

Article history:

Received May 30, 2018 Revised Sep 20, 2018 Accepted Dec 3, 2018

Keywords:

Neutral point clamped (NPC)-MLI Overmodulation Pulse width modulation Space vector pulse width Modulation technique Three-level multilevel inverter

ABSTRACT

In inverters' pulse width modulation techniques (PWM) the Space Vector PWM (SVPWM) is a smart contestant due to its direct control in nature with variables which provide the straight forward finds to each inverter switching vector. The industrial drives are acquainting to use SVPWM owing extended speed -torque region operations. However, the extended SVPWM operation is uses much mathematical calculation to predict the switching on-times, which demands high digital platform. In order to reduce this calculation in this paper a simple on-time calculation based SVPWM is proposed. The proposed SVPWM is developed for three-level multilevel inverter and the space perspective of vector analysis are established and explained. The over modulation enhances the proper power utilization capacity of voltage source inverter thereby improve the inverter output voltage and load. This proposed method tailed the similar mathematical practice as conventional two-level SVPWM for calculating sector identification and triangle determination. The approach finds the circular and hexagonal boundary on-time based on the straightforward reference vector position identification and calculates directly the switching pulse patterns for the inverter devices using an expression based on the definition of the duty cycle. The performance of the proposed SVM is simulated by MATLAB 11.b simulation software and validated with laboratory setup 2 kW, 12 switch neutral point clamped (NPC)-MLI fed 1.5 HP squirrel cage 3-phase induction motor open loop v/f control drive. The simulation and experimental results are closure and confirming the advantages of the proposed SVM method. The proposed scheme can be extended to n-level inverter and also applicable to cascaded H-bridge topology

> Copyright © 2019 Institute of Advanced Engineering and Science. All rights reserved.

Corresponding Author:

Bharatiraja Chokkalingam, Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, 603203, India. E-mail : bharatiraja.c@ktr.srmuniv.ac.in

1. INTRODUCTION

In recent years, multilevel inverters (MLIs) have been widely used in the area of high-power medium-voltage applications. They offer a set of features that are well suited to high-voltage drive systems and power system applications such as HVDC transmission, reactive power compensation equipment [1, 2]. The Neutral Point Clamped (NPC) has been mainly used MLI for motor control and PV applications [3-6]. To control the NPC-MLI, amongst various modulation techniques, SVPWM is an attractive candidate due to

the following merits [7-9]. It directly uses the control variable given by the control system and identifies each switching vector as a point in complex space. It is useful in improving DC link voltage utilization, reducing commutation losses and Total Harmonic Distortion (THD) [10-15].

The SVPWM treats sinusoidal voltage as constant amplitude vector rotating at constant frequency with reference voltage vector V^{*}, defined by V^{*}= $|V^*|*e^{jwt}$, rotates around the centre of the space vector diagram at an angular frequency $\omega = 2\pi f_{sys}$. The space vector diagram of any *n*-level inverter consists of six sectors, *n*³ switching states and again each sector consists of $(n - 1)^2$ triangles [16]. Based upon the value of modulation index, it is classified as linear modulation and over modulation. Over modulation enhances the proper power utilization of installed capacity of voltage source inverter. The implementation of SVPWM for multilevel inverters is considered complex. This complexity is expected to increase further in the over modulation region due to the nonlinearity of this region. In the over modulation range, the trajectory of the reference vector is not completely circular, it is a combination of circular and hexagonal trajectory. The maximum output voltage can be increased up to 2Vdc/II [16, 17]. The algorithm proposed in Beig [7] to operate the inverter in the over modulation zone. The reference samples which are closer to the medium and large vectors are moved towards their respective nearest medium and nearest large vectors. This vector selection is based up on the angle correction factor [15]. In Seo *et. at.* [16] proposed a scheme for a threelevel inverter based on two-level SVPWM. The 3-level SVM diagram is divided into six two-level space vector diagrams [22, 33].

McGrath *et al.*, [17] explains the behavior of the key multilevel carrier based PWM methods for diode clamped, cascaded, and flying capacitors topologies in the over modulation region. Mondal [18] performs SVPWM based over modulation on a three-level NPC inverter. The on-time calculation equations differ for every triangular section. Due to increased computational complexity, it is cumbersome to extend this scheme to a n-level inverter. Amit kumargupta [9], the scheme easily determines the location of the reference vector and calculates on-times. Saeedifard [19] uses classification algorithm in over modulation range for SVPWM of a three-level NPC inverter and similar implementation is done by bharatiraja *et.al.*, in [21]. It is not clear, how it can be extended to a n-level inverter. In over modulation [19-21, 29, 30] modify the trajectory of reference vector by using lookup tables. The author K.M. Kwon *et.al.* [20] extends his operation in to the over modulation region, the difficulty is the timing calculations which involve some trigonometric functions. In this paper, a simple SVPWM scheme for a 3-Level NPC-MLI was developed to operate the inverter in the entire modulation region. Figure 1 shows NPC topology and Figure 2 shows the SVPWM diagram of a 3-level inverter.



Figure 1. Schematic diagram for a 3-phase 3-level NPC inverter



Figure 2. SVD for a three-level inverter

2. MODE OF OPERATIONS

In SVPWM, the three-phase voltage reference is given as a voltage reference vector V^* [13]. The modulation index is defined as,

$$M = \frac{V_1}{V_{1 \text{ Six-step}}} \tag{1}$$

The range from 0 to 0.907 is called as linear modulation and 0.907 to 1.0 is termed as over modulation range. In linear range the maximum obtainable voltage is 90.7% of the six-step value. It can be increased further by properly utilizing the DC link capacity through over modulation.

2.1. Linear Modulation ($0 \le M.I \le 0.907$)

The Figure 3 (a) shows sector-1 of space vector diagram, the tip P of the reference vector can be located in any of the 4 triangles (Δ_{10} - Δ_{13}). The objective here is to identify the triangle in which the point P is located. In the linear modulation the trajectory of the reference vector is entirely circular and it is always lies inside the hexagon.

2.2. Over Modulation-I (0.907 ≤ M.I< 0.9535)

The maximum allowable length of the reference vector happens when it touches the boundary of hexagon. Any further increase in the M.I causes the reference vector to be partially outside the hexagon which is termed as over modulation [16].

2.3. Over Modulation-II $(0.9535 \le M.I \le 1)$

Once over modulation-I has reached the upper limit, over modulation-II becomes active. Under over modulation-II the essential feature is that the particular active voltage vector that is closest to the stator voltage reference vector is used gradually longer and longer time periods [18].



Figure 3. SVM diagram for sector-1; (a) linear modulation mode, (b) OVM mode-I, (c) OVM mode-II

3. OPERATION OF 3-LEVEL INVERTER OVER MODULATION REGION

3.1. Over modulation-I

In the over modulation range shown in Figure 3 (b), the trajectory of the reference vector is not completely circular but a combination of circular and hexagonal trajectory. Sector identification and triangle determination are same for both the trajectories and they are differ only in on time calculation equations. The transition from circular trajectory to the hexagon trajectory is determined by the transition angle α_c . For $\alpha_c \leq \gamma \leq \Pi/3 - \alpha_c$, the vector moves on hexagon track and for remaining part of the sector on circular track, where α_c is given by the (2) which tells that the value of α_c is constant for a given modulation index.

$$\alpha_c = (\Pi/6) - \cos^{-1}(\Pi/(2\sqrt{3}M)) \tag{2}$$

3.1.1.Circular trajectory

For applying the SVPWM technique, firstly it is required to determine the sector which the voltage vector is within. For any given reference vector, the angle γ and its sector of operation S_k can be determined by using (3) and (4) respectively,

$$\gamma = \operatorname{rem}(\theta/60) \tag{3}$$

$$S_k = \operatorname{int}(\theta/60) + 1 \tag{4}$$

After the sector identification the triangle determination is the most important one. Each sector in the 3-level inverter can be split into four triangles Δ_i , where i = 0, 1, 2, 3. The four triangles can be split into two types for the easy determination of the triangle in the sector. The sub triangle can be categorized into

type 1- base side of the triangle is at bottom and type 2- base side of the triangle at top side. The triangle Δ_{10} , Δ_{11} , Δ_{13} belonged to the type 1 and the triangle Δ_2 , belong to type 2.Depend upon the triangle number the on-time calculations and switching pulse can be generated. The search of the triangle of the small vector (V^*) can be narrowed down by using two integers k1 and k2. They are defined by the coordinates (V_{α}, V_{β}) as,

$$k_1 = int(v_{\alpha} + v_{\beta}/\sqrt{3})$$

$$k_2 = int(v_{\beta}/h)$$
(5)
(6)

K₁ represents the part of the sector between the two lines joining the vertices, separated by distance h and inclined at 120° with respect to α -axis. From the Figure 4, K₁=0 signifies that the point V^{*} is below the line X₁ X₂. k_1 =1 signifies that point V^{*} is between line X₁ X₂ and line X₃ X₅. K₂ represents the part of the sector between the two lines joining the vertices, separated by distance h and parallel to α -axis. k₂=0 signifies that the point P is between line $X_0 X_3$ and line $X_2 X_4$. $k_2=1$ signifies that the point V^{*} is above line $X_2 X_4$. Geometrically, the values of K_1 and K_2 are an intersection of two rectangular regions which is either a triangle or rhombus as shown in Figure 4.



Figure 4. 3-level SVPWM sector-1 with sub-triangles

Knowing the values of k_1 and k_2 the coordinates ($V_{\alpha i}$, $V_{\beta i}$) of the reference vector are determined [10] by,

$$\begin{aligned}
\nu_{\alpha i} &= V_{\alpha} - k_1 + 0.5k_2 \\
\nu_{\beta i} &= V_{\beta} - k_2h
\end{aligned} \tag{7}$$
(8)

for k₁=1 and k₂=0, the common intersection is rhombus which is the combination of two triangles Δ_1 and Δ_2 . the triangle where the reference point is located can be determined by the slope comparison $V_{\beta i} \leq \sqrt{3} V_{\alpha i}$. If $V_{\beta \leq \sqrt{3}V_{\alpha i}}$ is true, then the point V * is within the triangle Δ_1 (type-1), otherwise it is within the triangle Δ_2 (type-2).

However, these on-times are modified to compensate for the loss in volt seconds during the circular trajectory by introducing a compensation factor λ . For a given modulation index M, the value of the λ is constant and it is given by

$$\lambda = (M - 0.907)/0.045 \tag{9}$$

Modified on-time equations for type-1 triangle:

 $t_a = t_a + 0.5\lambda^2 t_o$ (10) $\ddot{t}_b = \ddot{t}_b + 0.5\lambda^2 \ddot{t}_o$

(11) $t_o = T_s - t_a - t_b$ (12)

Modified on-time equations for type-2 triangle:

$$t_a = t_a - 0.5\lambda^2 t_a \tag{13}$$

$$t_b = t_b - 0.5\lambda^2 t_b \tag{14}$$

$$\iota_0 = I_s - \iota_a - \iota_b \tag{13}$$

3.1.2. Hexagonal trajectory

If the angle γ , satisfies the condition $\alpha_c \leq \gamma < \Pi/3 - \alpha_c$, means that the reference vector follows the hexagonal trajectory. During hexagonal trajectory the coordinates of tip P of the vector are given in terms of angle γ and level n, as

$$V_{\alpha} = \sqrt{3} (n-1)/(\sqrt{3} + \tan \gamma)$$
(16)
$$V_{\beta} = \sqrt{3} (n-1) \tan \gamma / (\sqrt{3} + \tan \gamma)$$
(17)

The sector judgment and triangle determination can be done in the similar manner of circular trajectory. The search of the triangle of the small vector (V^*) can be narrowed down by using two integers k_1 and k_2 . They are defined as

$$k_1 = (n-2)$$
 (18)
 $k_2 = int(V_\beta/h)$ (19)

by knowing the values of k_1 and k_2 the value of the triangle number can be obtained by using the (20) and the coordinates of the small vector V_s are given by the (21) and (22).

$$\begin{aligned} \Delta_{j} &= k_{1}^{2} + 2k_{2} \end{aligned} (20) \\ V_{\alpha o}^{s} &= V_{\alpha} - k_{1} + 0.5k_{2} \end{aligned} (21) \\ V_{\beta 0}^{s} &= V_{\beta} - k_{2}h \end{aligned} (22)$$

on time calculation equations are similar to two-level inverter and are determined by using the (23)-(25_.

$$t_a = T_s (V_{ao}^s - V_{\beta o}^s / \sqrt{3})$$

$$t_b = T_s - t_a$$
(23)
(24)

$$t_o = 0 \tag{25}$$

3.2. Over modulation -11

Once over modulation-I has reached the upper limit, over modulation-II becomes active. Switching in over modulation-II is characterized by a hold angle \propto_h [21], defined as

$$\alpha_h = 10.5(1.05 - 1/M) \tag{26}$$

For $\alpha_h \leq \gamma < \Pi/3 - \alpha_h$, the vector moves on hexagon track and the on-time calculation is same as that during the hexagonal trajectory in over modulation mode Iand for remaining part of the sector i.e., $\alpha_h \leq \gamma < \Pi/3 - \alpha_h$ and $0 \leq \gamma < \alpha_h$ and $\Pi/3 - \alpha_h \leq \gamma < \Pi/3$ the vector is held at one of the large vector. In Figure 3 (c) the square dots at the points 4',3', 2' and 1' represent the reference vector samples in over modulation mode II. The samples 4',3' are closer to the large vector L₁ and they are moved towards the large vector L₁ and the samples 2',1', are closer to the large vector L₂ and they are moved towards the large vector L₂.

If the reference vector makes an angle, $0 \le \gamma < \pi/6$ then the vector is held at large vector L₁ as shown in Figure 3 (c) and the on-time equations are

$$t_a = T_s, t_o = 0, t_o = 0 \tag{27}$$

If the reference vector makes an angle, $\Pi/6 \le \gamma < \Pi/3$ then the vector is held at large vector L₂ as shown in Figure 3. (c) and the on-time equations are

$$t_a = 0, t_b = T_s, t_o = 0 \tag{28}$$

Figure 5 show the flowcharts for entire modulation index for linear and over modulation.



Figure 5. Main flowchart for entire modulation index

4. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed SVM have been investigated and simulated by MATLAB 11.b for 12 switch NPC-MLI with 300V DC-link, two 100μ F capacitor, 5kHZ switching frequency fed 1.5 HP squirrel cage 3-phase induction motor open loop v/f control drive. Further the simulation is extended to laboratory scale experimental power circuit is shown in Figure 6.



Figure 6. Experimental set up-SVM based 3 Level NPC-MLIFPGA SPARTEN III

The proposed over modulation SVPWM algorithm is programmed in Verilog Hardware Descriptive Language (VHDL) code and synthesized in minimum computational load using SPARTAN –III-3AN – XC3S400 FPGA family board [16]. The algorithm is tested on a 3-level NPC laboratory prototype inverter with 300V DC-link, two 100 μ F capacitor, 5kHz switching frequency fed 1.5 HP squirrel cage 3-phase induction motor open loop v/f control drive. Figure7shows the line voltage for a 3-level NPC-MLI for 0.907, 0.957, and 0.99 modulation index respectively.

5. RESULT DISCUSSION

Figure8 depicts the M.I versus line voltage for a 1.5 HP squirrel cage 3-phase induction motor fed from a NPC MLI for the proposed SVM scheme including overmodulation. From the graph it was observed that the output line voltage is 248V at M=0.8 and at the M=0.952 it was found that the output line voltage is

279 V. Therefore it is evident that the output voltage of the inverter gets increased as the operating value of M moves towards the over modulation region.



Figure 7. Shows the line voltage for a 3-level NPC-MLI for (a) 0.907, (b) 0.957, (c) 0.99 M_a respectively



Figure 8. Motor speed versus M. for a 3-level NPC-MLI.

M.I	Simulation results output motor voltage speed	Hardware results output motor voltage speed
0.800	248 928	246 927
0.906	260 1287	257 1282
0.938	273 1401	272 1396
0.952	280 1413	279 1411
0.998	293 1423	291 1422

A simple switching on-time calculation revision in multilevel inverter-space vector ... (Bharatiraja C)

6. CONCLUSION

This paper proposes a simple SVPWM technique for calculating the on-times in the entire modulation region, the on-times calculation is based on on-time calculation for two-level SVPWM. A simple method of calculating on-times in the over modulation range is used, hence, a solution to complex equations and lookup tables are not required. The proposed algorithm can be applied to a variety of modulation values and it can be easily applicable for any level inverter and to all the types of multilevel topologies. The experimentation validating the proposed RPWM. & AI can be extended to a broad range of applications such as driverless vehicles.

REFERENCES

- J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, control, and applications", *IEEE Trans. Ind. Electron.* Vol. 49, No. 4, pp. 724–738, Aug. 2002.
- [2] H. Abu-Rub, J. Holts, J. Rodriguez, and G. Baoming, "Medium voltage multi level converters, state of the art, challenges and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2581–2596, Aug. 2010.
- [3] C. Bharatiraja, R. Selvaraj, T. R. Chelliah, J. L. Munda, M. Tariq, and A. I. Maswood, "Design and Implementation of Fourth Arm for Elimination of Bearing Current in NPC-MLI-Fed Induction Motor Drive," *IEEE Transactions on Industry Applications*, Vol. 54, No. 1, pp. 745–754, Jan. 2018.
- [4] C. Bharatiraja, S. Jeevananthan, J.L. Munda, and R. Latha, "Improved SVPWM vector selection approaches in OVM region to reduce common-mode voltage for three-level neutral point clamped inverter," *International Journal of Electrical Power & Energy Systems*, Vol. 79, No. 1, pp. 285–297, Oct. 2016.
- [5] G.Prakash, C.Subramani, C. Bharatiraja, and M.Shabin, "A low cost single phase grid connected reduced switch PV inverter based on Time Frame Switching Scheme," *International Journal of Electrical Power & Energy Systems*, Vol. 77, pp. 100-111, March 2016.
- [6] C.Bharatiraja, S.Jeevananthan, Latha, R., "FPGA based practical implementation of NPC-MLI with SVPWM for an autonomous operation PV system with capacitor balancing", *International Journal of Electrical Power and Energy Systems*, Vol. 61, pp.489-509, Oct 2014.
- [7] Abdul Rahiman Beig, "Synchronized SVPWM algorithm for the over modulation region of a low switching frequency medium-voltage three-level VSI," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 12, Dec. 2012.
- [8] C. Bharatiraja, T. B. Prasad, and R. Latha, "Comparative realization of different SVPWM schemes in linear modulation using FPGA," 2008 IEEE Region 8 International Conference on Computational Technologies in Electrical and Electronics Engineering, Novosibirsk Scientific Centre, Novosibirsk, Russia.21-25 July 2008.
- [9] Amit Kumar Gupta and Ashwin M. Khambadkone, "A General Space Vector PWM Algorithm for Multilevel Inverters, Including Operation in Over modulation Range," *IEEE Trans. on Power Electron.*, Vol. 22, No. 2, March 2007.
- [10] C. Bharatiraja, P. Sanjeevikumar, and F. Blaabjerg, "CriticalInvestigation and ComparativeAnalysis of Advanced PWM TechniquesforThree-PhaseThree-Level NPC-MLI Drives," *Electric Power Components and Systems*. Vol. 46, No. 3, pp. 258–269, Feb. 2018.
- [11] Bharatiraja, C., Harish, S., Munda, J.L., (...), SriramKumar, M., Bhati, V. "A PWM strategies for diode assisted NPC-MLI to obtain maximum voltage gain for EV application", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, Vol.8, No.2, pp. 767-774, June 2017.
- [12] Santhakumar, C., Shivakumar, R., Bharatiraja, C., Sanjeevikumar, P. "Carrier shifting algorithms for the mitigation of circulating current in diode clamped MLI fed induction motor drive ", *International Journal of Power Electronics and Drive System (IJPEDS)s*, Vol.8, No.2, pp. 844-852, June 2017.
- [13] C. Bharatiraja, K. V. R. S. P. Rao, R. Palanisamy, and S. Jeevananthan, "Critical Evaluation of SVPWM Scheme for Capacitor balancing in NPC-MLI," *IET Chennai 3rd International Conference on Sustainable Energy and Intelligent Systems (SEISCON 2012)*, India, 27-29 Dec. 2012.
- [14] C. Bharatiraja, P. Sanjeevikumar, J. L. Munda, L. Norum, and S. Raghu, "Mitigation of Circulating Current in Diode clamped MLI fed Induction Motor Drive Using Carrier Shifting PWM Techniques," *Lecture Notes in Electrical Engineering*, pp. 71–83, Dec. 2017.
- [15] C Bharatiraja, N Sriramsai, "Investigation of the Common Mode Voltage for a Neutral-Point-Clamped Multilevel Inverter Drive and its Innovative Elimination through SVPWM Switching-State Redundancy", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, Vol.3, No.7, pp. 892-900, Dec 2016.
- [16] J. H. Seo, C. H. Choi, and D. S. Hyun, "A new simplified space-vector pwm method for three-level inverters," *IEEE Trans. Power Electron.*, Vol. 16, No. 4, pp. 545–550, Jul. 2001.
- [17] B. P. McGrath and D. G. Holmes, "Sinusoidal PWM of multilevel inverters in the over modulation region," Proc. IEEE 33rd Annu. PowerElectron. Spec. Conf. (PESC), Vol. 2, pp. 485–490, Jun. 2002.
- [18] S. K. Mondal, B. K. Bose, "Space vector pulse width modulation of three-level inverter extending operation into over modulation region," *IEEE Trans. Power Electron.*, Vol. 18, No. 2, pp. 604–611, Mar. 2003.
- [19] Saeedifard, A. R. Bakhshai, G. Joos, and P. Jain, "Extending the operating range of the neuro-computing of threelevel inverters into over modulation region," *Proc. IEEE 38th Ind. Appl. Conf.*, Vol. 1, pp. 672–677.vector classification space vector modulation algorithm Oct. 2003.

- [20] Kyoung-Min Kwon, Jae-Moon Lee, Jin-Mok Lee, M. "Over modulation Scheme of Three-Level Inverters for Vector Controlled Induction Motor Drives," *Journal of Power Electronics*, Vol. 9, No. 3, May 2009.
- [21] C. Bharatiraja, S. Jeevananthan and JL munda "Timing Correction Algorithm for SVPWM Based Diode-Clamped MLI Operated in overmodulation Region", *IEEE journal of Selected topics in Power Electronics applications*. Vol. 6, No. 1, pp. 233-245, Mar. 2018
- [22] C. Bharatiraja, P. Sanjeevikumar, and F. Blaabjerg, "Critical Investigation and Comparative Analysis of Advanced PWM Techniquesfor Three-PhaseThree-Level NPC-MLI Drives", *Electric Power Components and Systems*. Vol. 46, No. 3, pp. 258–269, Feb. 2018
- [23] C.Bharatiraja, S.Jeevananthan, Latha, R., "FPGA based practical implementation of NPC-MLI with SVPWM for an autonomous operation PV system with capacitor balancing", *International Journal of Electrical Power and Energy Systems*, Vol. 61, pp.489-509, Oct 2014
- [24] C. Bharatiraja, Harshavardhan Reddy, N. Sri Ramsai, and Sunkavalli Satya Saisuma "FPGA Based Design and Validation of Asymmetrical Reduced Switch Multilevel Inverter," *International Journal of Power Electronics and Drive System (IJPEDS)*, Vol. 7, No. 2, pp. 340-348, June 2016.
- [25] C.Bharatiraja, S. Jeevananthan, S, R. Latha, and V.Mohan, "Vector selection approach-based hexagonal hysteresis space vector current controller for a three phase diode clamped MLI with capacitor voltage balancing," *IET Power Electronics.*, Vol. 9, No. 7, pp. 1350-1361, June 2016.
- [26] Bharatiraja, C., Sanjeevikumar, P., Mahesh, Swathimala, A.S., Raghu, S. "Analysis, design and investigation on a new single-phase switched quasi Z-source inverter for photovoltaic application", in *International Journal of Power Electronics and Drive Systems (IJPEDS)*, Vol.8, No.2, pp. 853-860, June 2017.
- [27] C. Bharatiraja, Reddy, H. Sri Ramsai, N, Saisuma, S.S. "FPGA based design and validation of asymmetrical reduced switch multilevel inverter", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, Vol.7, No.2, pp. 340-348, June 2016.
- [28] C.Bharatiraja, S.Raghu, and K.R.S.Rao, "Comparative analysis of different PWM techniques to reduce the common mode voltage in three-level neutral-point- clamped inverters for variable speed induction drives", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, Vol 3, No 1, pp. 105-116, March 2013.
- [29] C.Bharatiraja, R.Latha, S.S.Dash, R.Gulati, R, and P.V Sharma, "A 3D-SVPWM algorithm design and its FPGA IP-core implementation for MLIS operating over a wide modulation range", *International Review of Electrical Engineering*, vol.8, no. 3 pp. 947-961,2013.
- [30] C. Bharatiraja, S. Jeevananthan and S. S. Dash, "A Vector Selection Approach Based on Control Degree of Freedom to Provide DC-Link Voltage Balancing in Diode Clamped Multilevel Inverter", *International Review of Electrical Engineering*, Vol.8, No. 1 pp. 39 – 51, Jan-Feb 2013.