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DC transformer modeling and control of DC-DC buck converter

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ABSTRACT

Switching Power Converters convert one form of power to another with high efficiency and accurate control. One of the most widely used DC-DC Converter is Buck Converter. Control is invariably required to maintain the output voltage/current in spite of variations in source/load. In order to design the controller and gain insight into the system, a dynamic model needs to be developed. Modeling techniques widely used are state-space averaging and PWM switch model. In this paper, a DC transformer modeling technique is used to develop the averaged model of the converter. One of the advantages of this model is that it can be implemented in Spice simulator using basic circuit elements. The same model can be used for time domain as well as frequency domain analysis. Analog type-II compensator is designed to compensate the system. Simulation and experimental results for start-up transient and load transient are shown to validate the model.

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319

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1. INTRODUCTION

Power converters change electrical power from one form to another with very high efficiency and accurate control.DC-DC conversion is a common function performed by power converters, in which the voltage of DC is changed and possibly regulated. To regulate the output voltage or current a controller is required that adjusts the control input to regulate the desired quantity. In order to design a controller, a mathematical model of the system is required. A good model incorporates the dominant behavior of the system, ignore the insignificant phenomena. Once basic insight is gained the model can be refined to incorporate some of the previously neglected phenomena [1].

Previously, many techniques have been proposed for modeling of a converter. Large signal modeling produces a non-linear model of the converter [2]. Since simulations shown in this paper are carried out using LTSPICE, therefore a linearized small signal model was used. Ref [3] discusses the averaged small signal modeling for a buck converter with average current mode control. In [4] an averaged small signal model is used which requires an additional correction factor to be included to match the output voltage of aver-aged model with that of the actual circuit. In [5], a non-linear controller is used whereas in [6], both non-linear as well as linear controllers are implemented on buck converter. In [7], [8] DC transformer modeling approach is used which is a graphical approach with minimum use of equations. This makes it easier to derive transfer functions from a final canonical model of the buck converter and any kind of controller design becomes

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easy.Ref [9], [10] discusses different control techniques and its analysis. Digital control techniques are discussed in [11], [12].

In [13] state space averaging is used to model the plant disturbance due to load variation. In [14] large signal non-ideal averaged model of the DC-DC buck converter is implemented using S- function. The proposed model is validated by comparing the open loop response of MATLAB with Saber. The controller in a Buck Converter must manage the transients. Load transients are managed by controllers and inrush current during power-up is managed by soft start circuit [15]. In [16] additional feedback is used using a capacitor multiplier from the output of the converter to the input of the error amplifier. It helps to control the converter output ramping speed during power up.

Different types of modeling techniques are used to model the dynamic behavior of the buck converter. DC transformer modeling technique which is a graphical approach is less explored. Models developed in previous work doesn't take into account dynamics during the start-up. This paper discusses DC transformer modeling of a voltage mode controlled DC-DC buck converter. The developed model is implemented in LTSpice simulator. The uniqueness of this model is that non-idealities can be easily incorporated using resistors and voltages sources, for example, diode voltage drop, MOSFET on-resistance etc. Start-up transient and load transient are analyzed using a type-II controller. Finally, simulation results are compared with hardware results to validate the model.

Section 2 describes the small signal DC transformer model of Buck Converter and its implementation in LTSpice. Controller design is presented in section 3. Finally experimental results of the prototype are provided and compared with the simulation results.

2. SMALL SIGNAL MODELING OF BUCK CONVERTER

Small modeling of a converter is required to represent the physical behavior by mathematical means. For example how do ac variations in source voltage $v_g(t)$, load R or duty cycle d(t) affect the output voltage v(t). While developing a model, only dominant behavior of the system needs to be taken into account. Figure 1 shows a Buck converter and (1) and (2) shows the steady state inductor current and capacitor voltage respectively.

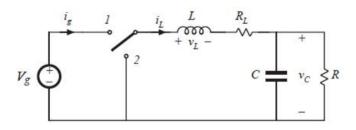


Figure 1. Buck Converter

Switch in position'1'

Inductor voltage is shown in (1)

$$v_L(t) = L\frac{di_L}{dt} = v_g(t) - v(t) \tag{1}$$

Capacitor current is shown in (2)

$$i_c(t) = C \frac{dv(t)}{dt} = i_L(t) - \frac{v(t)}{R}$$
 (2)

Using small ripple approximation switching ripple is neglected and switching harmonics can be removed by averaging all waveforms over one switching period T_s [7].

Moving average of a variable x(t) over a time period T_s is shown in (3)

$$\langle x(t) \rangle_{T_S} = \frac{1}{T_S} \int_{t+\frac{T_S}{2}}^{t+\frac{T_S}{2}} x(\tau) d\tau$$
 (3)

All the variables in (1) and (2) are replaced with its moving average values yielding (4) and (5)

$$< v_L(t)>_{T_S} = L \frac{d < i_L >_{T_S}}{dt} = < v_g(t)>_{T_S} - < v(t)>_{T_S}$$
 (4)

$$\langle i_c(t) \rangle_{T_s} = C \frac{d \langle v(t) \rangle_{T_s}}{dt} = \langle i_L(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R}$$
 (5)

Switch in position '2'

$$v_L(t) = -v(t) \tag{6}$$

$$i_c(t) = i_L(t) - \frac{v(t)}{R} \tag{7}$$

Using small ripple approximation

$$\langle v_L(t) \rangle_{T_S} = -\langle v(t) \rangle_{T_S}$$
 (8)

$$\langle i_c(t) \rangle_{T_s} = \langle i_L(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R}$$
 (9)

Averaging inductor voltage (4) and (8)

$$\frac{d < i_L >_{T_S}}{dt} = d(< v_g >_{T_S} - < v >_{T_S}) + d'(- < v >_{T_S})$$
(10)

Averaging capacitor current (5) and (9) over one switching period.

$$C\frac{d < v >_{T_S}}{dt} = d\left(< i_L >_{T_S} - \frac{< v >_{T_S}}{R} \right) + d'\left(< i_L >_{T_S} - \frac{< v >_{T_S}}{R} \right)$$
(11)

The source current of buck converter is discontinuous and needs to be averaged.

$$\langle i_q \rangle_{T_s} = d \langle i_L \rangle_{T_s} \tag{12}$$

2.1. Perturbation and Linearization

Consider the two independent inputs, source voltage $\langle v_g(t) \rangle_{T_s}$ and duty cycle d(t) of buck converter. Perturbing the inputs with low frequency ac variations $(\hat{v}_g \text{ and } \hat{d})$ which are small in magnitude when compared to steady state DC values V_g and D. Applying $\langle v_g \rangle_{T_s} = V_g + \hat{v}_g$ and $d = D + \hat{d}$ as inputs to the converter perturbs the inductor current and output voltage as shown in (13) and (14) respectively.

$$\langle i_L \rangle_{T_c} = I_L + \hat{\iota}_L \tag{13}$$

$$\langle v \rangle_{T_c} = V + \hat{v} \tag{14}$$

From (10), (11) and (12) can now be rewritten as shown in (15), (16) and (17) respectively.

$$L\frac{d(I_L + \hat{t}_L)}{dt} = (D + \hat{d})(V_g + \hat{v}_g - V - \hat{v}) + (D' - d)(-V - \hat{v})$$
(15)

$$C\frac{d(V+\hat{v})}{dt} = I_L + \hat{\iota}_L - \frac{V}{R} - \frac{\hat{v}}{R} \tag{16}$$

$$I_g + \hat{\imath}_g = (D + \hat{d})(I_L + \hat{\imath}_L) \tag{17}$$

From (15), (16) and (17) are non-linear equations, and can be linearized by assuming $\hat{v}(t) \ll V(t)$, $\hat{v}_g(t) \ll V_g(t)$, $\hat{i}_L(t) \ll I_L(t)$, $\hat{d}(t) \ll D(t)$.

322 **I**ISSN: 2088-8694

In these equations, average value of DC terms is zero and second order terms can be neglected due its smaller magnitude and remaining first order terms are shown in (17),(18) and (19) respectively. The three equations completely describe the dynamic behavior of buck converter.

$$L\frac{d\hat{\imath}_L}{dt} = \hat{d}V_g + D\hat{v}_g - \hat{v} \tag{18}$$

$$C\frac{d\hat{v}}{dt} = \hat{\imath}_L - \frac{\hat{v}}{R} \tag{19}$$

$$\hat{\imath}_g = D\hat{\imath}_L + \hat{d}I_L \tag{20}$$

3. DC TRANSFORMER MODEL OF BUCK CONVERTER

DC transformer modeling is a theoretical concept which is used to obtain the control-to-output transfer function $G_{vd}(s)$. The system can be modeled using independent, dependent sources and passive elements. Figure 2 depicts the inductor loop model using (18). From (19) shows that inductor current is equal to the sum of the capacitor and load current. We can replace the voltage source $\hat{v}(t)$ with the capacitor loop as depicted in Figure 3.

Input voltage source \hat{v}_g is not present in the model shown in Figure 3. Input side model can be developed using (20) as shown in Figure 4. Circuit models in Figures 3 and 4 can be combined to get the complete system model as shown in Figure 5. The dependent current source $D\hat{\iota}_L(t)$ and dependent voltage source $Dv_g(t)$ can be replaced with a DC transformer with conversion ratio 1: D as shown in Figure 6.

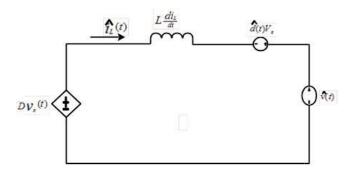


Figure 2. Inductor loop model

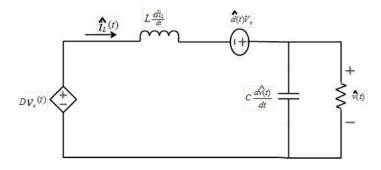


Figure 3. Model with capacitor loop inserted

The expression for control to output transfer function $G_{vd}(s)$ can be obtained by assuming source disturbance $\hat{v}_g(s)$ is zero and then pushing all the elements in the primary side to the secondary side of DC transformer. Simplifying the circuit removes the DC transformer from the model as shown in Figure 7 and now it can be modeled in LTSPICE using behavioral voltage source and basic circuit elements.

System parameters under consideration are depicted in Table 1. The specifications are taken from Buck Converter available on ASLK PRO Kit [17]. Figure 8 shows the uncompensated system response realized in LTSPICE. In order to obtain the frequency response of the system, an AC source is placed between output and feedback network.

Table 1. System parameters

Description	Parameter	Value
Input Voltage	V_{q}	10V
Output Voltage	V_0	5V
Inductance	L_1	33μΗ
Capacitance	C_1	660µF
Capacitor ESR	r_c	0.1Ω
Switching Frequency	f_s	400KHz
Reference Voltage	V_{ref}	0.7V

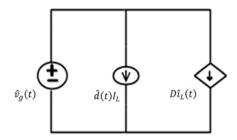


Figure 4. Input side model

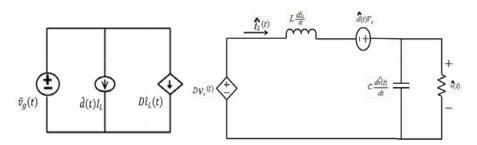


Figure 5. Combined system model

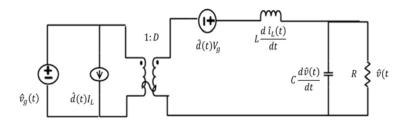


Figure 6. Buck coverter DC transformer model

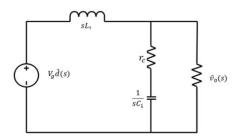


Figure 7. Simplified DC transformer model

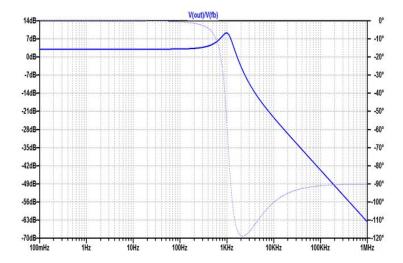


Figure 8. Uncompensated system response

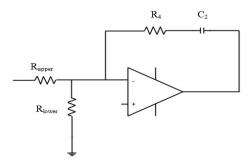


Figure 9. Type-II Compensator

4. COMPENSATOR DESIGN

The uncompensated system response in Figure 8 shows a phase transition of -90° at the corner frequency of 3 KHz. A type-II compensator as shown in Figure 9 is suitable for such type of system.

$$G_c(s) = G_{co} \frac{\left(1 + \frac{s}{\omega_s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \tag{21}$$

From 21 depicts the transfer function of the compensator, where $G_{co} = \frac{R_2}{R_{upper}}$, $\omega_z = \frac{1}{R_2 C_1}$ and $\omega_p = \frac{1}{R_{upper} C_1}$. The compensator is designed for a gain cross over frequency $f_c = 4KHz$ and Phase Margin =60°. The zero of the compensator is placed at $f_z = 340Hz$ and pole at $f_p = 48KHz$.

The simulation model uses LT1013 op-amp to realize the compensator as shown in Figure 10. The gain-bandwidth product of LT1013 is 1.5MHz which is same as the integrated op-amp available in TPS40200 controller chip [18]. TPS40200 is used for hardware realization of the compensator. The output voltage V_{out} is scaled down using the voltage divider network comprising of two resistors in parallel that make up R_{lower} . The reference voltage $V_{ref} = 0.7V$, realized using voltage source V_3 and modulator gain $V_m = \frac{V_g}{10}$. V_c is the output of the compensator, which in turn will control the value of behavioral voltage source B_1 . Figure 11 shows the compensated system frequency response.

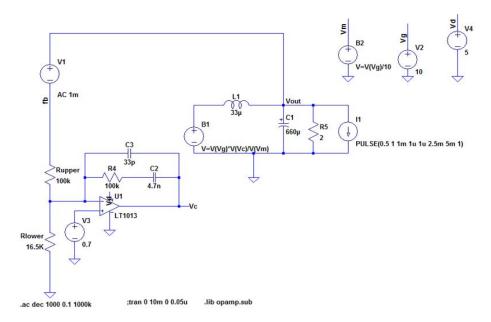


Figure 10. Compensated system

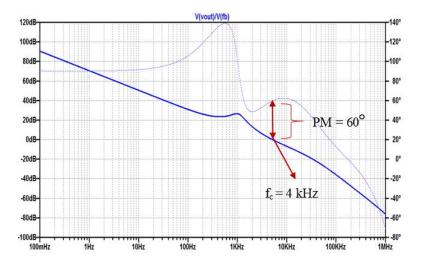


Figure 11. Compensated system frequency response

5. EXPERIMENTAL RESULTS

Once the compensator is designed its effectiveness needs to be tested. Two standard tests that are carried out for power converters are start-up transient test and load transient test.

5.1. Start-up Transient Test

During turn-on, there will be inrush current which can damage the switches and inductor. TPS40200 controller chip has a programmable soft-start pin. The capacitor connected to the soft start pin determines the start-up transient time t_{ss} . The simulation model in Fig. 5 is used to determine the appropriate t_{ss} . Soft start is implemented in simulation model using PWL voltage source, which ramps up the reference voltage from 0 to 0.7V in the specified time. Figure 12 shows the inductor current and output voltage for different t_{ss} .

Simulation results clearly indicate $t_{ss} = 10ms$ gives the minimum inrush current and output voltage overshoot. To obtain the same result in hardware, t_{ss} is programmed to 10ms by connecting a 470nF capacitor to soft start pin of TPS40200. Figure 13 shows hardware results for start-up transient.

5.2. Load Transient Test

Figure 15 shows the simulation result for a step change in load from 0.5 A to 1 A. The output voltage recovers smoothly without any ringing. The recovery time is $\approx 260\mu s$. Figure 10 shows the hardware result for load transient test. Recovery time is considerably less for hardware result because additional two $10\mu F$ ceramic capacitors are used along with the output capacitor to shape the V_{out} recovery.

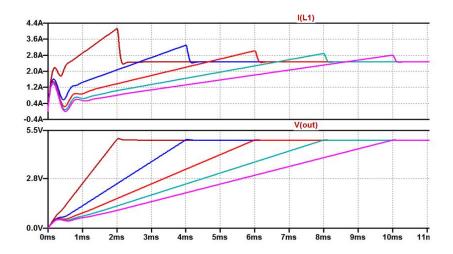


Figure 12. Simulation of startup transient with soft start

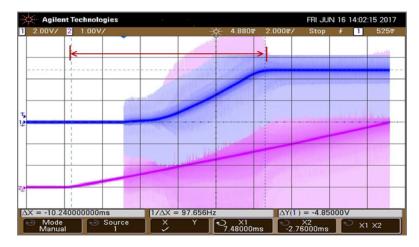


Figure 13. Start-up transient, CH1: Output voltage CH2: Soft start capacitor voltage

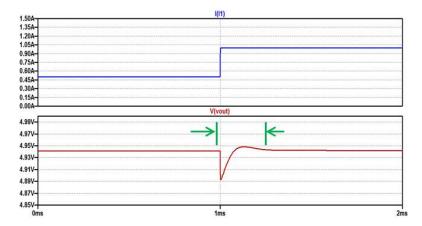


Figure 14. Simulation of transient response when load changes from 0.5A to 1A

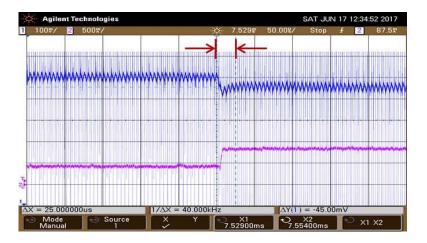


Figure 15. Transient response when load changes from 0.5A to 1A, CH1: Output voltage, CH2: Load current

6. CONCLUSION

This paper represents a graphical method for small signal modeling of DC-DC converters. The main advantage of this model is it can be implemented in SPICE simulator using basic circuit elements, independent and dependent sources. Start-up transient dynamics also can be determined using this model, which in turn is used to design the soft-start capacitor for the analog controller IC. Further, the simulation results are compared and it is observed that the hardware results are as expected from simulation which affirms the developed model is valid and reliable.

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