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A Novel DC-AC Inverter Topology to Eliminate Leakage Current

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ABSTRACT

Experiments confirmed that Transformerless Inverters (TIs) deliver more reliability and higher energy efficiency. Nonetheless, one of the shortcomings of TIs is the leakage current that occurs between the photovoltaic (PV) string terminals and the ground. Such a drawback is justified by the non-galvanic isolation caused by the transformer being omitted. As such, this study is intended to develop a novel TI inverter topology for solar PV systems. The latter is meant to remove the leakage current and enhance the operating system of the entire PV conversion as well. Added to its null zero-crossing distortion and capability regarding energy efficiency, the developed TI, being validated by simulation and experiment, eradicated the leakage current.

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1. INTRODUCTION

Transformerless inverters (TIs) are found to be more energy efficient, highly effective and perfectly compact compared to regular inverters equipped with high frequency or low frequency transformers. Though the fine performances of such TIs, their integration in PV systems has revealed some shortcomings. The leakage current circulation, occurring when the transformer is omitted due the galvanic non-isolation, is a typical example of these drawbacks [1]-[4]. This is to say that even though TIs are the most topologies being used nowadays in photovoltaic aplications due to their high efficiency, small size and low weight; avoiding the grid-side or the DC-side transformer requires some modulation techniques applied to novel topologies in order to mitigate DC current components from the grid and the leakage current that takes place between the PV module and the ground.

Given that Voltage Source Inverters (VSIs) display high power factor owing to pulse width modulated (PWM) control strategies being implemented, they are known to be the most inverters utilized in photovoltaic applications [5]-[8]. Needless to say, the current source inverters (CSIs) are being used for medium and high power applications in general.

So far, numerous famous topologies have been invented, tested and are currently commercially available. As commonly reported in the literature, the enumerated VSI topologies are classified into two families: Inverters including transformers, no matter it is a HF or a LF transformer and the inverter where the transformer is omitted known as “Transformerless inverter” [9]-[11].

By means of a HF transformer, the so-called Flyback topology is galvanically isolated. Such topology, where the output terminals are being connected to a center-tapped transformer, deploys a low power inverter. The transformer outputs are feeding the rest of the circuit [12]. The main shortcoming of this

topology is that the zero-crossing distortion phenomenon has not been eliminated. Furthermore, this topology is bulky and big in size due to the electrolytic capacitors having large values.

[13],[14] developed a novel topology includes a buck-boost chopper which minimized the size of the electrolytic capacitors and thus it improved the compactness of the topology. The proposed topology in [13],[14] is inspired from the Flyback topology and is, nonetheless, harmed by voltage spikes due to the leakage inductance of the transformer [15]. Having said that, [15], developed a quite enhanced topology by using a dual switch inverter instead of the single-switch one being used in the topology of [13],[14]. Such modified topology is the so-called "modified Shimizu inverter" [15].

The isolated inverter available in parallel-parallel configuration, as suggested in [16], can be recognized as transformer-equipped topology. It is an inverter topology where the output terminals of the conversion stages are interconnected in semi-parallel way to the output terminals of the transformer. In this topology, each stage is devoted to one half-cycle.

Both Nagao and Harada suggested in [17] a different design of the conventional Flyback inverter topology that is based on both, serial and parallel interconnections. Such inverter uses a number of two independent Flyback converters where their outputs are linked in series to the grid; whereas, their inputs are linked in parallel to photovoltaic module.

Despite the huge number of inverters topologies developed so far and that most of them are commercially available, still the neutral point clamped (NPC), the HERIC, the H5 and the conventional H-bridge inverters are the most known topologies exhibiting high energy efficiency and quite low leakage current level. Regularly, the H-bridge TI, being constituted of two branches of transistors, is deployed in variable speed drives for UPS power supplies and AC motors as well. The techniques of the different PWM could be implemented [18] with regard to its strategies of control. The inverter output voltage has shown large fluctuations producing a considerable leakage current through the parasitic capacitances, which could take place if a path between the earth and the PV module exists. In order to lessen this leakage current, an LCL filter, is in general inserted.

Sunways introduced The HERIC TI that blends the advantages of both the unipolar modulation (having highly efficient) and the bipolar one (having low leakage current) [19]. This inverter topology is based on the conventional full-bridge topology with an extra AC-bypass branch. Throughout the sequences of freewheeling, an extra two-transistor branch is deployed. One of the two transistors is switched ON; meanwhile, the four H-bridge transistors are switched OFF during every half cycle in such a way the grid gets completely disconnected from the PV source and the energy remains at the load side. Until date, the HERIC topology is considered one of the best inverter topologies in terms of energetic efficiency and power quality.

In [20], Calais et al. developed a topology also based on the conventional full bridge with a fifth transistor at the DC side to completely disconnect the DC source from the grid. The developed topology is the so-called H5 TI. Such topology exhibits a quite high energetic efficiency but it is penalized by a relatively high leakage current level.

An other well known topology called the neutral point clamped (NPC) TI has been developed by Rahman and Zahong suggested in [21]. In such topology, the two output terminals of the inverter are being clamped to middle of the DC bus. Such topology is acknowledged to have lessened ripple current, low switching losses, and three level voltages. The latter reduces in return the output filter size. In addition, the inverter is characterized by a power factor close to the unity. However, the NPC inverter requires high DC voltage at its input terminals, a voltage.

Selmi et al. propounded in [22] an inverter topology with no transformer for photovoltaic applications. This topology displays low leakage current, higher standards of efficiency and a nearly null zero-crossing distortion. The developed topology. Compared to the full-bridge topology, the developed topology has two extra transistors inserted at the AC side to disconnect the inverter from the grid when the zero-voltage of the control strategy is applied to the four main transistors of the topology. The control strategy of such topology has been implemented by means of a low cost microcontroller, which minimizes the cost of the inverter.

In light of the above, this paper analyses the origin of the common-mode voltage and leakage current through the stary capacitances. The analysis was based on the conventional full-bridge inverter topology from which all topologies listed next are derived. In an attempt to solve the previously mentioned shortcomings, this paper presents a novel transformerless intverter topology characterized by hight efficiency, a null leakage current level and a pure sinewave having no zero-crossing distortions. The proposed topology has been comparated to most famous transformerless topology and a slight superiority in terms of leakage current level and zero-crossing distortion has been obtained. To confirm its superiority over existing TIs, the proposed topology has been simulated and the obtained results have been compared to those of the HERIC and and exprerimentally validated.

2. LEAKAGE CURRENT VERSUS COMMON MODE VOLTAGE

2.1. Transformer-Based Inverters

As illustrated in Figure 1, the inverter is equipped with a transformer at the AC side.

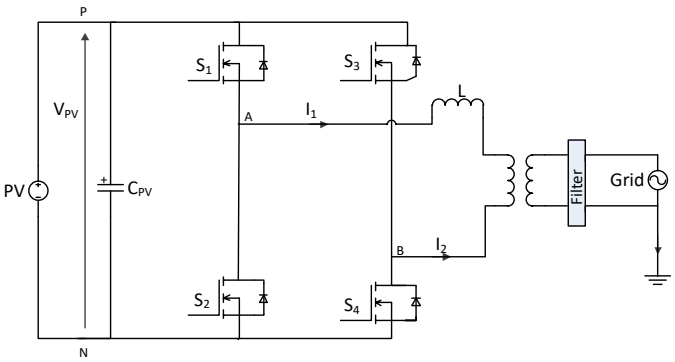

Figure 1. Transformer-base inverter topology

As for PV conversion systems, the frequent implementation of a capacitance leakage is aimed at accounting the path of the current between PV modules and the ground [23],[24]. This current is nothing but the common-mode current I_{cm}. Figure 2 illustrates all possible paths that can occur between the ground and the PV conversion system including PV modules.

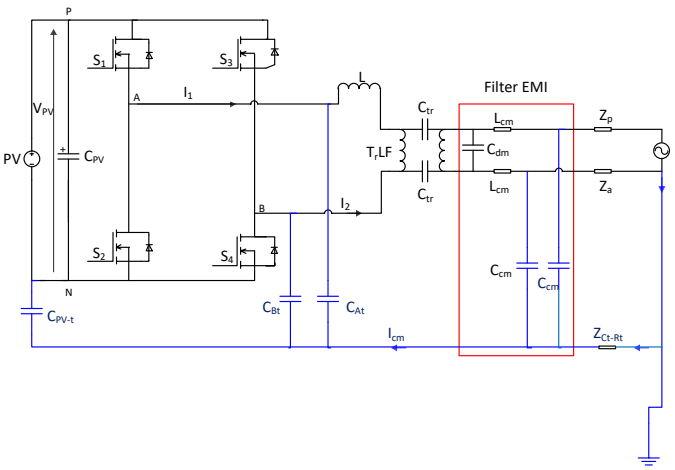

Figure 2. Basic single-phase PV system topology including parasitic elements

The parasitic capacitance, $C_{PV\text{-}t,}$ shown in Figure 2 represents the path between the ground (earth) and the PV system. The value of such capacitance depends on many parameters such as humidity, dust covering the PV module, etc. In Figure 2, the capacitances $C_{A\text{-}t}$ and $C_{B\text{-}t}$ represent the parasitic capacitances between the inverter output terminals and earth. Another capacitance which is of great importance exists between the connections points of earth and the network is represented by $Z_{CT\text{-}Rt}$. Finally, the phase, neutral and transformer stray capacitance are represented respectively by Z_p, Z_n and C_{tr}.

For inverters equipped with a transformer, no matter it is a HF or LF transformer, the common-mode current I_{cm} finds its path through the transformer's stray capacitance C_{tr}. It is well known in literature that such inverters are in general characterized by high impedances levels for frequencies less than 50Hz. Therefore, the variation of the common-mode voltage is in general insignificant leading therefore to a very low level of the leakage current. Accordingly, it is in general meaningless to talk about leakage current or common-mode voltage for transformer based inverters [25].

2.2. Inverters with no transformers "Transformerless"

Having eliminated the transformer and based on Figure 2, when S_1-S_4 from one side and S_2-S_3 from the other side are switched ON, the V_{AN} equals the voltage V_{PV} unless S_1 and S_4 are turned OFF. It is carried out when the pulse magnitude of the control strategy equals to V_{AN} while the voltage V_{BN} is zero. During the negative cycle, the phenomenon is much the same.

For the sake of more simplification, Figure 3 shows a redrawing of Figure 2. In Figure 3, the voltages being supplied by the inverter during each half-cycle are represented two pulse-based generators.

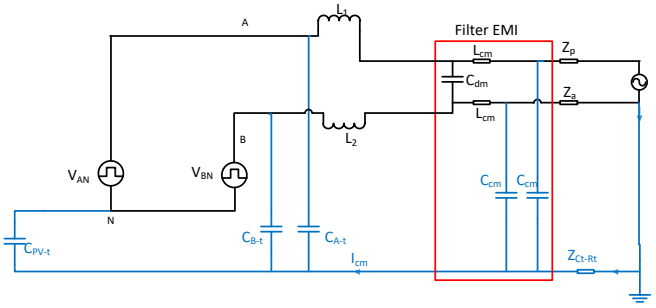

Figure 3. Electric circuit of the transformerless based inverter

In Figure 3, the filter is modified in such a way the inductor L is divided into two ones: L_1 and L_2, where their some is equal to L ($L = L_1 + L_2$). In this case, the differential-mode current denoted I_{dm} doesn't change. In fact, $I_{cm}/2$ circulates through the inductance L_1. As for L_2, the same phenomenon occurs. Therefore, the two voltages V_{AN} and V_{BN} are represented next:

$$V_{AN} = \frac{V_{dm}}{2} + V_{cm} \tag{1}$$

$$V_{BN} = -\frac{V_{dm}}{2} + V_{cm} \tag{2}$$

The analysis of Figure 3 could be redrawn as shown in Figure 4. In this case, $C_{A\text{-}t}$ and $C_{B\text{-}t}$ that are broadly small in size (Few hundred of pF). As such, the branch including C_{pv} is known to dominate the branches containing those two capacitors [26].

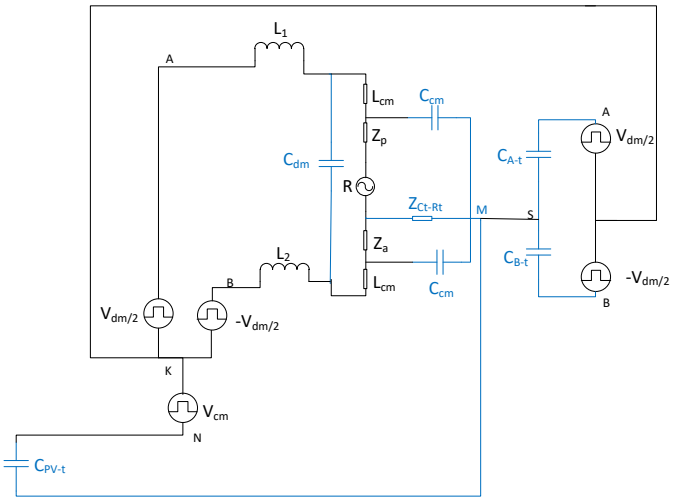

Figure 4. Equivalent circuit of the Transformerless Full-bridge inverter topology

Knowing that the grid frequency is small compared to the switching frequency of the inverter from one side and considering the small impedance of the network with respect to L, (L_1 + L_2), and L_{cm}, from the other side, one can neglect the influence of the network on the common-mode current. In light of the previous, a simple application of the electric circuit theorems, such as the superposition theorem, Thévenin's theorem and the voltage divider rule between the two points K and M could easily lead to the equivalent circuit shown in Figure 5.

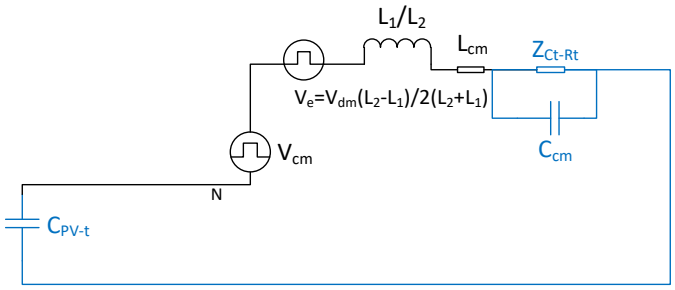

Figure 5. A very simple representation of the transformerless based full-bridge inverter topology

In light of the above analysis, it turns out that in order to investigate the leakage current through the parasitic capacitance, one can simply study the circuit of Figure 5 given above. In such figure, receives two supply voltages; those voltages are V_{CM} and V_e respectively. If the voltage between the two terminals of C_{pv} is constant, the current through it is evidently null [27]. To add to that, one can conclude that dividing the inductor L into two inductors L_1 and L_2 equates the voltage V_e to zero. Finally, it turns out that the leakage current is function on the common-mode voltage, V_{CM}, only.

3. DEVELOPED TI TOPOLOGY

As investigated within the previous sections, most TI topologies, such as the H5, the HERIC, the NPC, etc, are based on the conventional full-bridge topology with some transformations and adopting different control strategies. Most probably, an extra branch consisting of at least one transistor (H5 topology) is to be added. However, adding extra switches decreases the efficiency of the inverter due to conduction and switching losses. To add to that, each extra branch requires a control strategy which is in general complicated enough.

What would be stressed here is the major rationale for inserting a bypass branch. It is actually aimed at disconnecting the the inverter from the electric network whenever the zero voltage of the control is implemented. However, still the AC output signal is distorted when crossing the times axis even though the disconnection is quite short. Given the fact that it impacts the power quality, TI designers have generally eradicated this defect. The suggested topology compensates for such shortcoming which also includes the eradication of the current leakage.

3.1. The Proposed Topology: Analysis and investigation

Figure 6 is an illustration of the proposed topology:

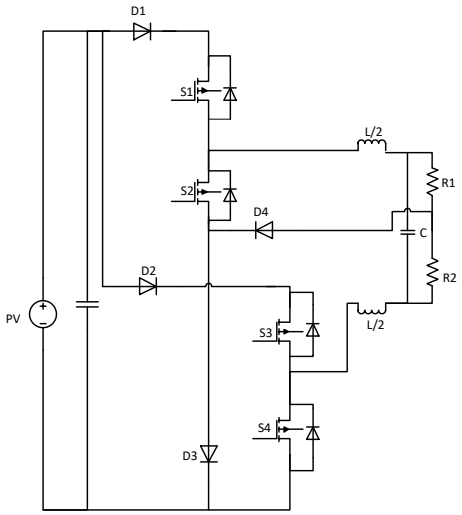

Figure 6. Proposed transformerless inverter (TI) topology

Referring to the discussions of the previous sections of this paper, it is worth mentioning that the leakage current occurs not unless the common mode voltage is inconstant. The common-mode voltage is being measured between the positive terminal of the DC bus and the midpoint of the load. It turns to be almost constant leading to a null leakage current.

Having said that, when the pair S_1-S_4 switches at high frequency, the current finds its path through D_1, S_1, S_4 and the filter, as shown in Figure 7. The freewheeling phenomenon is achieved through transistors S_1 and S_2. As illustrated in Figure 8, the current finds its way through the filtering circuitry, diodes of S_2 and D_4, respectively. As such, the power stays at the AC side and, in return, noticeably improves the inverter's efficiency, being matched to the conventional full-bridge inverter.

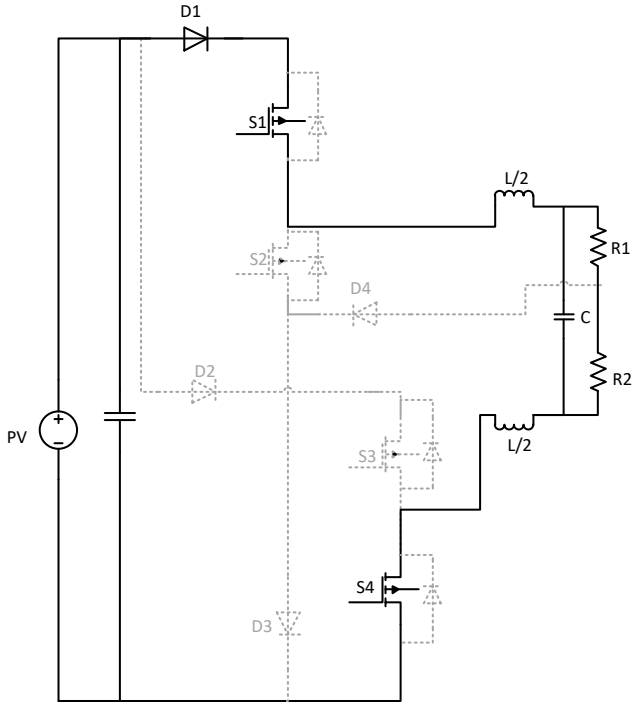

Figure 7. Path of the current (Solid) of the proposed topology during the positive half-cycle

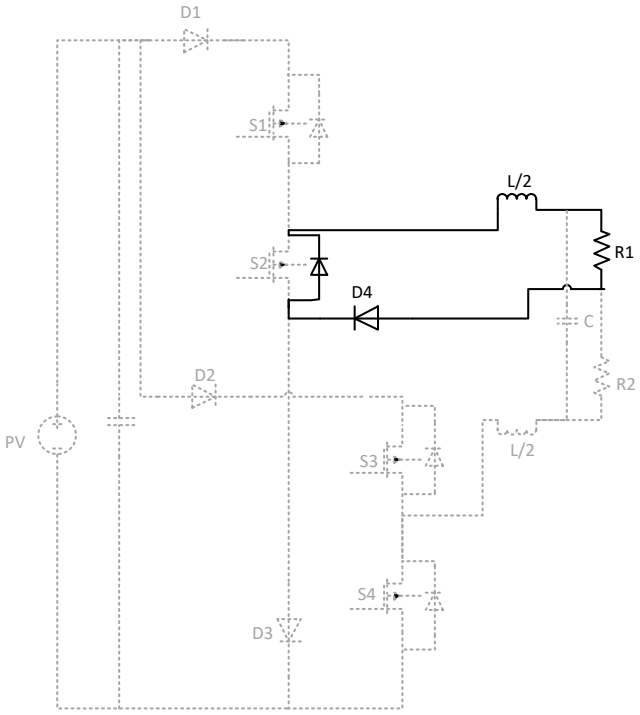

Figure 8. Path of the current during the freewheeling period

Throughout the negative half-cycle of the load period, pair S_1-S_4 is turned OFF. Meanwhile, S_2 and S_3 are switching at high frequencies. As illustrated in Figure 9, the current from the DC source to the grid flows through the filter, S_3, S_2 and the diode D_2.

Next, most famous TI topologies have been simulated and compared to the simulation results obtained for the proposed TI topology. This is aimed at highlighting the potentialities of the later.

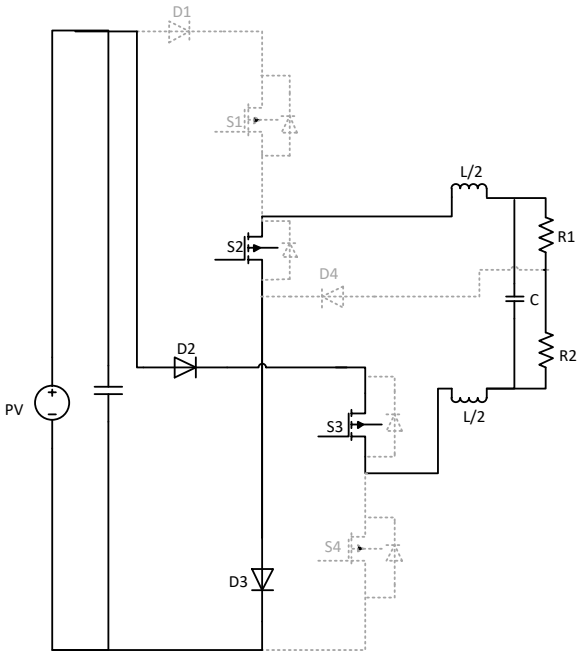

Figure 9. Path of the current during the negative half-cycle

4. RESULTS AND DISCUSSION

The H5, the full-bridge, the HERIC and the proposed topologies have been simulated and the output voltage, the load voltage and the leakage current have been compared, respectively.

Figure 10 shows the output waveforms of the full-bridge TI under a unipolar PWM control strategy. Such topology exhibits certainly a high level of the leakage current being higher than all the IEEE standards. Moreover, this topology has not removed the zero-crossing distortion.

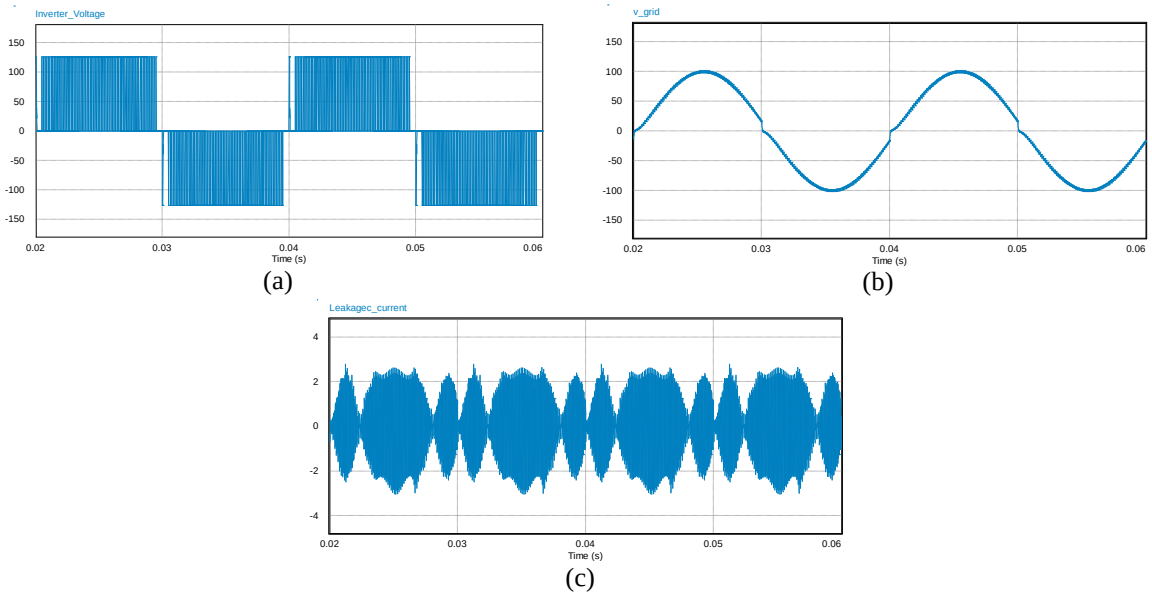

Figure 10. (a) the Full-Bridge inverter output voltage; (b) the load voltage; (c) the leakage current

The HERIC topology, characterized by a low leakage current level, being less than 5mA, is the second topology being inspired from the full-bridge TI topology. Just like full-bridge topology, the HERIC the topology did not solve the problem of the zero-crossing distortion. A best illustration of that is shown in Figure 11.

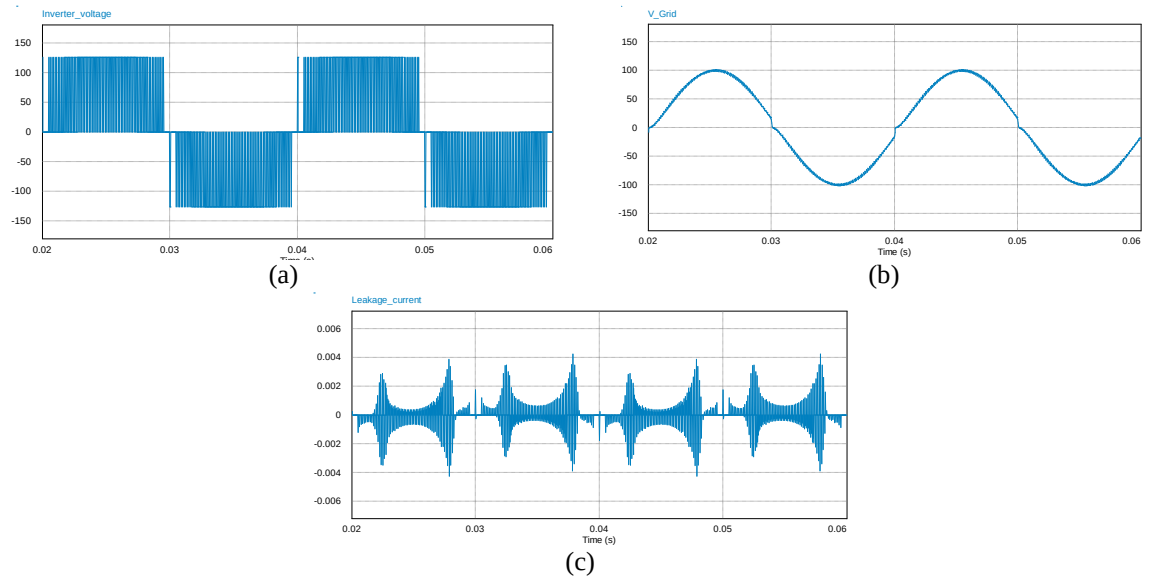

Figure 11. Selected features of the HERIC inverter: (a) Inverter output voltage; (b) the load voltage; (c) the leakage current

Likewise, the H5 TI topology is penalized by a quite high leakage current level that could reach 0.5A, as shown in Figure 12. To add to that, the H5 topology presents a load voltage distorted at the zero-crossing point.

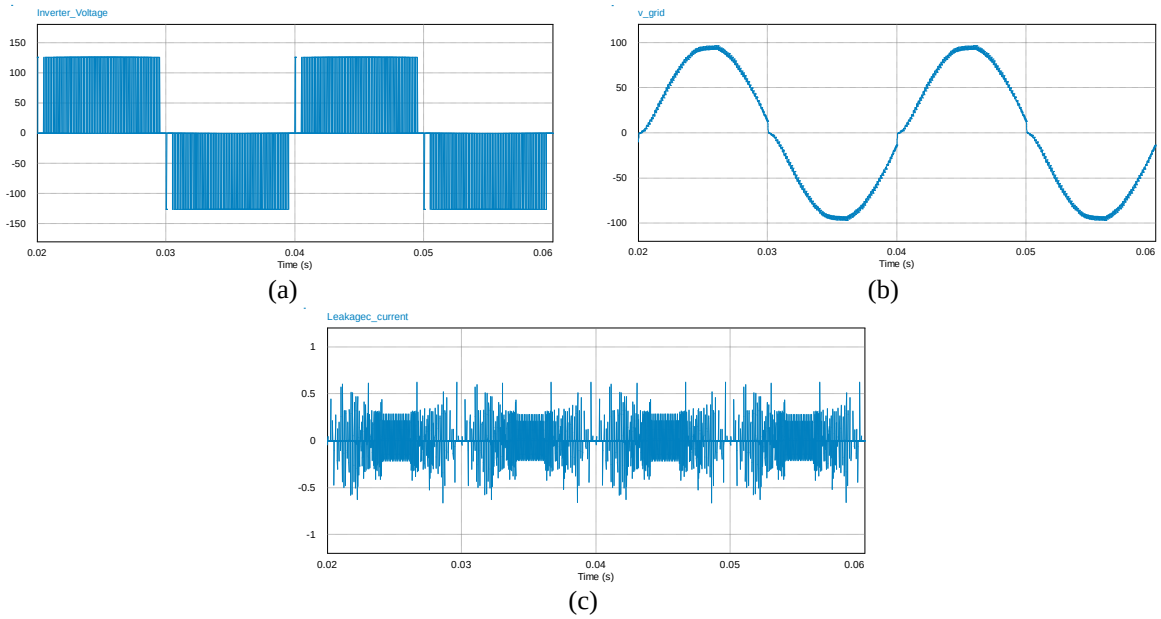

Figure 12. Selected features of the H5 inverter: (a) Inverter output voltage; (b) the load voltage; (c) the leakage current

Unlike the previously investigated topologies, the proposed topology has solved all drawbacks related to TI topologies such as a null leakage current, a high efficiency and a null-zero crossing distortion. Figure 13 shows the output waveforms of the proposed TI topology.

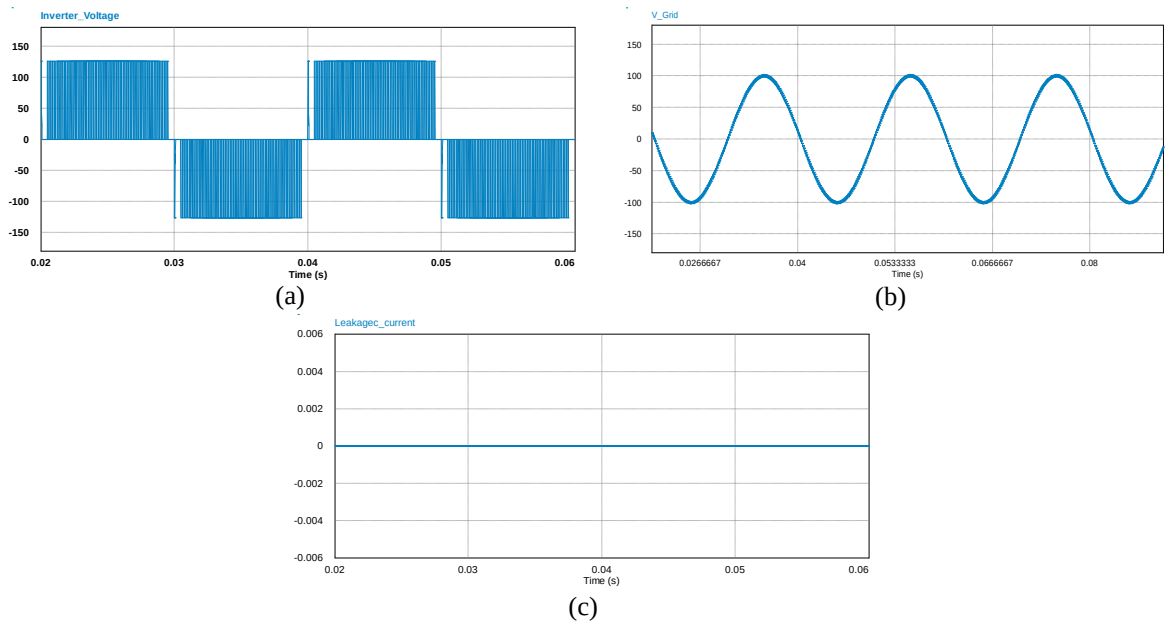

Figure 13. Selected features of the proposed inverter: (a) Inverter output voltage; (b) the load voltage; (c) the leakage current

One should stress the fact that the achievement of an astounding performance of the proposed topology does not request complicated circuits to create a control strategy of the intended PMW. It does not even need any extra switching devices. To make it possible to attain a constant common mode voltage, one must guide the current upon the corresponding period as well as clamp the midpoint of the load to transistor S_2. As such, the current leakage turns to be null. This actually provides the benefit of energy efficiency.

Given that it is equipped with a module of PWM power, a low cost microcontroller 18F2331 is used to implement the control strategy. Across its PORT "B", such microcontroller can actually create up to four independent PWM signals. These are output pins RB0, through RB3, respectively. An IGBT driver having independent high and low side referenced output channels (IR2110S), a MOSFET of high-speed power and a high voltage are deployed to enhance the signals of the PWM, which are generated from the microcontroller itself. This is aimed at controlling the four transistors IRF840 of the suggested topology.

A pure sine wave voltage through the load without any zero-crossing distortion (channel 1) all along with the leakage current which was equated to zero (channel 2) is illustrated in Figure 14. The load and inverter voltages are depicted in Figure 15; whereas, the FFT of the load voltage (Channel M) is displayed in Figure 16. Signifying the single frequency component of the output signal, the one single spike at the 50 Hz level is indeed depicted in The FFT analysis.

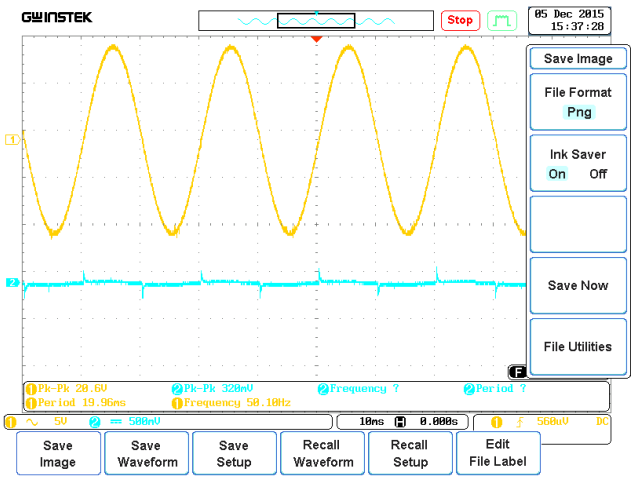

Figure 14. From top to bottom: Load voltage and leakage current

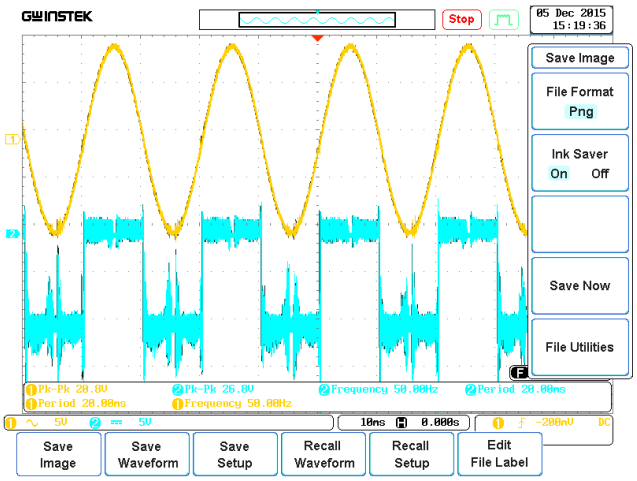

Figure 15. From top to bottom: Load and inverter voltages

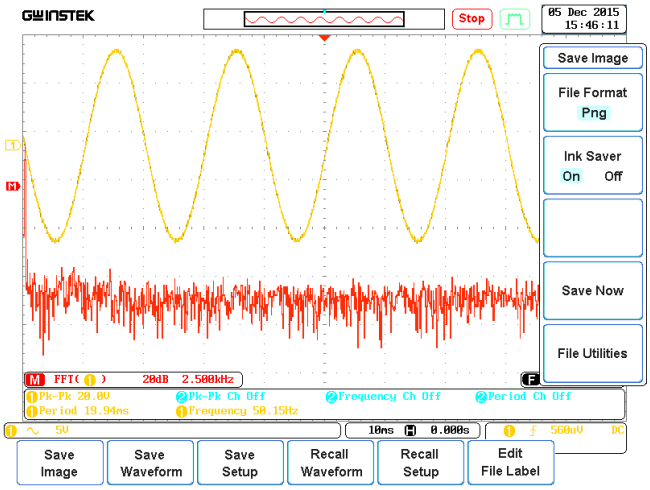

Figure 16. From top to bottom: Load voltages and FFT analysis of the proposed topology

5. CONCLUSION

It is acknowledged that Transformless Inverters (TI) in the PV chain's end are energy-efficient, compact and cost-effective. However, some defects are found when integrating TIs in PV systems. In fact, a leakage current between the inverter and the ground could take place through the parasitic capacitances. Moreover, a DC component could be injected to the grid due to the galvanic connection. This DC component shall saturate and damge domestic appliances equipped with tranformers.

This study examined a novel highly efficient TI topology with a nearly null zero-crossing distortion and an almost null zero-current leakage. Such topology has undergone a simulation-based comparison with a focus on some of its characteristics, including the HERIC, the H-bridge, and the H5 TIs. This process has been subject to the analysis of the operating sequences and the topological description of the suggested TI. The later has displayed the lowest current leakage, as being demonstrated by the experiment.

Having said that, the suggested topology could not ultimately be perceived as a mature technology for PV systems before an extended investigation is conducted. Such comparative study shall be aimed at investigating the harmonic content of the output voltage, which is already under different loading levels in an attempt to quantify the effect of the zero-crossing distortion. In fact, an experimental validation of the simulation results has been conducted and what has been found is a good match.

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