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# Grid Interconnection of PV System Using Symmetric and Asymmetric MLI Topology

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**ABSTRACT**

Generally, PV cell converts sunlight into electricity in the form of dc. Integration of PV system with the existing grid requires dc-ac conversion. This conversion is possible with the help of a dc-ac converter known as an inverter. Among all types of the inverter, multilevel inverters (MLIs) are playing a major role with all their major privileges like High power quality, low distortion, less blocking voltages for switching devices. Conventional multilevel inverter topologies such as diode clamped, flying capacitor and cascaded MLIs are having so many disadvantages. One of the common disadvantage among all the conventional MLIs is the requirement of more number of power electronic components as the level of the output voltage increase. To reduce the power electronic components this paper proposes a multilevel inverter topology in symmetrical and asymmetrical configuration. The proposed MLI uses 12 switches and 19 diodes which are very less compared to conventional MLI topologies for generates nine and thirteen level output voltages. Comparison between presented MLI topology and conventional MLI topologies is presented in this paper. Finally, the proposed MLI whose input is fed from the PV system is integrated into the grid. The proposed concept is validated by using the MATLAB/SIMULINK software and the appropriate results are presented in this paper.



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## 1. INTRODUCTION

In the present scenario, the use of electric power is increasing due to the advancement of technology. Unfortunately, conventional energy sources (like fossil fuels) are depleting day by day. To meet the required demand, people are looking for renewable energy sources (RES) such as photovoltaic (PV), wind and fuel cell, etc. Among all the RESs, PV gains more attention due to the advantages of clean and no pollution, etc [1]. Normally the voltage obtained from the PV system is of dc. To interface a PV system with the grid, a suitable inverter is needed. Conventional full bridge inverter generates an alternating output voltage with higher harmonic content and also it imposes high dv/dt stree on the switches. Over the last few decades, the use of multilevel inverters is increases tremendously [2]-[3]. Multilevel inverters are divided into three types [4]-[9] based on their configurations which are given below;
Diode clamped MLI
Flying capacitor MLI
Cascaded H-bridge MLI

Diode clamped MLI topology uses more number of clamping diodes [10] and switches as the level of the output increases. Flying capacitor MLI has the disadvantage of capacitor voltage balancing problem [11]-[13]. Cascaded H-bridge MLI topology has the advantages of high modularity but it requires separate dc sources. To overcome the above disadvantages this paper proposes a MLI topology with reduced number of components for induction motor in agricultural field which is shown in below. The proposed MLI topology is implemented in both symmetrical and asymmetrical configurations. Finally, the proposed MLI topology is used to interface PV system with grid. By using the proposed MLI, the PV generated dc voltage is changed into ac voltage and it is tied up with the existing grid with fullfilments of grid propoerties.

## 2. PROPOSED TOPOLOGY

### 2.1. Symmetrical Configuration

In symmetrical configuration, magnitude of each dc voltage sources is equal. Cascaded connection of proposed MLI increases the output voltage levels. The total output voltage is the summation of individual proposed MLIs output voltage. Proposed multilevel inverter consists of four dc voltage sources which is shown in the Figure 1. Our proposed topology can generate 9 levels in output voltage. By proper turning on and off switches required output voltage can be obtained. Therefore, in proposed topology required number of cascade blocks based on number of levels can be finding out by using

$$\mathbf{M=4n+1} \quad (1)$$

where
M= number of output voltage levels
n= number of cascade blocks

From the above expression, for generating 9 levels in output voltage two symmetric cascaded blocks are needed which are shown in Figure 1.

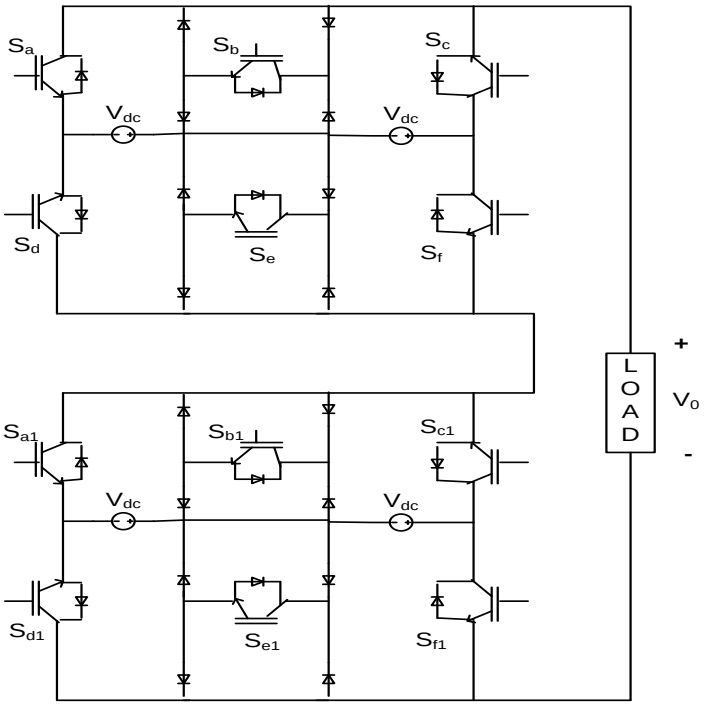


Figure 1. Proposed MLI topology in Symmetrical configuration

The output voltage waveform consists of nine levels ±4Vdc, ±3Vdc, ± 2Vdc, ± Vdc and 0. The switching pattern for the proposed inverter in symmetrical configuration is shown in below Table 1.

Table 1. Switching states and Output voltages for Symmetrical Configuration

| $S_a$ | $S_b$ | $S_c$ | $S_d$ | $S_e$ | $S_f$ | $S_a^1$ | $S_b^1$ | $S_c^1$ | $S_d^1$ | $S_e^1$ | $S_f^1$ | Voltage Level |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | $+4V_{DC}$ |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | $+3V_{DC}$ |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | $+2V_{DC}$ |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | $+V_{DC}$ |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | $-4V_{DC}$ |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | $-3V_{DC}$ |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | $-2V_{DC}$ |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | $-V_{DC}$ |

### 2.2. Asymmetrical Configuration

In this configuration, dc voltage sources are differing in their magnitudes. Therefore, the difference in the dc voltage sources enhances the output voltage levels. Due to increase of the voltage the output voltage levels are increase from 9 to 13. In these mode six positive voltages, six negative voltages and zero can be produced. The different output voltage levels are ± 6Vdc, ± 5Vdc, ± 4Vdc, ± 3Vdc, ± 2Vdc, ± Vdc and 0 and the corresponding switching states are shown in Table 2.

Table 2. Switching pattern and Output voltages for Asymmetrical Configuration

| $S_a$ | $S_b$ | $S_c$ | $S_d$ | $S_e$ | $S_f$ | $S_{a-1}$ | $S_b^1$ | $S_c^1$ | $S_d^1$ | $S_e^1$ | $S_f^1$ | Voltage Level |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | +6Vdc |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | +5Vdc |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | +4Vdc |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | +3Vdc |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | +2Vdc |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | +Vdc |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | -Vdc |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | -2Vdc |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | -3Vdc |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | -4Vdc |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | -5Vdc |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | -6Vdc |

## 3. COMPARISON OF PROPOSED MLI TOPOLOGY WITH CONVENTIONAL MLI TOPOLOGIES

The following Table 3 and Table 4 illustrate the comparison between existing topologies and proposed topology in symmetrical and asymmetrical configuration.

Table 3. Comparison of other topologies with proposed topology for symmetrical configuration

| Type of MLI | No of Main Switches | No of Diodes | No of DC Bus Capacitors |
|---|---|---|---|
| Diode Clamed MLI | 16 | 16 | 8 |
| Flying Capacitor MLI | 16 | 16 | 8 |
| Cascaded H-bridge MLI | 16 | 16 | 4 |
| Proposed MLI | 12 | 16 | 0 |

Table 4. Comparison of other topologies with proposed topology for asymmetrical configuration

| Type of MLI | No of Main Switches | No of Diodes | No of DC Bus Capacitors |
|---|---|---|---|
| Diode Clamed MLI | 24 | 24 | 12 |
| Flying Capacitor MLI | 24 | 24 | 12 |
| Cascaded H-bridge MLI | 24 | 24 | 12 |
| Proposed MLI | 12 | 16 | 0 |

From Table 3 and 4, the Proposed Inverter uses less number of power electronic components compared to conventional MLI topologies and hence switching losses as well as cost for implementing it is reduced.

## 4. SIMULINK MODELLING AND RESULTS

The Figure 3 depicts the MATLAB/ SIMULINK diagram of the proposed 5 level MLI topology. It uses six switches and eight diodes to get five level output waveform. The output voltage obtained from the symmetrical configuration contains five level (Figure 4). Compared to cascade H-bridge MLI it uses less switches and hence the switching losses are reduced. From the Figure 5 and 6, as the level of the inverter increases THD content reduces.

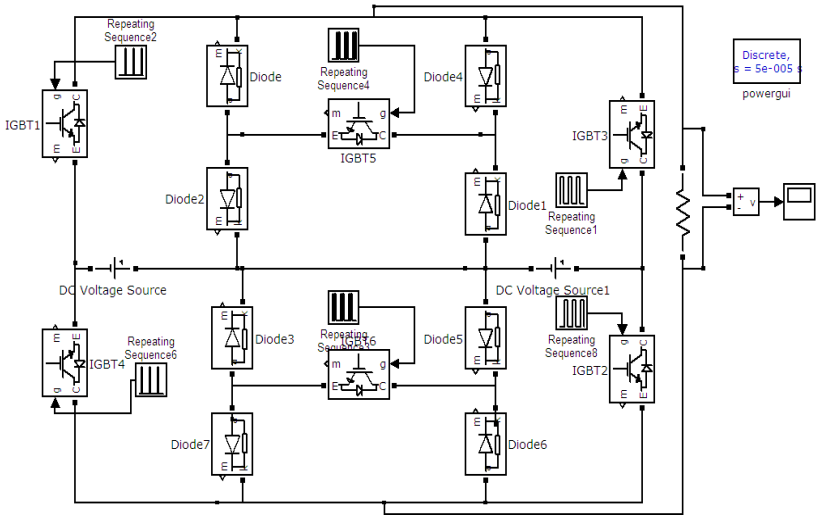


Figure 3. MATLAB/ SIMULINK diagram of the proposed 5 level MLI topology

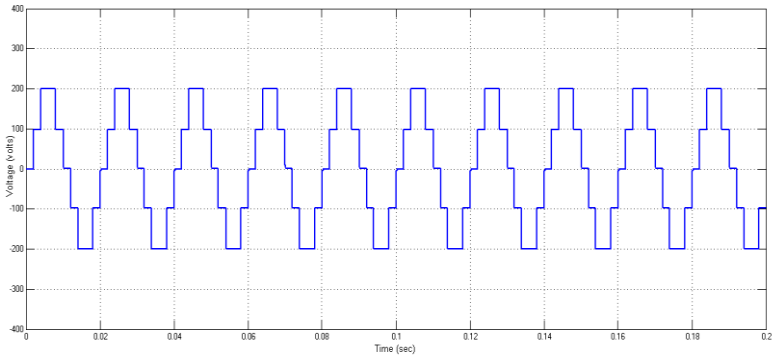


Figure 4. Output voltage of proposed 5 level MLI topology

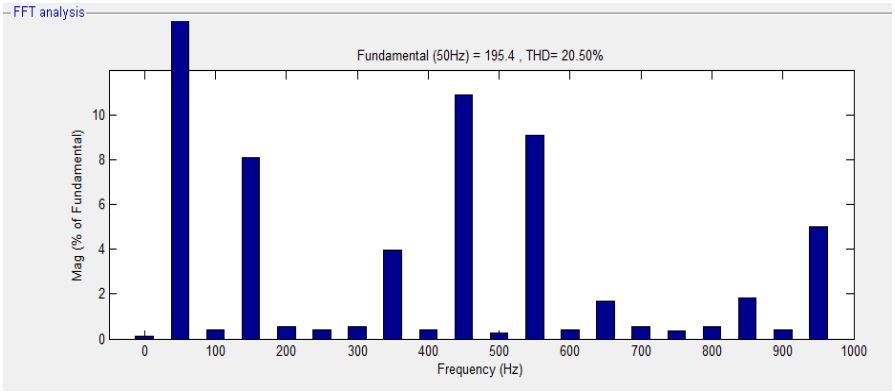


Figure 5. THD of the 5-level proposed MLI topology

The Figure 6 depicts the FFT analysis of the proposed 7-level proposed MLI topology. The Figure 7 depicts the MATLAB/ SIMULINK diagram of the proposed 9 level MLI topology in symmetrical configuration. Output waveform and FFT analysis of the proposed 9-level proposed MLI is shown in Figure 8.

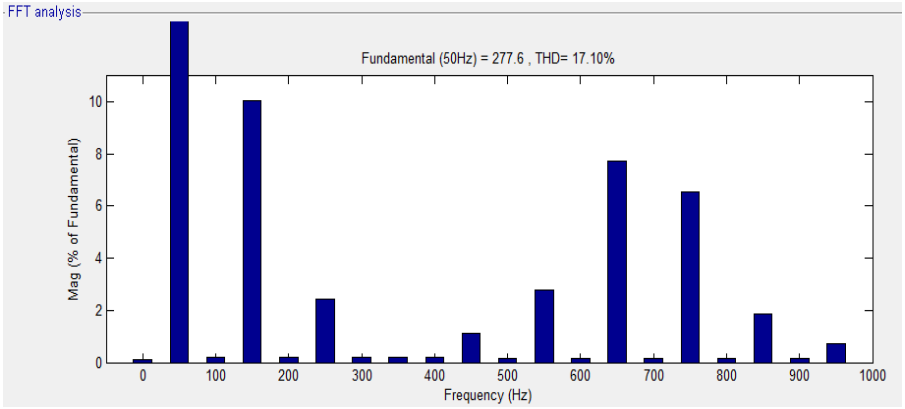


Figure 6. THD of the 7-level proposed MLI topology

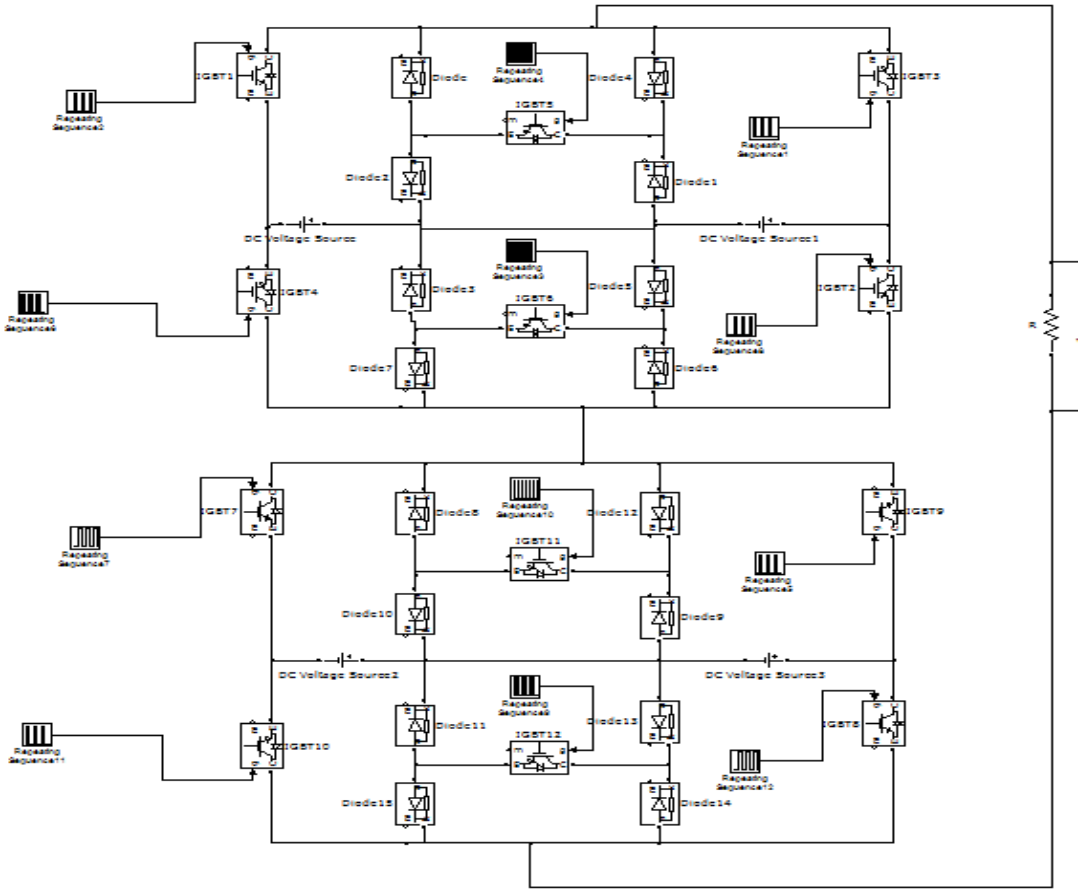

Figure 7. MATLAB/ SIMULINK diagram of the proposed 9 level MLI topology

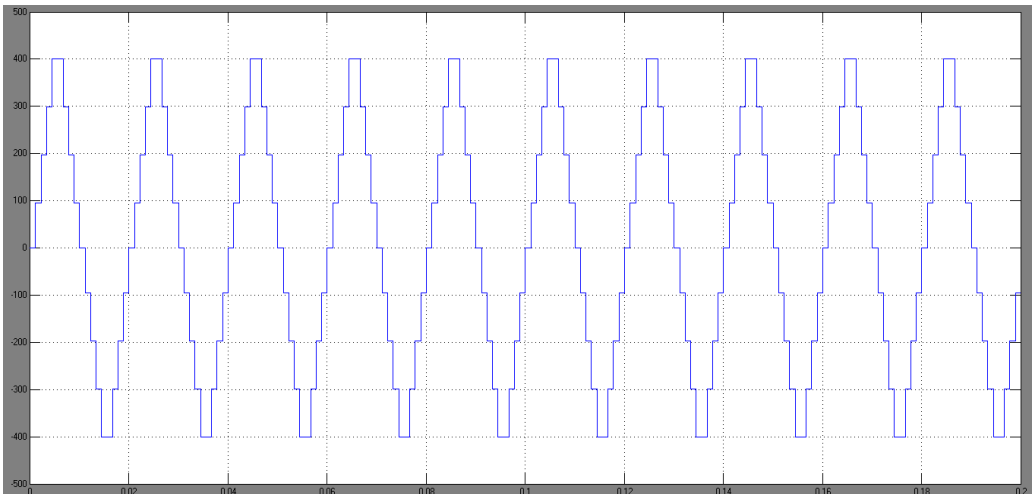

Figure 8. Output voltage of proposed 9 level MLI topology

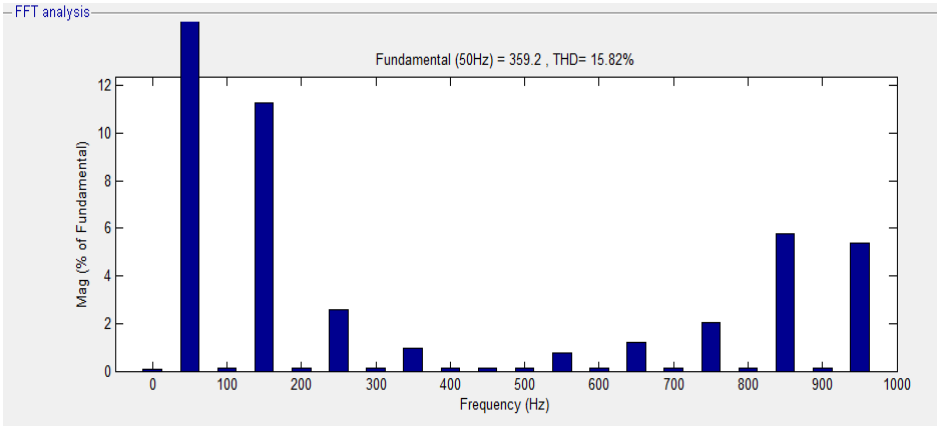


Figure 9. THD of the 9-level proposed MLI topology

The Figure 10 and 11 shows the output wave voltage waveform and FFT analysis of the proposed 13-level MLI topology.

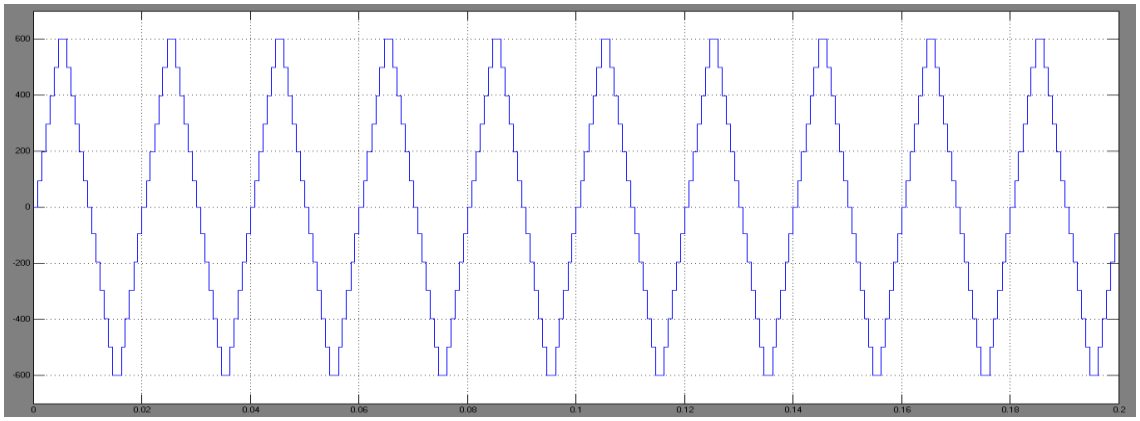

Figure 10. Output voltage of proposed 13 level MLI topology

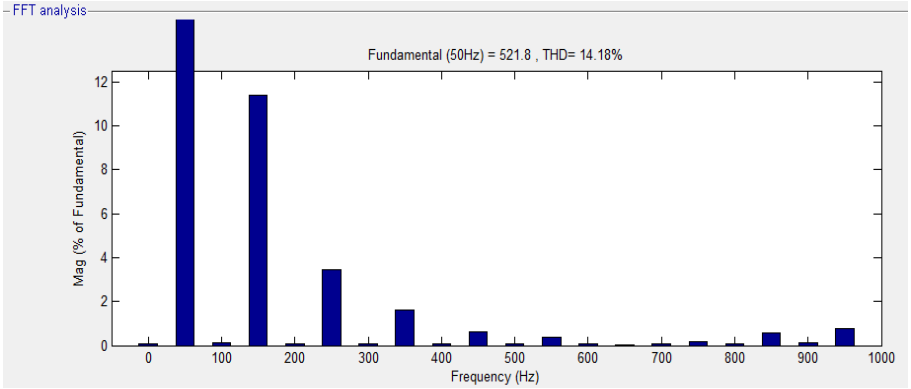


Figure 11. THD of the 13-level proposed MLI topology

From Figure 12, the phase angle between the grid Voltage and grid Connected Current is zero, i.e. the system works under unity power factor and also it satisfies the grid conditions such as frequency, amplitude of the grid voltage and the phase angle.

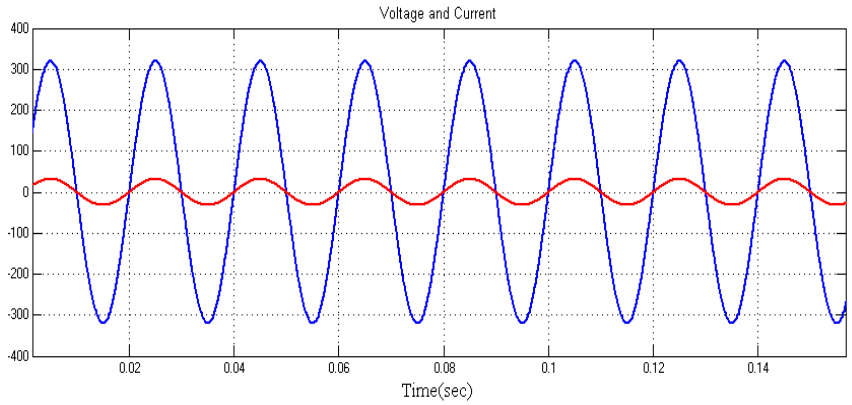


Figure 12. Grid voltage and grid connected current

The Table 4 depicts the THD analysis of the proposed MLI topology. From Table 4, as the level increases THD value decreases.

Table 4. Comparison of other topologies with proposed topology for symmetrical configuration

| Number of Levels | THD Content |
|---|---|
| 5-level | 20.50 % |
| 7-level | 17.10 % |
| 9-level | 15.82 % |
| 13-level | 14.18 % |

## 5. CONCLUSIONS

This paper proposes a new multilevel inverter topology with reduced number of switches. The main disadvantages of diode clamped MLI, flying capacitor MLI and cascaded H-bridge MLI topology are eliminated in this proposed one. The most attractive renewable energy source (i.e. Photovoltaic) is interfaced to the conventional grid through proposed MLI topology which satisfies the grid requirements like phase angle, frequency and amplitude of the Grid voltage. Finally, the proposed concept is verified with the help of MATLAB/SIMULINLK environment and the corresponding results are also presented. Results shows that as the level of the inverter increases THD value decreases. Form the results, the grid connected current and grid voltage are in phase with each other.

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