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Improved dead-time elimination method for three-phase power inverters

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ABSTRACT

In real inverters' operations, it is essential to insert delay time in the pulses provided to the inverter switches to protect the DC link against the short circuits. From this situation, the dead time phenomenon is introduced that causes undesirable performance and distortion of the output signal. Previously, researchers have proposed various schemes for compensating or eliminating dead-time. In this paper, a new dead-time elimination (DTE) scheme is proposed with a guarantee algorithm to eliminate dead-time and overcome the issues produced at the zero-currents-crossing point (ZCC). This method does not require additional hardware or filters to determine the polarity of the output current, and its principle is very simple to implement. The developed DTE method completely removes the dead-time issues on the magnitude and phase of the output voltage, and avoid the problems which can be induced around the ZCC. The results confirm the effectiveness and safety of this method.

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1. INTRODUCTION

The switching devices of the inverters such as IGBT and MOSFET are not ideal switches, they have finite turn-ON/turn-OFF times which may provide shoot-through on the DC link [1]. To overcome this issue, the deadtime is introduced, which assures that the switches of one leg are not closed at the same time. Dead-time is realized by delaying the rising edge of the pulses provided to the switches [2]. Dead-time creates a nonlinear converter characteristic that causes a distortion of the output voltage [3], i.e., it generates a low-order harmonics in the output voltage of the inverter, which leads to additional losses which increase significantly with increasing switching frequency [4].

Various methods have been proposed to eliminate the dead time or to compensate for its effects. These methods can be categorized as follows: a) methods based on average voltage compensation, b) pulse-based compensation methods, c) methods based on harmonic compensation, d) Dead time elimination (DTE) methods.

In the compensation based on average voltage, the error voltage between the actual output voltage and ideal output voltage, due to the Dead-Time, is averaged and added or subtracted from the reference voltage according to the current polarity [5-8]. These methods compensate the magnitude error of output voltage but the correction of phase error is not considered [9].

Pulse-based methods compensate the voltage error introduced by dead time for each pulse [10, 11]. In these methods, the voltage error is detected and then corrected in the next pulse. This delay in the voltage correction is considered as the main drawback of these methods [12].

In the methods based on compensating the harmonics induced from the dead-time insertion, additional control loops are employed in the inverter control system to filter these harmonics [13-15]. The dead-time produce even harmonics and mainly the sixth order harmonics in the synchronous reference frame. The sixth order harmonic is suppressed using an integral controller in [16] and a compensator based neural networks in [17]. The repetitive control has been used and embedded with the proportional resonant control system in [18] and [14], and used with PI controller in [15] to mitigate the dead-time harmonics.

All the dead-time compensation methods are used to compensate the defects produced from the dead-time insertion. They don't give ideal solutions because the dead time effects vary with many factors like the circuit design, device characteristics, load condition [19]. Moreover, there is no one compensation method can compensate all the dead time effects together, such as the error in magnitude and phase, and the delaying effect and harmonics.

The work in [20, 21] proposes a DTE technique to avoid the short circuit on the DC link of the inverter without inserting dead-time. This technique is executed by disabling the PWM signal provided to one switch of the inverter leg according to antiparallel diode conduction of the other switch in the same leg. To detect the conduction of diodes, a hardware detection circuit is introduced, resulting in additional cost, low reliability, and noise immunity. This method has a high dependence on the current polarity detection because the wrong detection leads to serious distortion. Moreover, this method is not reliable around the zero-crossing point of inverter current which may contain high ripple, this will be detailed in the next sections.

In [19], the DTE is performed by disabling the inverter switches according to the polarity of the duty cycle provided by the current regulator without requiring additional detection hardware circuits. Around the zero-crossing point of the inverter current, a transition from the DTE scheme to the conventional PWM with dead-time compensation is applied. The proportional resonant control is used to compensate the dead-time harmonics in this situation. This is a mixed-method that doesn't give full elimination of dead time because in 50% of the switching period the conventional PWM is applied. Moreover, this method highly depends on the type of control technique.

The work in [22] uses the inverter current feedback, instead of duty cycle estimation [19] or hardware detection circuit [20], through a double second-order generalized integrator locked loop (DSOGI-FLL) to mitigate noise and minimize the current distortion around the zero-crossing moment. This gives error between the filtered feedback signal and the actual value of current. Moreover, this method required a delay compensation for the filtered signal.

To avoid all the DTE issues, this paper offers a simple DTE scheme with actual inverter current feedback through a regular current sensor without any precise additional hardware detection circuit or filters. A new guarantee scheme is proposed to prevent the overlap between the leg switches which can be produced around the zero-crossing of the inverter current. The developed DTE method is safe, effective and does not depend on the method of control or modulation. This method is employed for a three-phase voltage source inverter (VSI) controlled by PID-controller with PWM.

2. DEAD-TIME EFFECT

The topology of three-phase autonomous VSI with LC-filter is shown in Figure 1 [23]. The typical control scheme with dead-time insertion for one leg inverter is depicted in Figure 2. Dead-time is executed by applying a delay time in the rising edge for every PWM pulses. The delay time is about 2-5 µs according to the switch characteristics. Figure 2 shows also the current flow direction through the anti-parallel diodes during the dead-time, where the current polarity is defined as positive if the current flows from the inverter to the loads, and vice versa. The voltage drops of switching devices and freewheeling diodes, parasitic capacitances are beyond the scope of this paper and not considered.

The switching signals (S_a, S'_a) before and after the dead-time insertion (T_d), and the effect of the dead time on the inverter output voltages are demonstrated in Figure 3. The turn-on (T_{on}) and turn-off (T_{off}) delay times of the inverter switches are not shown but are considered in this analysis.

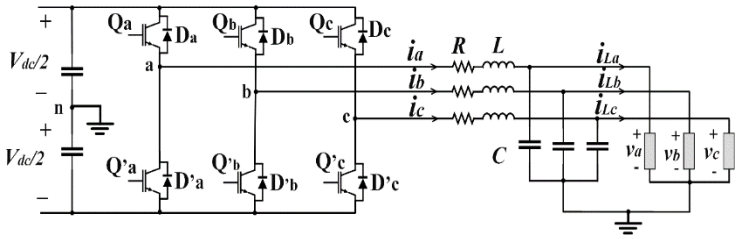

Figure 1. Three-phase autonomous VSI with LC-filter

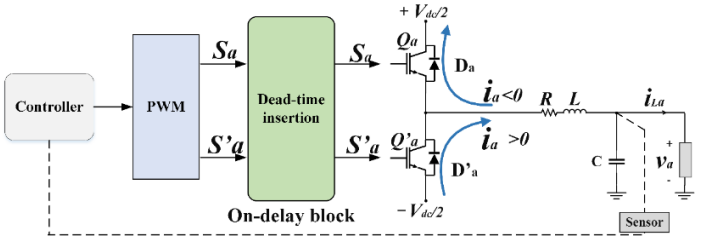

Figure 2. Typical control scheme with the introduction of the dead time insertion for one inverter leg

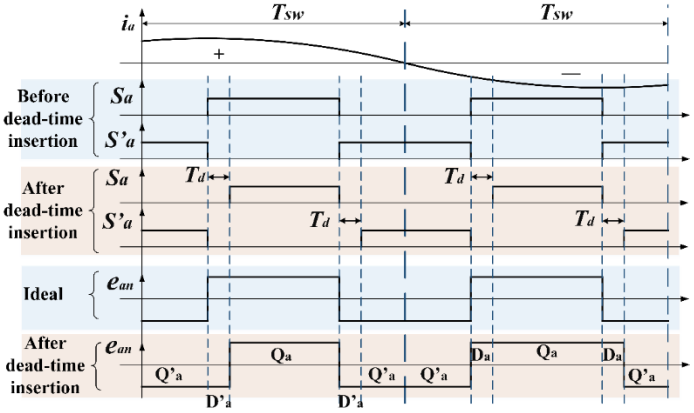

Figure 3. Switching signals and the corresponding output voltage of one leg of the inverter, before and after inserting a dead time, with respect to the output current of the polarity inverter.

It can be observed that the inverter output voltage (e_{an}) depends on the polarity of the output current (i_a). Comparing with the ideal case, when the output current is positive, the inverter output voltage is reduced (voltage loss), and when i_a is negative, the inverter output voltage is increased (voltage gain). Figure 3 indicates the conductions of the transistors (Qa and Q'a) and their anti-parallel diodes (Da and D'a). It can be observed that during the daed-time the diodes are conducting and allow the output current to flow. At the negative polarity of the output current i_a, the diode D'a is conducted and provides a positive output voltage e_{an}. At the positive polarity of the output current i_a, the diode Da is conducted and provides a negative output voltage e_{an}. In one switching period T_{sw}, the average voltage error can be expressed as [14]:

$$\Delta e = \begin{cases} \dfrac{-T_d - T_{on} + T_{off}}{T_{sw}} \times V_{dc}, & i_a > 0 \\ \dfrac{T_d + T_{on} - T_{off}}{T_{sw}} \times V_{dc}, & i_a < 0 \end{cases} \quad (1)$$

and assuming $T_{on} = T_{off}$ yields,

$$|\Delta e| = \frac{T_d}{T_{sw}} \times V_{dc} \quad (2)$$

Where T_{sw} is the switching period and V_{dc} is the instantaneous DC voltage. From (2), to decrease the voltage error provided by the dead-time, either decrease the dead-time T_d or increase the switching period T_{sw} (i.e. decrease the switching frequency). The inverter with lower switching frequency requires a larger LC-filter for filtering the switching frequency harmonics. On the other hand, with a shorter dead time period, the converter legs have risks of short-circuiting.

3. THE PROPOSED DTE METHOD

From Figure 3, after dead-time insertion, it can be clearly observed that when the current is positive, the output voltage follows the shape of the switching signal S_a. When the current is negative, the output voltage follows the inversion of the switching signal S'_a. This is due to the fact that during the dead-time the two switches are open, the output current i_a in negative polarity flow through Da, giving output voltage $V_{dc}/2$, and when i_a is in the positive direction, the diode D'a is connected and provides output voltage $-V_{dc}/2$. It can be concluded that when the current is positive or negative, the output voltage follows only one of the switching signals, and since this signal includes a dead time, this affects the output voltage. From this phenomenon, the principle of the methods of elimination of dead time is introduced.

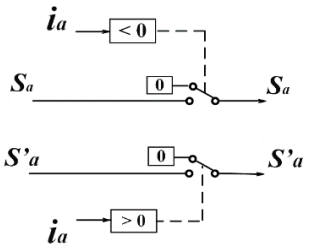

Figure 4. The scheme of the proposed DTE

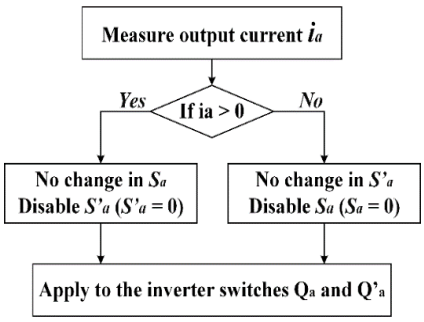

Figure 5. The proposed DTE algorithm

The proposed DTE scheme for one phase (i.e. phase a) is shown in Figure 4. During the positive polarity of output current ia, the switching signal S'a is disabled (i.e. the switch Q'a is permanently opened), whereas no changing is applied to the other switching signal. And vice versa during the negative polarity of the output current. This algorithm is executed every sampling period Ts. The proposed DTE algorithm is shown in Figure 5. In this case, the time interval between the two switches is very long and is about 25% of the switching period, without any distortion in the output voltage. Therefore, there is no need to insert dead-time, as shown in Figure 6.

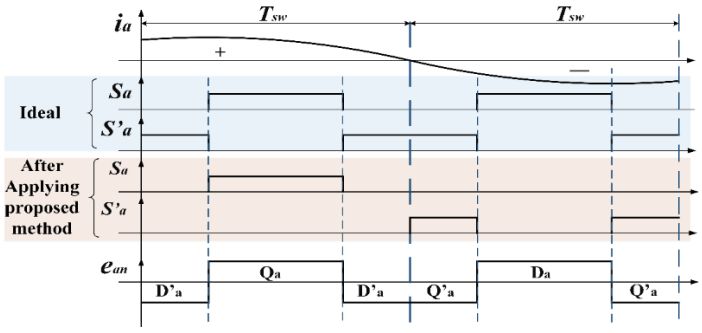

Figure 6. Switching signals and the corresponding output voltage of leg a with the proposed DTE method

4. THE POTENTIAL LIMITATIONS OF THE DTE AND ITS PROPOSED SOLUTIONS

As the output inverter current is not pure sinusoidal and contains ripples in high frequencies and amplitudes, there are many oscillations in the current polarity around the zero-crossing point as shown in Figure 7. This may lead to loss of switching signals in some intervals and stop the disabling algorithm in other intervals. Thanks to the freewheeling diodes, the output voltage is not distorted as revealed in Figure 7. However, in this situation, the time interval between the two switches may be very small and lower than the dead-time tolerance and resulting in a short circuit in the inverter leg. This paper offers a guarantee algorithm to avoid this problem. This algorithm proposes two feedforward decoupling loops with off-delay blocks between the two switching signals, as shown in Figure 8.The open loop transfer function of the APS model with the current control loop can be written as:

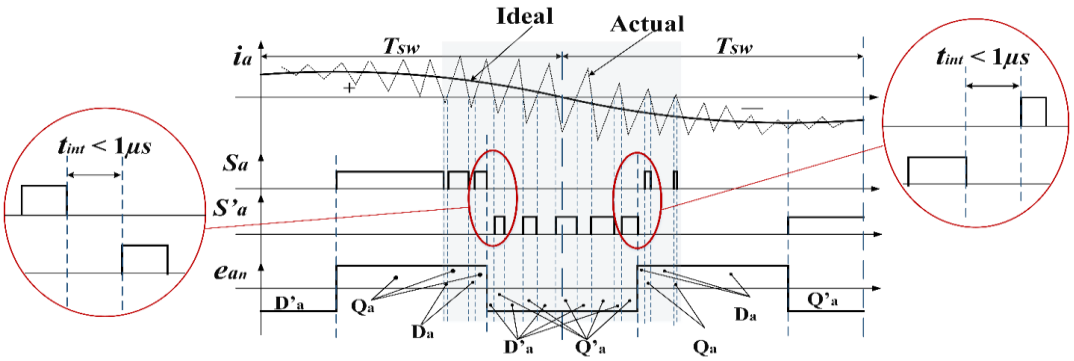

Figure 7. The issues around the zero-current-crossing point

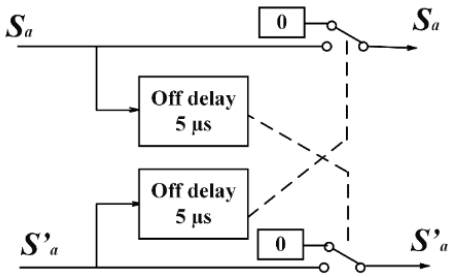

Figure 8. The proposed guarantee algorithm

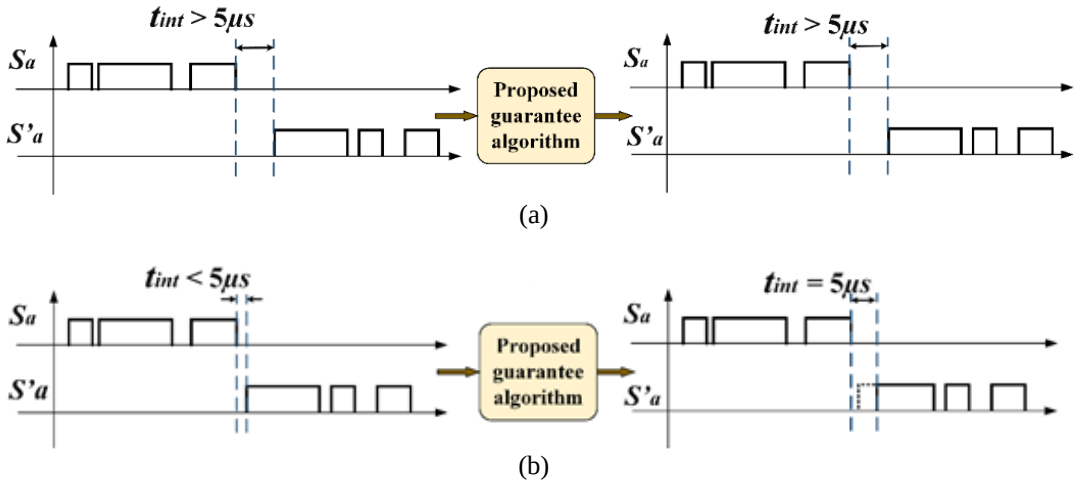

Figure 9. The effect of the guarantee algorithm when (a) t_{int}> 5 µs and (b) t_{int} <5 µs

As the output inverter current is not pure sinusoidal and contains ripples in high frequencies and amplitudes, there are many oscillations in the current polarity around the zero-crossing point as shown in Figure 7. This may lead to loss of switching signals in some intervals and stop the disabling algorithm in other intervals. Thanks to the freewheeling diodes, the output voltage is not distorted as revealed in Figure 7. However, in this situation, the time interval between the two switches may be very small and lower than the dead-time tolerance and resulting in a short circuit in the inverter leg. This paper offers a guarantee algorithm to avoid this problem. This algorithm proposes two feedforward decoupling loops with off-delay blocks between the two switching signals, as shown in Figure 8.

The proposed guarantee algorithm disables the switching signal provided to one switch when the other switch of the same leg is turned on and this disablement is continued for 5 µs after the falling end of the other switching signal. The effect of this guarantee algorithm appears only when the time interval (t_{int}) between two switching signals is less than 5 µs, as shown in Figure 9. Figure 10 shows the typical block diagram of the proposed scheme of the DTE for one leg of the inverter. The proposed guarantee algorithm is placed between the switch gates and the proposed DTE block. The PWM is utilized to provide the switching signals for the proposed DTE block. The PID control technique is used to regulate the load voltage [24, 25]. As shown in Figure 10, the proposed DTE has no influence on the control system and PWM [26].

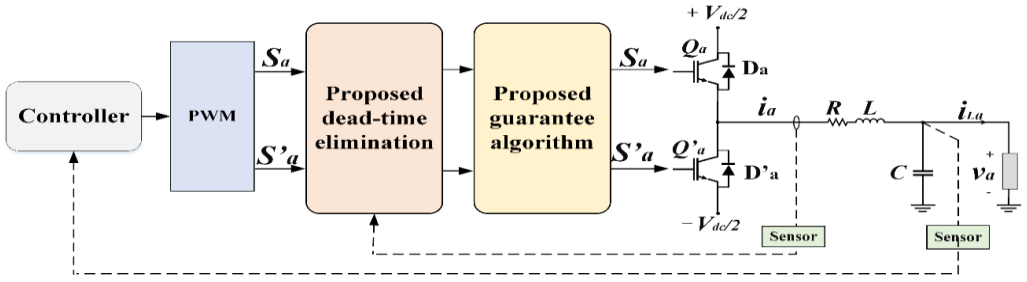

Figure 10. Topological control scheme with the proposed DTE method for one inverter leg

5. SIMULATION RESULTS

The proposed DTE is tested on a three-phase VSI with LC filter connected to (a) resistive loads (b) and inductive loads. Mathematical and simulation modeling was carried out in MATLAB / SIMULINK environments. The parameters used in the simulation is shown in Table 1.

Table 1. System parameters

Parameters	Values
DC input voltage of the inverter	V_{dc} = 640 V
Sampling time	T_s = 20 µs
Switching frequency	f_s = 5000Hz
DC-link capacitance	C_{dc} = 1000 µF
LC filter	L = 2.5 mH, C= 80 µF
Resistive loads	$R_a = R_b = R_c$ = 15 Ω
Inductive loads	$R_a = R_b = R_c$ = 15 Ω $L_a = L_b = L_c$ =10 mH

In the resistive load's case, the switching signals, the corresponding load voltage of the phase a and the DC link voltage are shown in Figure 11 (a) and 11 (b) with the dead-time influence and with the proposed DTE, respectively. With the dead-time insertion, the load voltage is distorted, the total harmonic distortion(%THD) is 2.8%, while this distortion is greatly reduced with the elimination of the dead time, %THD= 0.53%.

The same test is performed in the case of inductive loads, where the performance signals without and with the DTE are shown in Figure 12 (a) and 12 (b), respectively. The proposed dead-time elimination reduces the %THD of the load voltage from 3.77% to 0.5%. In addition, the proposed DTE reduces the voltage ripple in the DC link, which leads to a decrease in the required size of the DC link capacitor.

From the enlarged image in Figure 11 (b) and 12(b) it can be seen that the time interval between the two switching signals a the zero-current-crossing is more than 5 µs. This confirms the effectiveness and

safety of the proposed DTE. From the results, it can be observed that the ripples of the DC-link voltage are highly reduced with the proposed DTE, resulting in reducing the size of the capacitor required.

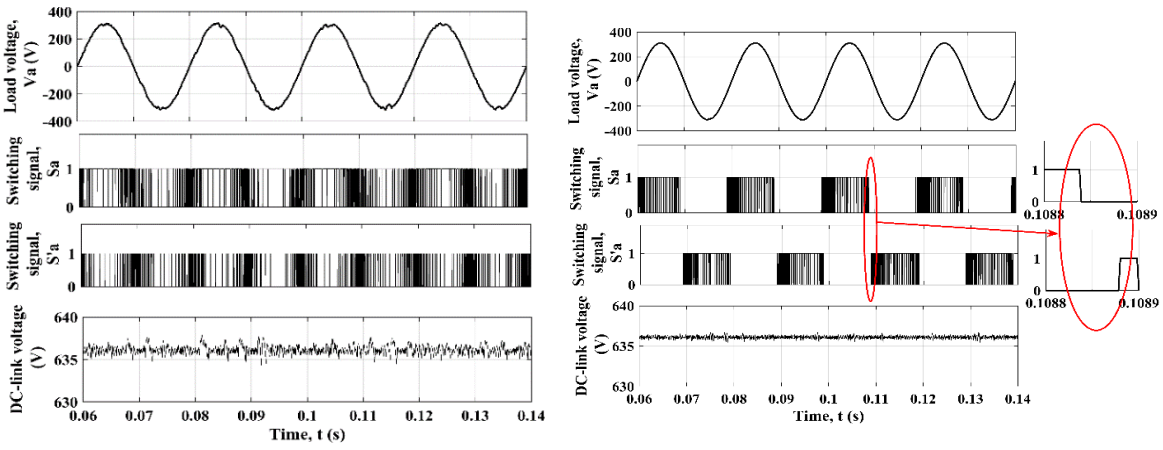

Figure 11. Load voltage of phase a, the corresponding switching signals, and voltages in the DC link of the VSI with resistive loads (a) without the proposed DTE, (b) with the proposed DTE

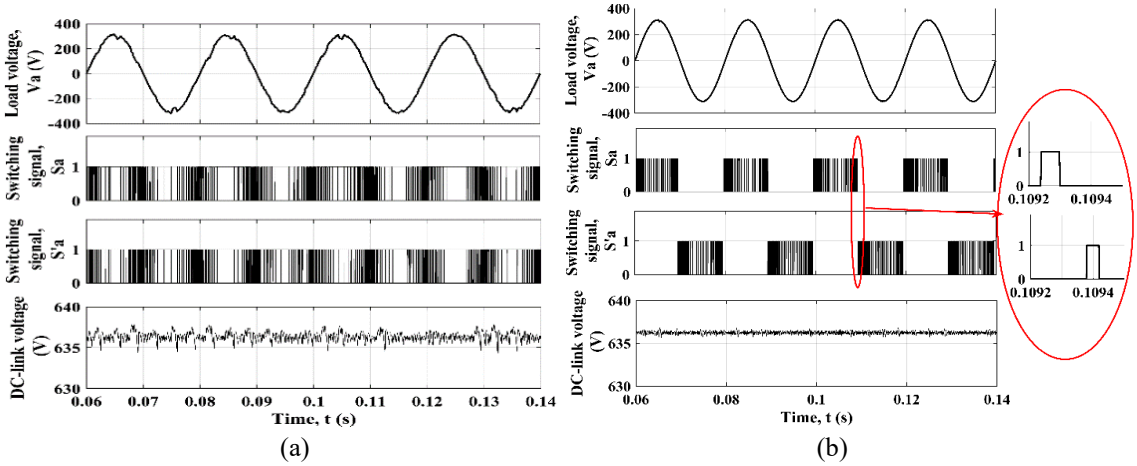

Figure 12. Load voltage of phase a, the corresponding switching signals, and voltages in the DC link of the VSI with inductive loads (a) without the proposed DTE, (b) with the proposed DTE.

6. CONCLUSION

This paper proposes a simple dead-time elimination scheme without any additional hardware or filters for the detection of the output current polarity. A new guarantee algorithm is proposed to solve the problems which may be induced from the output current ripples. This method is applied for three-phase VSI with LC-filter. the method highly reduced the load voltage distortion. This method is effective, safe, can be easily implemented, and independent of the control or modulation technique.

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