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Design and digital implementation of power control strategy for grid connected photovoltaic inverter

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ABSTRACT

This paper presents the optimization design and a detailed implementation in FPGA (Field-Programmable Gate Array) of a power control strategy. This strategy is based on the phase shift angle of the inverter output voltage with respect to the grid voltage and DSPWM (Digital Sinusoidal Pulse Width Modulation) patterns "Phase shift angle-DSPWM" for an inverter for photovoltaic system connected to the grid. The proposed control can synchronize a sinusoidal inverter output current with a grid voltage and control the power injected into the grid. Detailed development of a digital controller with lower hardware and computation requirement is proposed. Description on the digital implementation of the A/D converter, the PI compensator, the phase shift and the DPWM, is provided. This digital control exhibit simplicity, reduction of the memory requirements and power calculation for the control. The functional structure of this system with digital control has been validated with simulations and experimental results.

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1. INTRODUCTION

The overall efficiency of grid-connected photovoltaic power generation systems depends on the efficiency of the DC-into-AC conversion of the inverter. Important improvements in the design and implementation of this power converter device can be carried out [1–6]. Control of active and reactive power injected into the grid; control of dc-link voltage; guarantee high quality of the injected power; reduction of the harmonic distortion, elimination of the DC component injected into the grid; grid synchronization and digital implementation of the control [7, 8]. Pulse width modulation (PWM) technique is used for controlling the voltage source inverters, which injects currents into the grid. Two methods of PWM techniques can be adopted: The PWM technique consist on the comparison of a triangular carrier signal "high frequency" with a sinusoidal reference waveform "low frequency". The intersection point determines the switching waveform. The second method, the PWM technique based on generated switching patterns. The PWM pattern reduce the low order of harmonic components [9], [10]. In this case, the switching patterns are calculated a priori for certain operating conditions and are then stored in memory (look-up table) for use in real time [11–13]. Digital implementation offers advantages over their analogue counterparts [14–17]: immunity to the noise and insensitiveness in the changes of voltage and temperature [13]. FPGA's implementation give suppleness in changing the designed circuit, easy and fast circuit modification without modifying the hardware and rapid prototyping [12].

In this work, the objective is to implement an inverter with a simple power control strategy. That implies to reduce both hardware and software required resources (reducing memory and computing needs of the control system) using FPGA design platform. The proposed control strategy implementation allows to design an inverter with low cost and high reliability, while many other implementations are based on

complex mathematical algorithms that require many resources of both software and hardware. FPGA technology offers a flexible programmable environment and a higher level of versatility. The code is written as blocks to be processed in parallel, which makes the FPGA implementation more attractive.

In PV systems connected to the grid, system control can be divided into two important parts. The MPP control, which extract the maximum power from the PV generator and the inverter control, which ensure the control of active and reactive power generated to the grid, the control of DC-link voltage, high quality of the injected power and grid synchronization [2, 3, 7, 9, 17–19]. The proposed power control method [20–22] is based on the phase shift angle of the inverter output voltage with respect to the grid voltage and DSPWM patterns "Phase shift angle-DSPWM". High power factor can be achieved for a large range of output current. The main advantages are simplicity, few resources, less memory, less circuitry and high accuracy.

This control strategy allows the control of power injected into the grid. Using DPWM patterns for different modulation index ma and the phase shift angle of the inverter output voltage as control parameter. The output current amplitude and the power factor can be controlled, changing the power factor; the injected inductive or capacitive reactive power can be dynamically changed and controlled, for achieving an inverter with advanced accuracy and reliability. In [20–22], the strategy has been developed with methodical description and mathematical analysis. The theoretical predictions has been validate with simulation and first experiment results.

In this paper a detailed implementation in FPGA of this power control strategy, "Phase shift angle-DPWM" for PV inverters based on the look up table, is presented. Description on the digital implementation of the main control blocks, which are the A/D converter, the PI controller, the phase shift and the DPWM, is provided. The proposed control is simple and adapted to FPGA platform; it is attractive for low power grid connected applications and allows controlling the active and reactive power injected into the grid. Moreover, robustness of the proposed control allows designing a low cost and simple inverter with a reduced amount of components, based on a full bridge topology that can be implemented with minimum computational resources.

2. POWER CONTROL STRATEGY

In photovoltaic power system, the control of power factor is achieved by adjusting amplitude and phase angle between inverter voltage and grid voltage as is shown in the phase diagram of the equivalent electrical circuit of the inverter connected to the grid Figure 1.

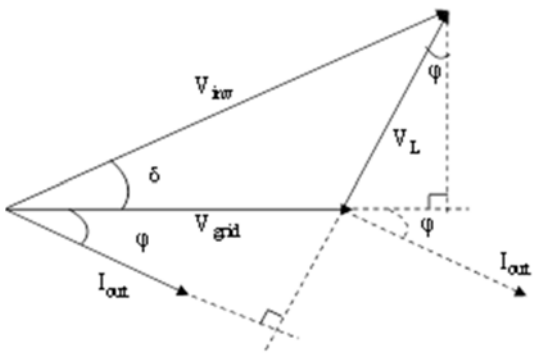


Figure 1. Phase diagram of the equivalent electrical circuit of inverter connected to the grid inverter

The power control is obtained by means of the phase shift angle (δ) of the inverter output voltage, with respect to the grid voltage and the use of SPWM patterns. The power factor is determined by angle (φ) between the grid voltage and the fundamental current component of inverter output current.

Controlling the phase shift of the inverter output voltage, the output current amplitude and the power factor can be controlled, and therefore the magnitude of the active and reactive power injected into the grid [20], [22].

The analysis is established using the inductive filter between the inverter and the grid [24]. Considering the fundamental harmonic (pure sinusoidal wave), as a first approach, the total harmonics (THD)

of the current injected into the grid is assumed equal zero (THD≈0). Therefore, the power factor, PF, is determined, only, by the displacement factor (cosφ), as will be shown in (1) [20–22]

$$PF = \cos\varphi = \frac{m_a \cdot V_{dc}}{\omega L \cdot I_{out}} \cdot \sin\delta \quad (1)$$

To valid the performance of the proposed power control strategy it is necessary, to guarantee a total harmonic distortion not higher than specified 5% as suggests the International Standard IEEE Std 929-2000 [2, 5, 18]. This condition can be achieved calculating and optimizing of using different digital SPWM pattern and selecting an appropriate coupling filter [23] and frequency modulation index (m_f); and the displacement factor (cosφ) has to be within the pre-calculated limits, to guarantee the specified output current. This magnitude can be controlled selecting an adequate amplitude modulation index, m_a, and a phase shift,δ, of the inverter output voltage. In Figure 2, which shows PF vs δ, for two different values of m_a and of the inverter output voltage, V_{inv}, (V_{inv} = ma.V_{dc}), it can be seen, that with two values of ma we can reach the PF ≈ 1 In a wider range of δ.

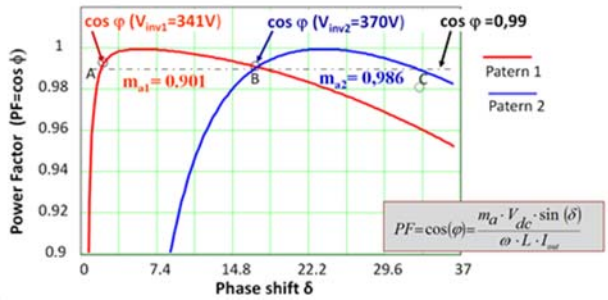


Figure 2. Power factor (PF) according to the phase shift δ

The choice of inductance grid connection influences the harmonic content of the current injected into the grid and the maximum active and reactive power that the inverter can deliver to the grid. High inductances lead to reduced harmonic distortion. However increasing the inductance in the filtrate shows a number of drawbacks: cost reduction and transfer of power inverter.

To analyze the behavior of this control strategy for single-phase inverter connected to the grid via an L or LCL filter. It has been using the expression of power factor mentioned in (1) and to measure the distortion of the output current, the total harmonic distortion, THD is often used. Total Harmonic Distortion is a measure of the proportionality between the fundamental and the sum of all other frequencies in the current waveform. As show in (2) defines the THD used here:

$$THD_i = \frac{\sqrt{I_{out}^2 - I_{out1}^2}}{I_{out1}} \quad (2)$$

Where Iout is the total current; (RMS) is the Root means square and Iout1 is the fundamental current (RMS). The relationship between the switching frequency fc and the inductance value of output filter is presented, assuming a power factor PF= 0.996.

In Figure.3, the simulation results of the inverter connected to the grid via an L filter and an LCL filter. Assuming a PF = 0.996, it can be conclude that for lower switching frequencies (modulation indexes for low frequencies) less than 5kHz, the inductance value of the L filter is higher than the value of the inductance (L1 + L2) of the LCL filter.

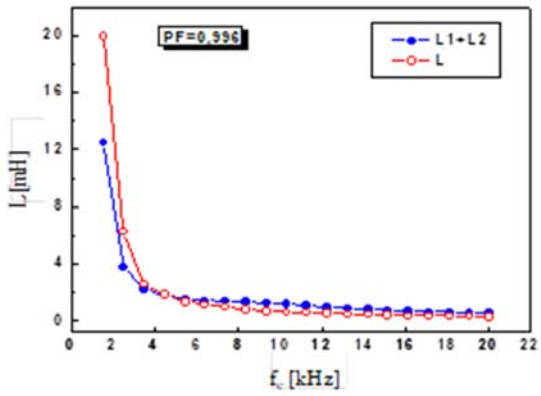


Figure 3. Inductance of L filter and LCL filter as function of switching frequency fc, for PF = 0,996.

3. PROPOSED CONTROL STRUCTURE

The proposed control system, for a photovoltaic system connected to the grid is shown in Figure 4. The photovoltaic generator (PVG), DC/DC for a maximum power point tracking (MPPT) and a PWM inverter (DC/AC).

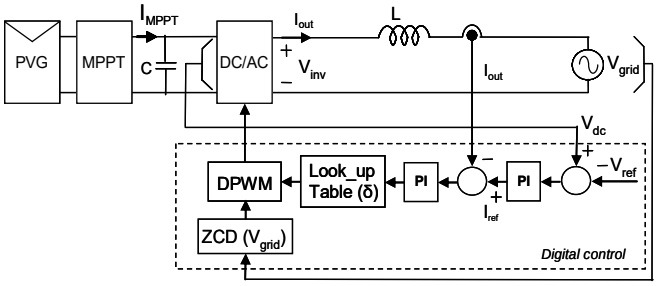


Figure 4. Control structure for a single phase inverter [20]

The DC/DC converter is employed to boost the PV-array voltage to an appropriate level based on the magnitude of grid voltage, while the controller of the DC–DC converter is designed to operate as a maximum power point tracker (MPPT). The perturb-and-observe method is adopted owing to its simple structure and it requires fewer measured parameters [24, 25]. This strategy is implemented to operate under rapidly changing solar radiation, using only one variable. The constant voltage method is accomplished by keeping the voltage in the PV terminals constant and close to the MPP.

The control loop for the PWM inverter is assured by the output current control, the DC bus control and synchronizing to the grid, to inject power into the grid at all time. The output voltage of the PWM inverter is already set by the utility PV modules. Therefore, the inverter is controlled to ensure only power injection into the grid. In Figure 5, are represented an internal and an external control loops of a controller. The internal one in order to control the inverter output current and the external one to control the DC bus V_{dc}. The reference of the output current (I_{ref}) depends on the DC bus voltage (V_{dc}) and its reference (V_{ref}). A low pass Filter is incorporate in order to ensure that high frequency switching noise present in the measured inverter output current signal does not pass through to the PI controller.

The control structure is associated with proportional–integral (PI) controllers since they have a satisfactory behavior when regulating dc variables. The gain and time constants has been calculated for the two PI controllers. The Gain of the current PI controller is equal to 0.9819, where the time constant is about 0.001717. In addition, the gain of the voltage PI controller is 2.438, and the time constant is about 0.02758. A look up table to store the different patterns and the zero crossing detector (ZCD) for synchronizing the DPWM with the grid voltage.

4. PROPOSED CONTROL IMPLEMENTATION

The block diagram of the control is detailed in Figure 5. To each amplitude modulation index m_a corresponds a switching pattern SPWM characterized by switching angles (α_1, α_2, α_3, α_n, α_{n+1}) defined by the number of intersections, Only the change angles are stored, High accuracy resolution can be achieved and when using symmetric patterns the look up table can be reduced. Each pattern is accompanied by attributes such as a maximum and a minimum phase angle, a minimum and a maximum current stored in the lookup table (ROM). Once the data are stored, the DPWM converts the data code patterns and its attributes in a pulsed signal that will be generate the switching signals for the inverter transistors.

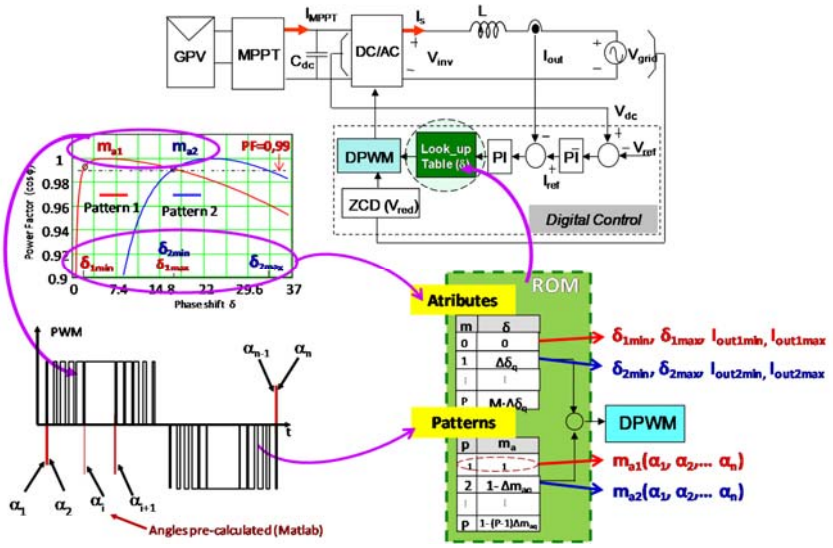


Figure 5. Scheme of the proposed control implementation

The control algorithm implemented in FPGA is shown in Figure 6. The reference current is update in each period of the control system and compared with the output current of the inverter. Depending on the sign error, the controller increases or decreases the phase angle δ between V_{inv} and V_{grid} to compensate the error. Once the output current is equal to the reference current, the control keeps the current phase angle. The design method of inverter proposed in this work is attractive to medium and low power PV system, which can control active and reactive power for relative low cost.

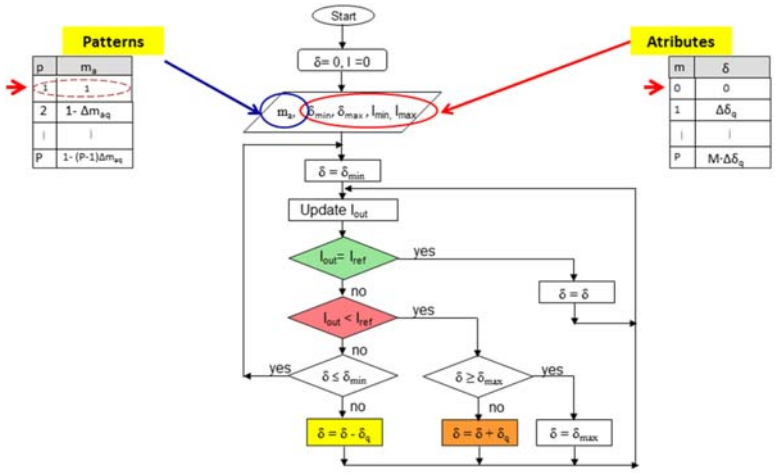


Figure 6. Control algorithm

In this control scheme, the controller is implemented by specific hardware in FPGA. These devices are particularly suitable for the direct generation of trigger signals for the switches, so the DPWM block is actually embedded within the controller; it is one of the advantages of the specific hardware features. However, the specific hardware features two distinctive advantages: greater accuracy and flexibility in block DPWM, it is reached and it is possible to generate any number of trigger signals, which is impossible in a DSP because they have one or as many two DPWM block. Normally, all signals involved in the control loop are continuous. However, when using a digital controller some of the continuous functions are replaced by discrete sequences, thus two distinct domains appear the continued dominance (Analog) connector on the process side and the (digital) discrete domain on the side of the regulator. To connect both domains some kind of interface is needed. Usually these interfaces are analog / digital converters (DAC) and digital / analog converters (DAC).

The following describes and requirements for each of the digital blocks that are part of the control loop to ensure certain design specifications are discussed: filter, PI controller, modulator DPWM, look up table, zero crossing detector ZCD. It is clear that each of the blocks forming the control loop, directly affect the system response.

5. DIGITAL CONTROLLER

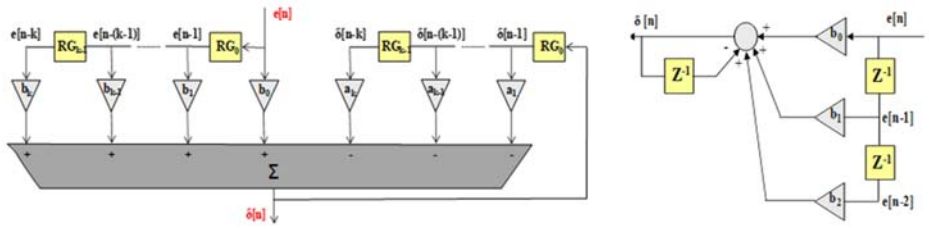
The proportional integral controllers PIs are a good compromise between the simplicity in digital implementation and the obtained performances. The PI compensator designed in this study guarantee the stability of the output-regulated variable, the phase shift. The hardware realization of the compensator transfer function in the FPGA platform is achieved by using the corresponding difference equation:

$$D[n+1] = k_p\, e[n] + k_i D_i[n] \tag{3}$$

Where: k_p and ki are the coefficients that determine the proportional, derivative and integral gain, respectively. $D[n]$ is the value of the duty cycle at discrete time n; $e[n]$ is the digitized value of the error; $D_i[n]$, is the state of the integrator; Once the digital code of the error, e[n] is obtained, the value of the phase shift angle δ[n] is generated following the scheme shown in Figure 8.

The coefficients of each gains (K_p and K_i), may be rounded to powers of 2 in practice. This makes it implementation easy using binary shifts. This control law can be implemented using difference equations, look-up tables or calculated directly using microprocessors with high performance. In this paper, the proposed phase shift control is based on that for a determined voltage of the DC bus and current modulation index, m_a, it can inject current into the grid by varying the phase angle between the inverter output voltage and the grid voltage.

The control parameter in this case, is the angle phase δ generated between output voltage of the inverter and the grid voltage. The updating of the current value of the phase shift according to the law of the implemented control is realized. It is clear that the method used is to average the error between the reference current and the actual measured value in several cycles of grid voltage, so that regulatory requirements will ensure stability of the system [19], [36]. Direct representation of differentials equation and operating modes of Linear Regulator for this case are shown respectively in Figure 7(a) and Figure 7(b).



(a) (b)

Figure.7. (a). Direct representation of differentials equation and (b). Operating modes Linear Regulator

The A/ D converter needed to implement the controller must have better performance (resolution) with greater number of bits (n + 1). This is due a greater number of levels of quantification are needed. The

voltages that define the tolerance band limit these levels. Once the error signal e [n] is obtained, the value of phase shift δ [n] is generated according to Figure 7.

$$\delta[n] = -\delta[n-1] + b_0\, e[n] + b_1\, e[n-1] + b_2\, e[n-2] \tag{4}$$

To avoid excessive FPGA resource consumption, fixed-point format is used in the rounding of the difference equation coefficients (b0, b1 and b2) when implementing the compensator transfer function in hardware. Moreover, in order to improve the transient response of the converter, the time delay of the analog/digital (A/D) converter should be minimized. Therefore, a high-speed A/D converter is needed.

6. DIGITAL SPWM

In this work, the PWM generator is based on only one counter witch guarantee the synchronism of all signals, the address signal, syncro-signal and the control signal. In Figure 8, is shown the simulation results of DPWM signals implemented in ModelSim. (Vg1, Vg2, Vg3, and Vg4) which represent the PWM signal for each IGT of the single-phase inverter.

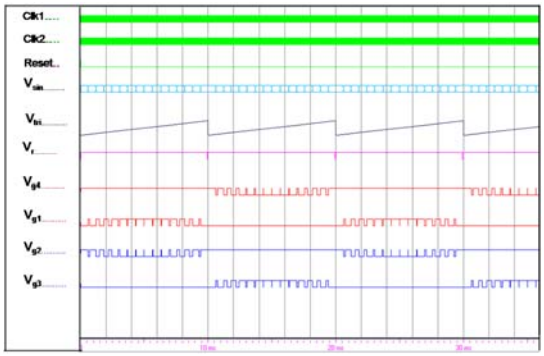


Figure 8. DPWM signals

7. DIGITAL PHASE SHIFT IMPLEMENTATION

Figure 7 (4 section), shows the control algorithm of the inverter output current based on the phase shift of the inverter output voltage. The phase shift is designed to provide flexibility in order to produce either lagging, leading or in phase, in order to adjust the power factor.

Initially the phase counter is loaded to the shift phase angle value equal zero (δ = 0). The control have to maintain the adequate shift phase angle which accomplish that the inverter output current I_{out} equal to the reference I_{ref}. The sign of the phase angle depends on the power factor character (inductive or capacitive). From the resolution with which the magnitude of the output current I_{out} is represented, the resolution (number of bits) of the phase shift, I_{ADC} resolution of the analog digital A / D converter, expressed in current, will depend on maximum output current I_{max} and increment current $I_{q:}$

The resolution of the converter A/D depend on the magnitude of the current to steady

$$\mathrm{N}_{\mathrm{ADC}} = \log_2 \cdot \frac{I_{\max}}{I_q} \tag{9}$$

From design topology, the selected approach has been the regulation of the output current of the inverter (I_{out}) as a function of the δ offset [2]-[4].

$$\delta = \cos^{-1}\left(\frac{V_{inv}^2 + V_{red}^2 - \omega^2 \cdot L^2 \cdot I_s{}^2}{2 \cdot V_{inv} \cdot V_{red}}\right) \tag{10}$$

From (9), each value of the angles δ can be calculated for each output current value of the inverter I_{out} corresponding to the current of the maximum power point on the side of the photovoltaic system. Once the phase shift angle δ has been calculated, the phase shift angle φ between the inverter output current and the grid voltage (1), is determined, which allows to determine and to control the active power and reactive power injected into the grid by the inverter.

Since the output current I_{out} is a function of the output voltage of the inverter V_{inv} and the phase shift δ, then V_{inv} can be expressed as a function of the duty cycle (d) (10).

$$V_{inv} = d \cdot V_{dc} \tag{11}$$

The principle operation of this control strategy, based on the PWM control and phase shift, consists of sensing the current and calculating the phase shift. The output current can be represented by a single PWM switching pattern (d = constant) as a function of a single state variable: phase shift angle δ between the output voltage of the inverter V_{inv} and the voltage of the grid V_{grid}.

$$I_{out} = f(\delta) \tag{12}$$

This is a very important function since it greatly simplifies the hardware complexity by transferring the previous calculations to a PC of the SPWM switching pattern. In a "look up table" we store each phase shift angle values bye their corresponding current magnitude I_{out}. Using as a design platform an FPGA, the phase shift angle can be generated according to the clock and the grid frequency (t_s corresponding to f_s).

$$\delta_q = \frac{\delta_{\max}}{2^{N_\delta}} \tag{13}$$

Taking the maximum number of pulses corresponding to the maximum phase shift angle for an I_{out} max, the counter of the phase shift angle can be sized.

$$N_\delta = \log_2 \frac{\delta_{\max}}{\delta_q} \Rightarrow 2^{N\delta} = \frac{\delta_{\max}}{\delta_q} \tag{14}$$

The design of the look up table will be determined by the maximum angle of phase shift δ_{max} and by the resolution of the output current I_{out}. Figure.9, shows the inverter output current I_{out} as a function of the phase angle δ. This figure represents the output current I_{out1} for an inverter output voltage V_{inv1} = 342 V (m_{a1} = 0.910) and the output current I_{out2} for V_{inv2} = 370 V (ma2 = 0.986), ensuring a power factor PF> 0. 99. Only two patterns are necessary to cover range from 3.5 A to 33.4 A, while PF remains always higher than 0.99. Therefore, the number of DSPWM patterns is determinate by the m_a, and the minimum affordable PF (with respect to the quality of injected current).

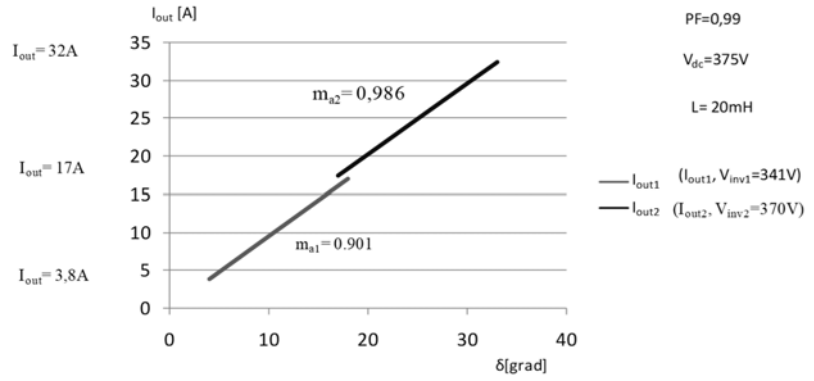


Figure 9. Inverter output current, I_{out} vs angle phase δ

In Figure 9, it is possible to observe how the current I_{out} changes as a function of the phase shift δ. As a result, the output current I_{out}. Discretized in 2^{N_δ} intervals as a function of the phase shift δ represented by a finite number N_{CD} bits for each values of the current of the system.
The condition of the limited duty cycle to be happened:

$$N_\delta = \log_2 \frac{\delta_{\max}}{\delta_q} \tag{15}$$

Then:

$$N_\delta = N_{ADC} + 1 \tag{16}$$

$$I_{q\ \delta} < I_{qADC} \tag{17}$$

It means that the resolution expressed in current must be greater than that of the A / D converter.

The FPGA used in this work is Xilinx SPARTAN-3 XC3S200 FPGA family board processor. To implement the proposed control strategy, XC3S200 processor is used as a PWM generator to build the appropriate gating signals to the inverter switches. Figure 10, shows the simulation results of the control Strategy "Phase shift angle-DPWM"; the DPWM signals, the angle phase and the DZC.

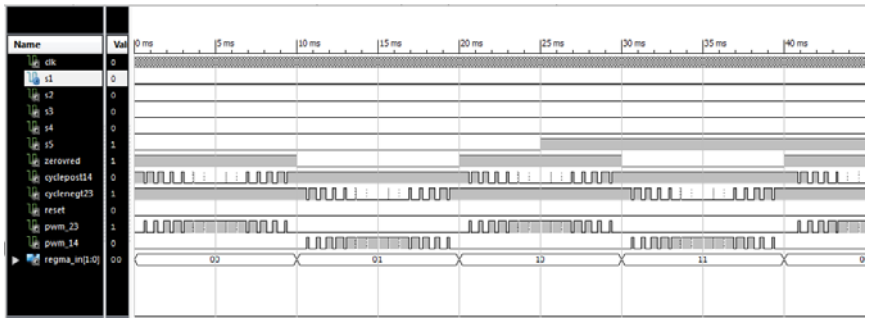


Figure 10. Proposed high-resolution control strategy based on FPGA resources

The proposed Digital Pulse Width Modulator (DPWM) takes advantage of the capability of FPGA to shift the phase of the clock in small increments. A Spartan-3E device from Xilinx has been used in the experimental results. The solution has been implemented by means of a counter based DPWM architecture and a specific block available in the FPGA [37]. The time period of the system clock is sliced by means of the proper phase shifting of the clock signal. This solution provides a lower equivalent FPGA clock period.

8. EXPERIMENTAL RESULTS

Figure 11 shows a prototype of single-phase inverter with the digital control "Phase shift angle-DSPWM" implemented in a FPGA platform (Spartan-3 of Xilinx) realized and tested
V_{grid} =230 V, and coupling inductance L=20 mH.

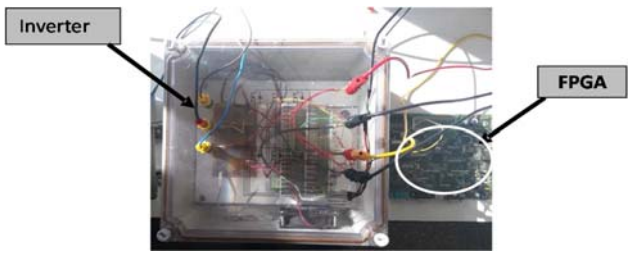
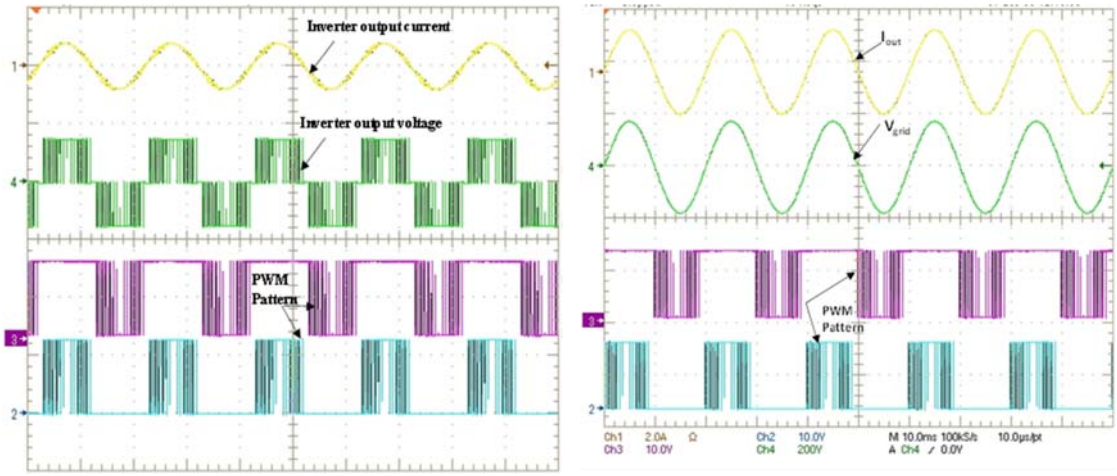


Figure 11. Single-phase inverter prototype

Figure 12(a) shows the PWM Pattern, the inverter output current I_{out} and inverter output voltage V_{inv}. Figure 12(b) shows the Inverter output current and grid voltage and PWM Patterns.



(a) (b)

Figure 12. (a). PWM Pattern, inverter output current and inverter output voltage, (b). Inverter output current and grid voltage.

The experimental results show the viability of the SPWM method proposed and validate the theorical predictions. The current total harmonic distortion (THD) is 3.5%, which is below the suggested value by Standard IEEE Std 929-2000.

9. CONCLUSION

The paper has focused on the detailed implementation of the power control strategy of PV inverter connected to the grid. The proposed strategy based on a "Phase shift angle–DSPWM" pattern is able to control both the active and reactive power and reduce both hardware and software required resources using FPGA design platform. Digital implementation of the main control blocks, which are the A/D converter, the compensator PI, the phase shift and the DPWM, has been provided. However, the proposed control algorithm provide flexibility to adjust the power factor and regulate the reactive power. This digital power control strategy has been implemented in FPGA platform and validated with experimental results. The experimental results show the viability of the SPWM method proposed, the simplicity of the digital implementation, reduction of the memory requirements and power calculation for the proposed control.

This technique is simple and adapted to FPGA platform, it is attractive for low power grid connected applications and allows to control the active and reactive power injected into the grid. Moreover, robustness of the proposed control allows designing a low cost and simple inverter with a reduced amount of components, based on a full bridge topology that can be implemented with minimum computational resources.

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