Experimental verification of three phase quasi switched boost inverter with an improved PWM control

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Article Info	ABSTRACT
	In this paper, an experimental investigation of a three phase quasi Switched Boost Inverter (qSBI) topology is proposed and analysed with an improved Pulse Width Modulation strategy. The qSBI is capable of providing both boost and inversion actions in a single stage. The improved PWM control technique can provide a higher boost with the reduced duty ratio. The theoretical analysis presented in this work is validated using an experimental set up of 100W qSBI topology and hardware results are shown for verification. The improved PWM strategy is implemented and firing pulses are generated in FPGA SPARTAN 3E kit. With the duty ratio of 0.05, the peak ac load voltage of 80 V is obtained. The performance of three phase qSBI is analysed with both conventional PWM strategy and improved PWM strategy. The observations are presentated in detail.

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1. INTRODUCTION

The vast growth of sustainable energy sources like solar, fuel cells, wind and geothermal energy *etc.*, are gaining the major interest among most of the researchers due to the reduction of fossil fuels and other conventional energy sources [1]. Designing a suitable power electronic converter is the major task in transforming the available DC power to AC power in the case of solar PV systems. With the help of a traditional three phase Voltage Source Inverters (VSI) [2, 3], the available DC voltage is inverted to a reduced voltage level. Whenever the output voltage requirement is more than the available DC voltage, a boost inverter needs to be connected which forms a two stage power conversion. It also increases the cost, size and weight of the converter. Both the devices in a single leg should not be switched on at the same time. Electro Magnetic Interference (EMI), dead time, shoot through are the other major issues in traditional VSI [4].

To eliminate the complex two stage structure, Impedance Source Inverter (ZSI) is proposed in 2002 [5]. The modified topologies of ZSI like, a class of quasi ZSI (q-ZSI)[6], extended boost ZSI/ q-ZSI [7], Trans Z Source Inverter (Trans ZSI)[8] are presented to obtain continuous input current. In traditional ZSI, inductors are replaced by switched inductor cells to obtain a higher boost [9]. The tapped inductor ZSI (TL-ZSI [10]), TZ-Source Inverter (TZSI) [11] possess all the advantages of traditional ZSI by using transformer. There are cascaded TZSIs, alternate cascaded switched/ tapped inductor cells, cascaded multi cell Trans ZSIs are available in literature [12-16]. All the ZSI topologies are of bulky, heavy and of large volume due to the presence of large value of passive elements. Hence it results in higher loss and reduced efficiency. To overcome the aforementioned issues Switched Boost Inverter (SBI) and various modulation algorithms of SBI are proposed by researchers in [17-20].

A class of quasi-SBIs (qSBIs) is suggested in [21] to have continuous current profile. The qSBI has a reduced count of passive elements and the features are similar to that of ZSI. A Current Fed Switched

Inverter (CFSI) is suggested in [22]. The CFSI has the boost factor (1-D) times higher than SBI. To produce high voltage gain, CFSI needs to be operated at high shoot through duty ratio which results in reduced modulation index. Switched inductor and switched capacitor based boost inverter topologies are proposed in [23-24]. Since the conventional SBC control strategy has restriction on its modulation index, a modified control algorithm is proposed in [25] to extend the modulation index. A single phase quasi SBI topology is analysed with the modified SBC technique is presented in [25].

In this paper, a three phase quasi SBI with an improved simple boost PWM strategy is discussed to resolve the drawback of reduced modulation index. Compared to the conventional SBC method, the improved PWM technique can offer a high gain using a reduced shoot through duty ratio and higher modulation index. So the stress across the switches, diodes and capacitors are reduced significantly. In this modified PWM control, the switch S_0 is gated during the active state of the inverter circuit. A 100 W three phase qSBI topology is developed and tested with an input voltage of 36 V. The topology with the improved PWM provides the boosted dc voltage of 80 V and the boost factor of 2.22 whereas the traditional PWM offers the boost factor of only 1.11. The inverter topology is simulated in MATLAB/SIMULINK environment and it is validated by experimentation. The experimental results are presented in detail.

2. THREE PHASE qSBI TOPOLOGY

The single phase qSBI is proposed in [21]. Figure.1 shows the circuit diagram of three phase qSBI topology. It includes an inductor L, a capacitor C, two passive switches (D_1, D_2), seven active switches ($S_0 - S_6$) and a resistive load. An LC filter is connected at the inverter output terminal to filter out the harmonics present in the inverter output voltage.
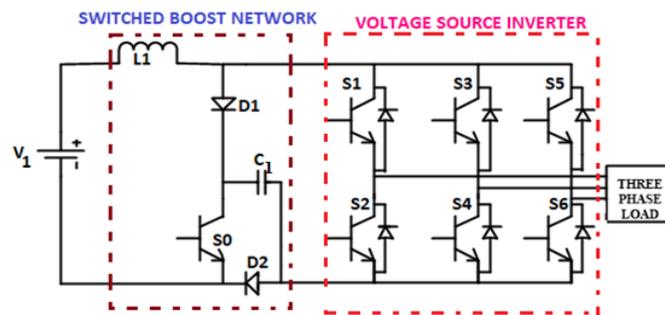

Figure 1. Three phase quasi switched boost inverter

3. MODIFIED SBC MODULATION STRATEGY

In conventional SBC method, reference signals are compared with triangular carrier signal to generate pulses for the inverter switches.The positive and negative envelops are compared with triangular signal to generate shoot through pulses.The shoot through pulses are ORed with the bridge inverter pulses to produce boosting action. The improved PWM control strategy is illustrated in Figure 2(a) [25]. A shoot through envelop V_{sh} is compared with a high frequency repeating sequence V_{saw} (saw tooth waveform) of magnitude 2 to obtain the pulse for the boost network switch. Again the shoot through envelop is compared with the repeating sequence 1 (triangular carrier pulse) of double the frequency to generate the shoot through pulse. Then, sinusoidal modulating signals are compared with the repeating sequence 2 (triangular carrier pulse) to generate the firing pulses for the inverter switches S_1 to S_6. Finally, shoot through signals are added into the signals of the switches in the H-bridge to operate along with the boost inverter switch S_0. The control logic is shown in Figure 2(b).
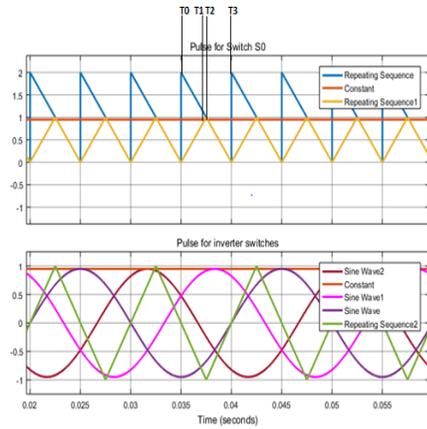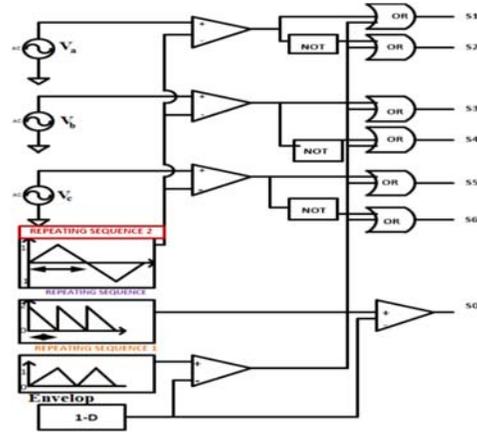
Figure 2. (a) Modified simple boost control PWM   Figure 2. (b) Control logic diagram

4. STEADY STATE ANALYSIS OF THREE PHASE qSBI

With the conventional PWM technique, the circuit can operate in two modes [21]. One is the shoot through state during which all the active devices in the circuit remains on. The other mode is the non- shoot through state during which the inverter works as the conventional VSI. When the inverter is analysed with the modified boost control method; there are three different operating modes namely, shoot through state, active state-1 and active state-2 as shown in Figure 3.
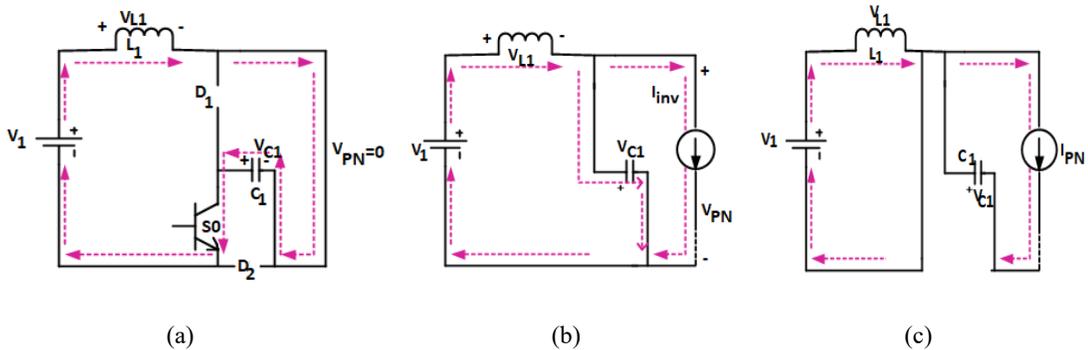

(a)   (b)   (c)

Figure.3. operating modes of three phase qSBI

a)   Shoot through state
b)   Active state-1
c)   Active state-2

4.1. Shoot through state

During shoot-through state $[T_1 - T_2]$, all inverter bridge switches ($S_1 - S_6$) are on along with the boost network switch (S_0) as shown in Figure 3(a). Both the diodes D_1, D_2 are reverse biased. The inductor (L_1) is charged by the capacitor (C_1) along with the input DC source (V_1).

$$V_L = V_I + V_C \tag{1}$$

$$I_C = -I_L \tag{2}$$

4.2. Active state-1

During non-shoot-through state 1 $[T_2 - T_3]$, switch S_0 is turned off as shown in Figure 3(b). The inductor discharges through the capacitor and the duration for this interval is $(1-D)T_S/2$. During this mode power flows through the load

$$V_L = V_I - V_C \tag{3}$$

$$I_C = I_L - I_{PN} \tag{4}$$

4.3. Active state-2

During non-shoot-through state 2 $[T_0 - T_1]$, switch S_0 is turned on as shown in Figure 3 (c), and the inverter circuit operates in conventional states. The switching period is same as that in the non-shoot-through state 1.

$$V_L = V_I \tag{5}$$

Applying volt second balance using (1)-(5),
The capacitor voltage is given by,

$$V_C = \frac{2}{1-3D} V_I \tag{6}$$

Inverter input current is given by,

$$I_{inv} = \frac{1-3D}{2(1-2D)} I_L \tag{7}$$

Peak DC link voltage is derived as,

$$V_{PN} = V_C = \frac{2}{1-3D} V_I \tag{8}$$

Boost factor is given as,

$$B = \frac{V_{PN}}{V_I} = \frac{2}{1-3D} \tag{9}$$

The expression for the RMS output voltage of three phase qSBI with traditional SBC modulation strategy is given by,

$$V_{rms} = \frac{\sqrt{3}M.B.V_I}{2\sqrt{2}} = \sqrt{3}.M.\frac{V_I}{1-2D}.\frac{1}{2\sqrt{2}} \tag{10}$$

Similarly, the expression for the rms line voltage with improved PWM is given by,

$$V_{rms} = \frac{\sqrt{3}M.B.V_I}{2\sqrt{2}} = \sqrt{3}M.\frac{2}{1-3D}.\frac{V_I}{2\sqrt{2}} \tag{11}$$

5. PASSIVE COMPONENTS DESIGN

The passive components, inductance and capacitance in the qSBI topologies are chosen based on the High Frequency(HF) peak –peak ripple content in inductor current and High Frequency(HF) peak-peak ripple on capacitor voltage [25]. The ripple content present in the inductor current (ΔI_L) and in the capacitor voltage ((ΔV_L) are calculated by $r_L\%$ and $r_C\%$ respectively. The percentage of ripple content is calculated by the following equations.

$$L > \frac{V_g{}^2(1-D)(1+3D)T}{2r_L\%(1-3D)P_0}I_L \tag{12}$$

$$C > \frac{(1+D)(1-3D)TP_0}{8r_C\%V_I{}^2}I_L \tag{13}$$

The ripple inductor current and ripple capacitor voltage are obtained as follows,

$$\Delta I_L = \frac{V_g(1-D)(1+3D)T}{2L(1-3D)}I_L \tag{14}$$

$$\Delta V_C = \frac{I_L(1+D)T}{4C} \tag{15}$$

For the modified SBC PWM scheme, the peak values of *LF* (Low Frequency) inductor current and the *LF* capacitor voltage are calculated as [25],

$$i_{L\_P} = \frac{(1-3D)MI_m}{16LC\omega^2-(1-3D)^2} \tag{16}$$

$$V_{C\_P} = \frac{4\omega LMI_m}{16LC\omega^2-(1-3D)^2} \tag{17}$$

The values of passive components are calculated as per the expressions given in (12) and (13) [25]. The peak values can be obtained by substituting the selected inductance and capacitance into (14) and (15). If the peak values of *LF* ripple are in the desired range, the values calculated are the desired one. If the values exceed the limit, the values of passive elementss need to be increased, and need to be re-checked (16) and (17) till the values reach the desired range.

6. SIMULATION RESULTS

The topology is simulated in MATLAB/SIMULINK environment. The simulation parameters of the three phase qSBI are listed in Table.1. The input voltage is taken as 36 V and the inductor current which is connected in series with the dc source is observed as 2.9 A. It is shown in Figure. 4(a). The voltage stress across diodes and the boost network switch are obtained as 80 V as shown in Figure. 4(b). The capacitor voltage and boosted dc link voltage are obtained as 80V as obtained in Figure.4(c).

The simulated waveform of unfiltered peak load current is shown in Figure.4(d). The peak line voltage is obtained as 150 V at a reduced duty ratio of 0.05 which is presented in Figure. 4(e). The harmonic spectrum is obtained as shown in Figure. 4(f).

Table.1. Simulation specification

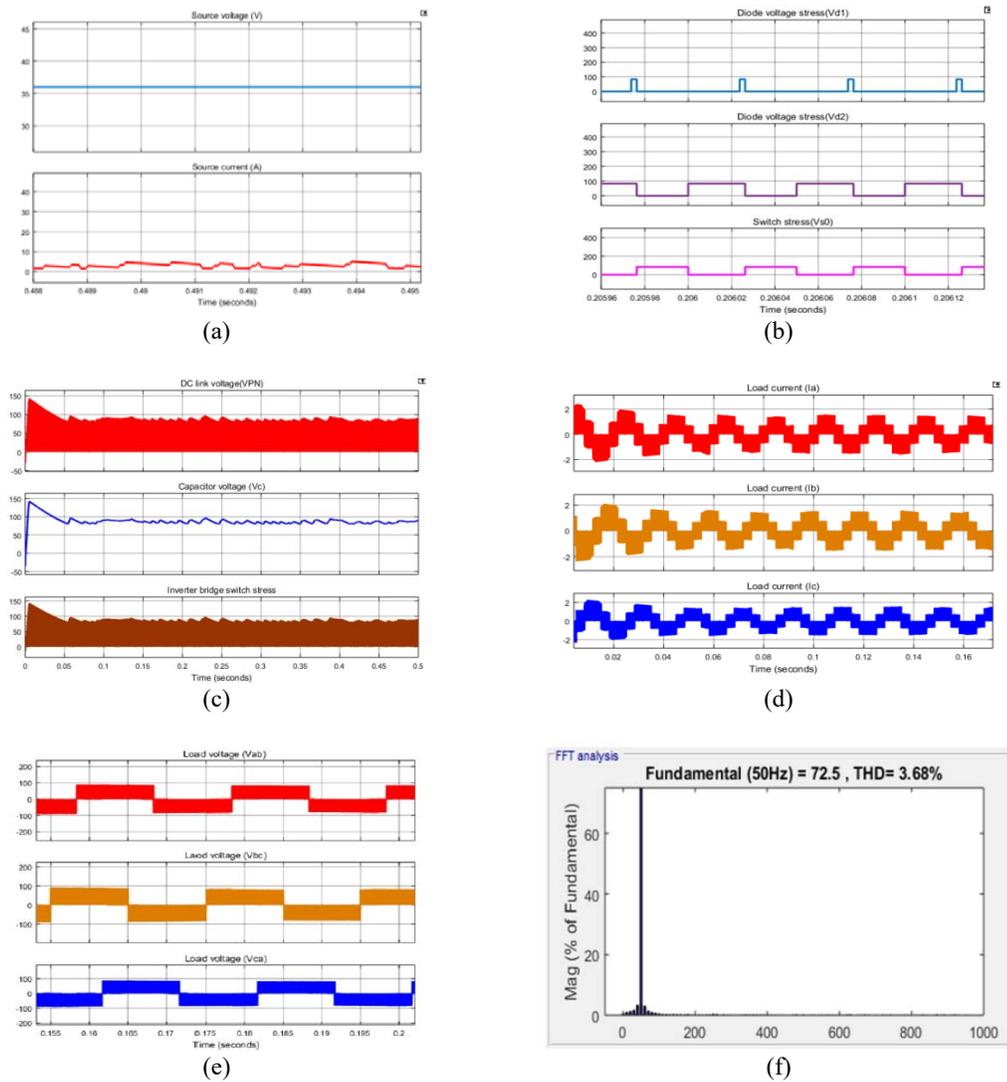| Parameter/Components	Attributes	
Input voltage (V_g)	36 V	
Inductance (L_I)	1.3 mH	
Capacitance (C_I)	680 µF	
Modulation index (M)	0.95	
Shoot through duty ratio (D)	0.05	
Switching frequency (f_{tri})	S_0	= 20 kHz
	S_1-S_6	= 10kHz

(a)

(b)

(c)

(d)

(e)

(f)

Figure 4. Simulation results, (a) Simulated results of source voltage, (b) Diode and Switch voltage stress and source current, (c) DC link voltage,capacitor voltage, (d) Load current waveforms And inverter bridge stress, (e). Unfiltered load voltage waveform, (f) Harmonic spectrum

7. EXPERIMENTAL ANALYSIS OF THREE PHASE QSBI

The laboratory set up of three phase qSBI topology is shown in Figure.5. The hardware set up is made with the same parameters as it is considered for the simulations.

Table 2. Hardware components specification

Components	Manufacturer	Attributes
S_1-S_6	MOSFET(IRFP460)	500 V, 20 A, R_{DSon} = 0.27Ω
S_0	MOSFET- IRFP4668	200 V, 130 A, R_{DSon} = 8mΩ
D_1, D_2	Diode(STPS60SM200C)	200 V, 60 A, V_F = 0.7V
FPGA	SPARTAN 3E	-
Driver circuit	Gate driver(TLP250)	0.1μF, 65V, 22Ω, 1kΩ

Figure. 6(a) and Figure.6(b) show the pulses generated for phase A and the boost network switch (S_a) in FPGA platform. Figure. 6(c) shows that the inverter bridge stress. It is obvious that the switch stress is equal to that of the dc link voltage since the dc link voltage is observed as 81 V from the Figure.6(d). The three phase peak ac load voltages of 80V are obtained as shown in Figure. 6(e) and Figure 6(f).
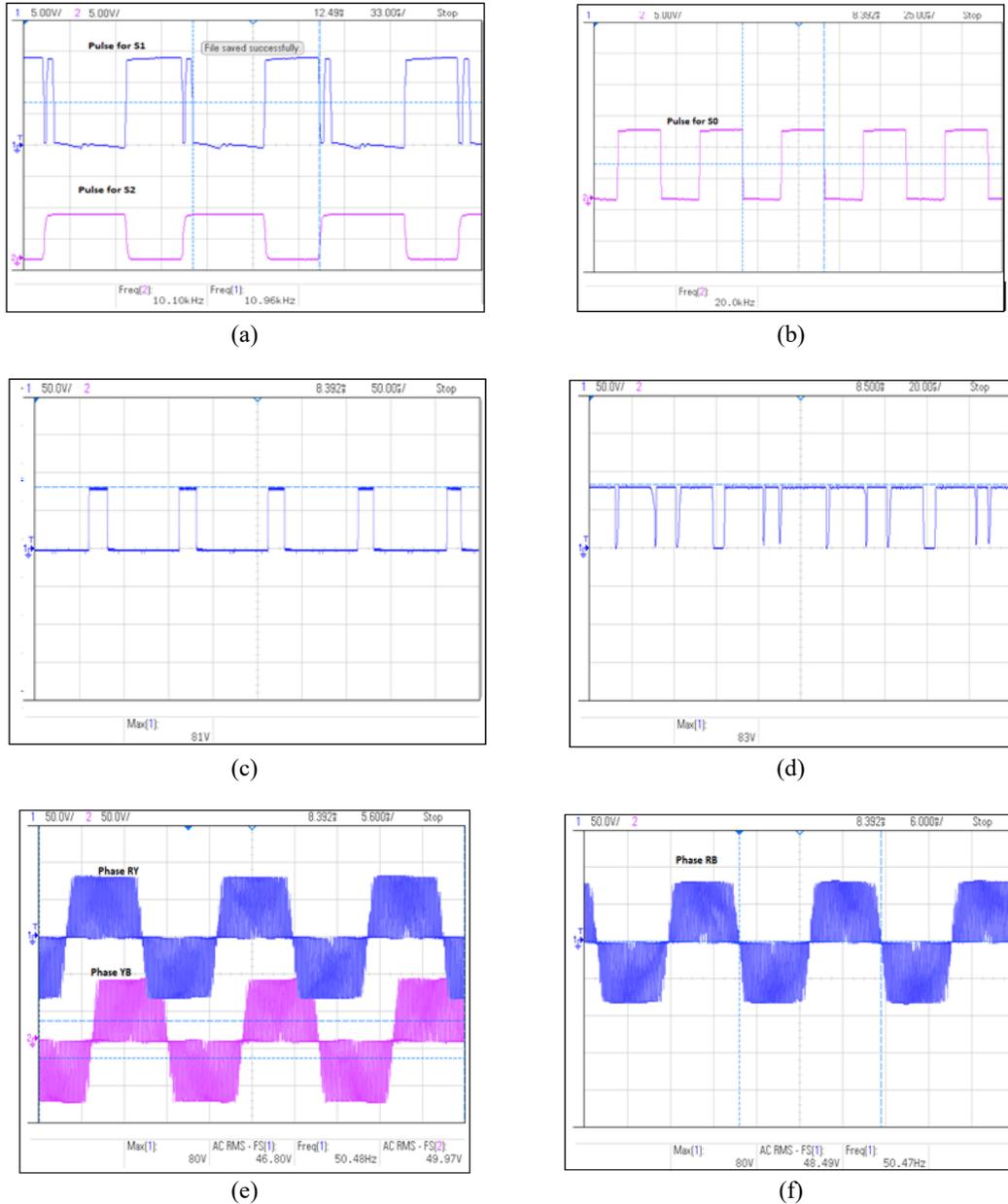

(a)

(b)

(c)

(d)

(e)

(f)

Figure 6. Experimental results, (a)Pulse for phase A, (b) Pulse for boost network switch (S_a), (c) Voltage stress across inverter switch, (e) Load voltage waveforms of phase RY, (f) Load voltage waveforms of phase RB Phase YB

8.   PERFORMANCE ANALYSIS OF THREE PHASE QSBI

A performance analysis is done on three phase qSBI with traditional SBC control strategy and improved PWM control strategy.

8.1. Boost factor(B) Vs Shoot through duty ratio(D)

A graph as shown in Figure 7(a) is plotted between boost factor (B) and shoot through duty ratio (D) with the following relationships. The boost factor expession for three phase qSBI with traditional PWM strategy is given by [21],

$$B = \frac{V_{PN}}{V_g} = \frac{1}{1 - 2D}$$ (18)

Similarly, the boost factor expession with improved PWM strategy is given by[25]

$$B = \frac{V_{PN}}{V_g} = \frac{2}{1 - 3D}$$ (19)

Under the improved PWM control, the qSBI can provide higher boosted voltage as compared to the traditional SBC modulation strategy for the same shoot-through duty ratio. At the same time, the voltage stress across the switches is increased. It is understood from the plots that the improved SBC can provide the higher voltage boost of 2.22 whereas the conventional SBC technique offers only 1.11 for the same duty ratio of 0.05.

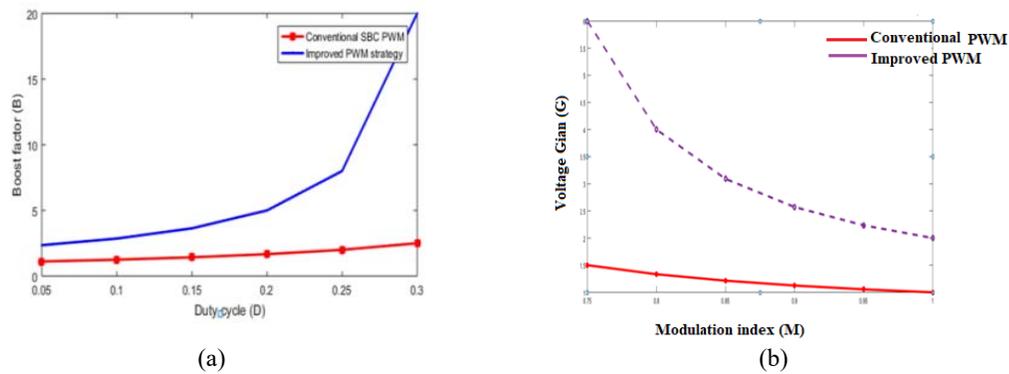(a)   (b)

Figure 7. (a) Plot between shoot through duty ratio(D) Vs Boost factor(B), (b) Plot between Modulation index (M) Vs Voltage gain (B)

8.2 Modulation index Vs Voltage gain

The relationship between modulation index and voltage gain of the qSBI is plotted as shown in Figure 7(b). The expression for the RMS output voltage of three phase qSBI with traditional SBC modulation strategy is given by,

$$V_{rms} = \frac{\sqrt{3}M.B.V_1}{2\sqrt{2}} = \sqrt{3}.M.\frac{V_1}{1 - 2D}.\frac{1}{2\sqrt{2}}$$ (20)

Similarly, the expression for the rms line voltage with improved PWM is given by,

$$V_{rms} = \frac{\sqrt{3}M.B.V_1}{2\sqrt{2}} = \sqrt{3}M.\frac{2}{1 - 3D}.\frac{V_1}{2\sqrt{2}}$$ (21)

With the input of 36V, duty ratio 0.05 and modulation index of 0.95, the rms output voltage of three phase qSBI is obtained as 46.49V wit the improved PWM whereas the traditional PWM technique offers only 23.27V.

9. CONCLUSION

An experimental set up of three phase quasi Switched Boost Inverter topology is developed for 100W power output. It is simulated and validated with experimental results to understand the performance of the topology with an improved PWM control strategy. It is clear that the topology can provide a higher boost factor of 2.22 with lower duty ratio of 0.05 and it offers high quality of output voltage. Also with the improved PWM control technique, the topology offers increased peak ac output voltage at reduced harmonic distortion. The voltage gain of 2.11 is obtained with the input voltage of 36V. The topology can be very well suitable for renewable energy applications. This research work can be further extended with closed loop control techniques.

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