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Optimization of PFC cuk converter parameters design for minimization of THD and voltage ripple

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ABSTRACT

This paper presents the optimization of PFC Cuk converter parameter design for the minimization of THD and voltage ripple. In this study, the PFC Cuk converter is designed to operate in discontinuous conduction mode (DCM) in order to achieve almost unity power factor. The passive components, i.e., inductor and capacitor are designed based on switching frequency and resonant frequency. Nevertheless, the ranges of duty cycle for buck and boost operations are $0<D<0.5$ and $0.5<D<1$, respectively for the output voltage variation of the converter. The principle of the parameters design optimization is based on the balancing energy compensation between the input capacitor and output inductor for minimization of THD current. In addition, the selection of high output capacitance will minimize the output voltage ripple significantly. A 65 W PFC Cuk converter prototype is developed and experimentally tested to confirm the parameters design optimization principle. The experimental results show that the THD current is reduced to 4.5% from 61.3% and the output voltage ripple is reduced to 7 V from 18 V after parameters optimization are realized. Furthermore, it is confirmed that the output voltage ripple frequency is always double of the input line frequency, 50 Hz and the output voltage ripple is always lower than the maximum input voltage ripple.

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1. INTRODUCTION

In recent years, portable electronic equipment has advanced from a power converter and has the advantages of high efficiency, small in size and possess a wide input and output voltage ranges [1]-[3]. On the other hand, the conventional power converter is not able to operate in a wide operation range and at the same time maintaining high efficiency; especially when the step up and step down voltage conversion need to be achieved [4]-[6]. Besides, battery voltage decreases as the battery discharges and lead to various difficulties if there is no voltage control. Therefore, the most effective method of regulating voltage through a circuit is by using a DC/DC converter. Cuk converter can be used as a DC voltage regulator due to the ability of the converter to stepping-up or stepping-down the voltage with negative polarity depending on the application requirement. In addition, the traditional telecommunications equipment requires an input power DC of -48 V [7] and contains numerous parallel-redundant rectifiers which convert the input AC power to output DC power. Besides, the telecommunications networks and information technology equipment has converged causing the power equipment need to have a various input power requirements [8]. Therefore, it is a challenge to telecommunications facilities designer to construct a reliable and economical power converter so that it ableto support various input power requirements [9]-[11].

In order to convert the available input AC source from grid to DC source -48 V, a full-bridge rectifier is required to rectify the input AC to output DC while Cuk converter is a suitable conveter to be used to convert the output positive polarity to negative polarity [12]. The Cuk converter is a modified boost-buck converter and can be used either to step up or step down the output voltage with respect to the duty cycle. The integration of these two converters which are the full-bridge rectifier and the Cuk converter namely the PFC Cuk converter. Nevertheless, the use of bridge rectifier, transformer, inductor, and capacitor can produce the DC output voltage without any distortion however will cause the input current to be extremely distorted. Hence, a rectifier i.e., AC/DC conversion is totally required in PFC converter structures to ensure the input voltage and input current are purely sinusoidal. Several circuit topologies; boost, buck-boost, Cuk, and SEPIC converter have been developed for PFC applications. However, the PFC Cuk converter has several drawbacks i.e., high THD current at the input side as well as high voltage ripple at the output side due to the output voltage from the full-bridge rectifier produced inconstant DC.

This paper presents the optimization of PFC Cuk converter parameters design for the minimization of THD and voltage ripple in order to overcome its drawbacks. Besides, to reduce the THD current at the input side, the principle of balancing energy compensation between the input capacitor, C_1 and output inductor, L_o is concerned. Meanwhile, the output voltage ripple can be reduced by optimizing the output capacitance, C_o. Therefore, the energy from the output full-bridge rectifier must be transferred to the Cuk converter effectively without any "extra" energy. If the energy is not effectively transferred, the input THD current is affected at the input side and increases the output voltage ripple. The parameters are designed based on the standard of IEC 61000-3-2, which is class D i.e., maximum of THD current is 5% [13]-[15]. The PWM signal for the switch is realized using Altera DE2 as in [16], [17]. The results of the optimization produced an output of -48 V with the THD current is down to 4.5% and the maximum output voltage ripple is approximately 20% of the output voltage.

2. CONVENTIONAL PFC CUK CONVERTER

A conventional PFC Cuk is a type of conventional PFC converter with the integration of full-bridge rectifier and Cuk converter that allows the step-up and step-down of output voltage by controlling the duty cycle. Figure 1 shows the full-bridge rectifier part that requires four standard-diode as a bridge, while large input inductance L_1 and large output capacitance C_o are required for the Cuk part. The operation of Cuk is the same as the conventional buck-boost converter with constant DC source, which the output voltage is always in negative polarity.

Generally, the characteristics of the conventional PFC Cuk converter and Cuk converter are different, which the Cuk converter receives a constant DC as the supply while the PFC Cuk converter receives a not constant DC source. Therefore, a large input inductance and ouput capacitance are required for the structure of PFC Cuk converter. Nevertheless, the output voltage can be stepped-up or stepped-down with appropriate components design for both structures. When the same specifications and parameters of the Cuk converter are applied in the conventional PFC Cuk converter, the THD current and output voltage ripple become high. Therefore, the inductance and capacitance of the output inductor and capacitor, respectively are required to be optimized in order to reduce the THD current and output voltage ripple.

2.1. Basic Principle of PFC cuk converter

Theoretically, when a duty cycle approaches unity, the DC gain towards zero [14]. The switching frequency need to be considered for parameters optimization purpose. When the switching frequency increases, the ripple curret on the inductor decreases. Figure 2 shows the DC gain characteristics for the PFC Cuk converter. Besides, the structure as depicted in Figure 1 consists of buck and boost operations where for the buck operation, the duty cycle is less than 0.5 and the duty cycle is greater than 0.5 for the boost operation.

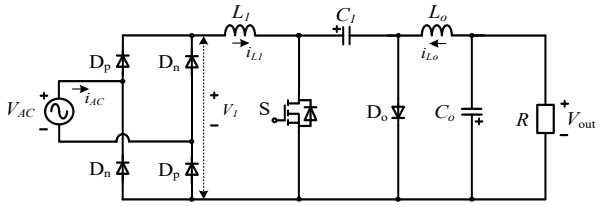


Figure 1. PFC Cuk converter circuit

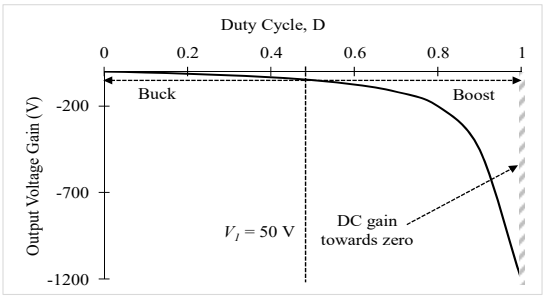


Figure 2. DC gain characteristics for PFC Cuk converter

2.2. Operation of PFC cuk converter

The PFC Cuk converter circuit with single-switch is controlled by duty cycle signal. This circuit can be divided into six operating modes and consist of positive and negative half cycles, referring Figure 1.

Mode-1 and Mode-4: Mode-1 is positive half cycle while mode-4 is negative half cycle. When the switch S is turned-on, the energy from source is stored in inductor L_1. At the same time, capacitor C_1 is discharging to inductor L_o and capacitor C_o. During this interval, the diode D_o is turned-off and the power supplied to the load.

Mode-2 and Mode-5: Mode-2 is positive half cycle where mode-5 is negative half cycle. When the switch S is turned-off, the inductor L_1 recharges the capacitor C_1, and inductor L_o recharges the capacitor C_o through the freewheeling diodes D_o and supplies power to the loads.

Mode-3 and Mode-6: Mode-3 is positive half cycle while mode-6 is negative half cycle. During the same state when the switch S is turned-off, the capacitor C_1 and inductor L_o store energy through the discharging inductors L_1. The capacitor C_o are discharging. During this interval, the diode D_o is turned-off and the power supplied to the loads.

2.3. Parameters design of PFC cuk converter

Table 1 shows the specifications to design the passive elements. Based on the operation mode, the passive elements are estimated based on the DCM condition.

Table 1. Specifications

Parameters	Values
Input Voltage, V_{AC}	(50-100) V
Frequency line, f_L	50 Hz
Period of line voltage, T_L	0.02 s
Output Voltage (DC), V_o	-48 V
Output Power, P_{out}	65 W
Switching Frequency, f_s	50 kHz
Maximum input current ripple, Δi_{L1}	< 25% of fundamental current
Output Voltage ripple, ΔV_o	< 20% of V_o

2.3.1 Design of input inductor

The input inductors L_1 are expressed in (1) with input voltage (V_{AC}) is in positive and negative half cycles.

$$L_1 = \frac{V_{AC}(t) \cdot D}{\Delta I_{L1} \cdot f_s} \quad (1)$$

2.3.2 Design of output inductor

The voltage conversion ratio M in terms of the rectifier parameter can be obtained by applying the power-balance principle [13]:

$$M = \frac{V_o}{\sqrt{2} \cdot V_{AC}} \quad (2)$$

The value of $K_{e\text{-}critical}$ can be evaluated by:

$$K_e < K_{e-critical} = \frac{1}{2(M+2)^2} \tag{3}$$

To ensure the operation is in DCM, the following value of K_e is selected:

$$K_e = 0.85 \times K_{e-critical} \tag{4}$$

Thus, by evaluating the parameter K_e gives an equivalent inductance L_e value of

$$L_e = \frac{K_e \cdot R_L}{2 \cdot f_s} \tag{5}$$

The value of L_o can be expressed as follows:

$$L_o = \frac{2L_1 \cdot L_e}{L_1 - L_e} \tag{6}$$

2.3.3 Design of output inductor

The capacitor C_1 will not cause low-frequency oscillations with the converter inductors. Thus, the energy transfer from capacitors C_1 is determined based on the inductor L_1, and L_o such that the line frequency (f_L) should be lower than the switching frequency (f_s). Thus, a better initial approximation for choosing the resonant frequency (f_r) is given by [5]:

$$f_L < f_r < f_s \tag{7}$$

$$f_r = \frac{1}{2\pi\sqrt{C_1\left(L_1 + L_o\right)}} \tag{8}$$

2.3.4 Selection of output capacitor

The output voltage ripple frequency of the converter is two times of the input frequency. Therefore, C_o can be obtained as follows:

$$C_o = \frac{P_o}{4f_L \cdot V_o \cdot \Delta V_o} \tag{9}$$

2.4. Optimization parameters design of PFC cuk converter

Figure 3 shows the optimization parameters of L_o and C_1 with THD current, however the allowable THD current range must be within 1.8% to 4% in order to estimate L_o and C_1 for optimization purpose. Energies of L_o and C_1 must be compensating each other. Otherwise, the remaining energy of L_o will be transferred to the source and consequently the quality of input current line will be affected. As has been mentioned, the THD current of 2% is used as a reference to ensure the efficiency of the proposed converter is high and THD current is low, according to the standard of IEC 61000-3-2.

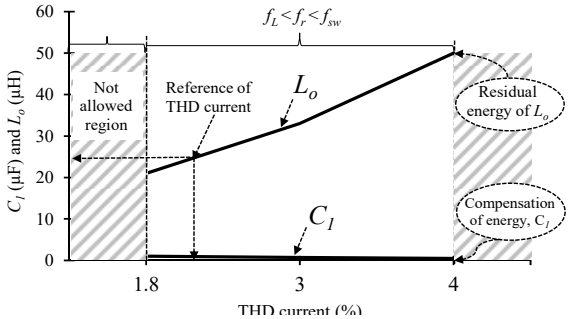


Figure 3. Optimization parameter of L_o and C_1 with THD current

The output capacitor ripple current, Δi_{c1} and capacitor voltage ripple, ΔV_{c1} are expressed by (10) and (11). In addition, the output voltage ripple is expressed by (13).

$$\Delta i_{c1} = \Delta i_L = \frac{V_L}{L_o} DT_s \tag{10}$$

$$\Delta V_{c1} = \frac{1}{C_1} \int i_{c1} dt \tag{11}$$

$$\Delta V_{ESR} = \Delta i_{c1} \cdot ESR \tag{12}$$

$$\Delta V_o = \Delta V_{c1} \cdot \Delta i_{ESR} \tag{13}$$

Based on (9), the output voltage ripple is reduced when capacitance increases. After all the parameters are optimized by considering availability in the market, the PFC Cuk converter specifications are listed as shown in Table 2.

Table 2. Optimization parameter design of passive element

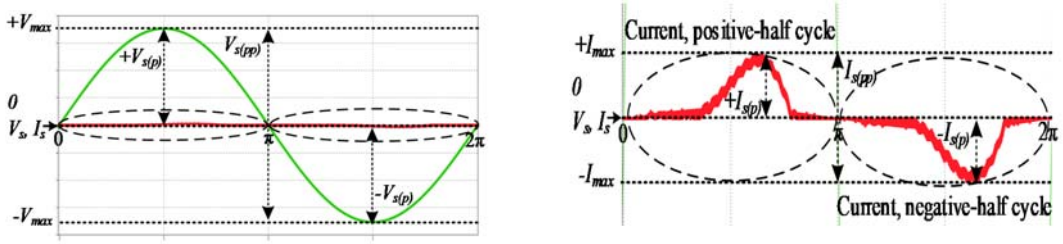
Parameters	values
Input inductor, L_1	2.2 mH
Output Inductor, L_o	22 µH
Input capacitor, C_1	1 µF
Output Capacitor, C_o	3300 µF

3. RESULTS AND ANALYSIS

Referring to the Table 2, the simulation and experimental results are discussed by focusing on the minimization of THD current and output voltage ripple. To reduce the THD current, the inductance of the output inductors are set to 2.2 mH and 22 µH while the capacitance of the output capacitors are set to 470 µF and 3300 µF in order to observe the output voltage ripple reduction with the switching frequencies of 10 kHz and 50 kHz.

3.1. Minimization of THD current

During the simulation of the converter circuit, all the switching devices and components are assumed ideal with no losses. Figure 4(a) and Figure 4(b) show the input source voltage and input source current, respectively for the PFC Cuk converter. The quality of the input current is poor.



(a) (b)

Figure 4. Input source (a) voltage, (b) current

This means that the THD current is very poor in this condition and the percentage of the THD current of the input line current is 61.3%. Figure 5 shows the frequency spectrum of THD current before optimization. In other words, the input line current is not a pure sinusoidal as the input line voltage because the input line current contains single harmonic distortion. The optimized parameter is needed to ensure the harmonic limits is always within the range of IEC 61000-3-2 standards. The parameters for the hardware experiment listed in Tables 1 and 2 are constructed to evaluate the performance of the proposed circuit as

shown in Figure 1. The THD current is measured by using power analyser and all data are tabulated in one graph. In addition, the inductance of the output inductors, L_o used are 2.2 mH and 22 µH with a fixed capacitance of the output capacitor, C_o which is 3300 µF and the switching frequency is 50 kHz to observe the THD current in terms of the ripple current as shown in Figure 6. From Figure 6(a), the THD current of L_o = 2.2 mH is used and the result of the input THD current is high at the input line current with THD_i of 61.3% with peak-peak current is 10 A and peak-peak voltage is 160 V. In Figure 6(b), the L_o = 22 µH is used and produces the THDi of 4.5% with peak-peak current is 7.4 A and peak-peak voltage is 160 V. In addition, the position of the sine wave is in phase. From Figure 6, when large inductance of the output inductor is considered, the THD current is poor and the output voltage ripple frequency is double from the line frequency for one cycle as shown in (14).

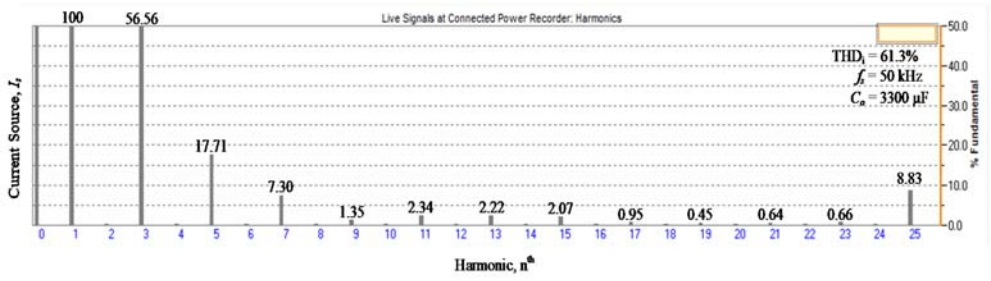
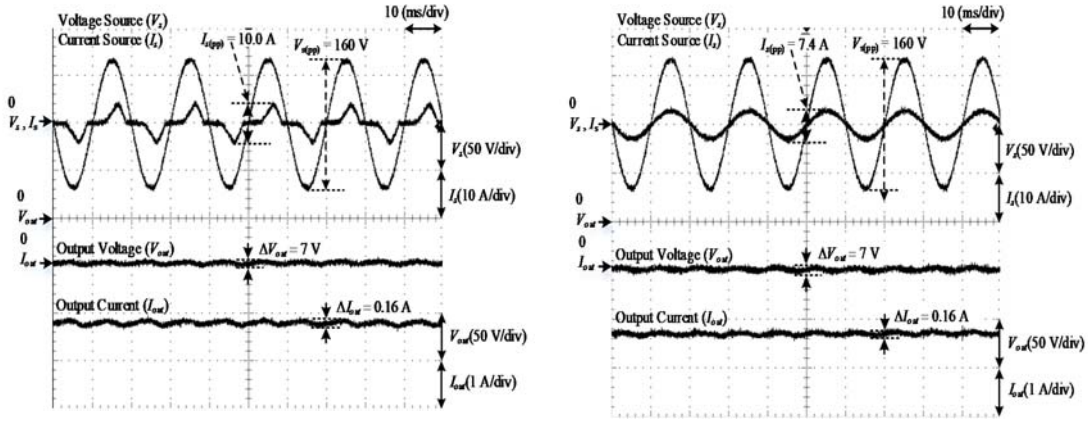


Figure 5. Frequency spectrum of THD_i before parameters optimization



(a) (b)

Figure 6. THD current of output inductance (a) 2.2 mH, (b) 22 µH

The output DC is depending on half-wave and full-wave bridge rectifiers is shown in Figure 7. However, the output voltage ripple is decreased which will be discussed in the next section. Meanwhile, Figure 8 shows the frequency spectrum with various frequencies and output capacitor values. The harmonic components are collected from the fundamental harmonic to 11th harmonics by using power analyser. The switching frequency of 50 kHz and the output capacitance of 470 µF produce the 3rd and 5th highest harmonics which results in a high THD current. However, for the 7th and 9th harmonics component, the current is low compared to the other harmonic components magnitude. It means that to reduce THD current with regard to standards IEC 61000-3-2 which is less than 5%, the 3rd and 5th should be minimized as low as possible. Figure 9 shows the frequency spectrum of THD current after optimization which is 4.5%.

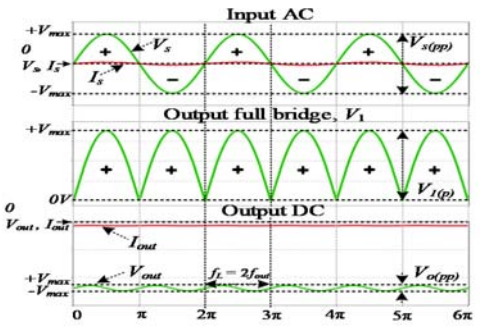


Figure 7. Frequency line and frequency output DC

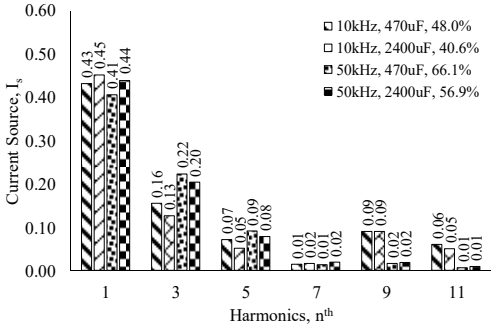


Figure 8. Frequency spectrum with various frequency and output capacitor

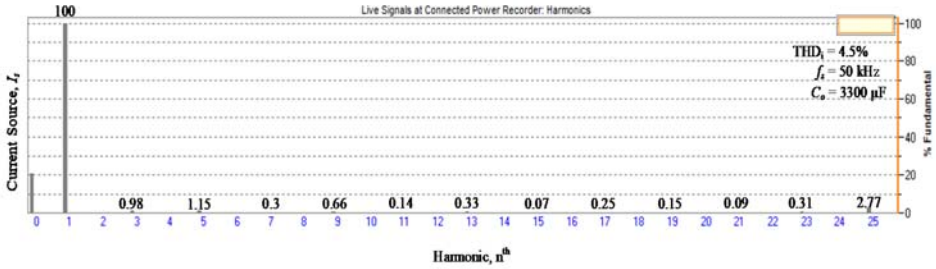
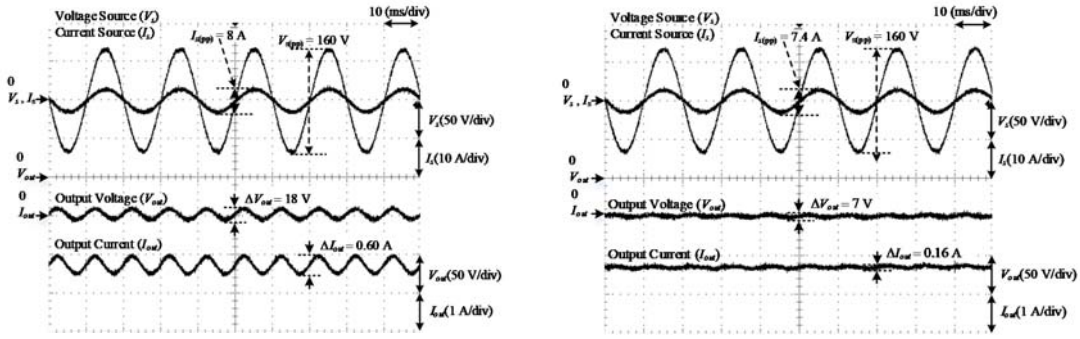


Figure 9. Frequency spectrum of THD_i after parameters optimization

3.1. Minimization of output voltage ripple

Figures 10 shows the comparison of the output voltage and ripple current when the capacitance of the output capacitor used are 470 µF and 3300 µF with a fixed switching frequency of 50 kHz. It can be seen that the output voltage ripple is reduced from 18 V to 7 V when the capacitance of output capacitor is increased. Furthermore, the output current ripple also decreases from 0.60 A to 0.16 A when the capacitance is increased. Besides, the output ripple frequency of the structure is two times of the input frequency.

Figure 10(a) shows the output voltage ripple with the output capacitor of 470 µF. In this case, the output voltage ripple is 18 V and the output current ripple is 0.60 A. It can be seen that the experimental results is approximately agree with the simulation results. The spike of the output voltage waveform is depending on the parasitic elements. When the output capacitance is 3300 µF, the output voltage ripple is reduced to 7 V and output current ripple becomes 0.16 A. This is because when the capacitance is high, the output voltage ripple is reduced. Thus, the function of the capacitor is to reduce the output voltage ripple as shown in Figure 10(b).



(a) (b)

Figure 10. Output voltage ripple with output capacitance (a) 470 µF, (b) 3300 µF

4. CONCLUSION

This paper has presented the optimization of PFC Cuk converter parameters design for the minimization of the THD current ripple and the output voltage ripple. A prototype of the PFC Cuk converter with optimized parameters has been proposed and experimentally confirmed. The experimental results have shown a good agreement with the designed parameters. The THD current is 4.5% after parameters optimization. Satisfaction of IEC 61000-3-2 less than 5% requirement have been achieved by balancing the energy compensation of passive elements. Moreover, the output voltage ripple 7 V is reduced significantly with the output frequency is two times of the line frequency. Other than that, with higher power factor and efficiency, the structure can be used to most of the consumer electronic appliances. This topology uses the combination of full-bridge rectifier and Cuk converter structures with single-switch (MOSFET). A high power factor can be achieved by applying appropriate PWM switching schemes.

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