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Bridgeless PFC single ended primary inductance converter in continuous current mode

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ABSTRACT

This paper presents bridgeless single ended primary inductor (SEPIC) converter operated in continuous conduction mode (CCM). The converter used in the study offers a lesser conduction loss compared to the other bridgeless SEPIC converter. In order to regulate the required output current and output voltage with high efficiency while achieving high power factor correction (PFC) at the input side, average current mode control (ACMC) is applied. The model is simulated using MATLAB/Simulink and it is found that the converter and the proposed control strategy provide a promising result. The preliminary results obtained from the experimental test-rig shows a good agreement as in simulation. The theoretical analysis of the proposed controller is verified on an output 100V to 300W prototype.

1. INTRODUCTION

A nonlinear load such as a battery, electronic device, and generator produce high harmonic distortion to ac input supply. This leads to losses in the supply and low power factor in the electrical system. PFC improves the power factor of electronic circuit. PFC ensure both input voltage and current are in phase, which leads to high power factor and reduces harmonic in supply. Normally, a conventional PFC can be accomplished by using a full bridge diode rectifier and dc-dc converter. Even though bridge rectifier has the ability to produce dc output but its drawback which produce an absolute sinusoidal voltage with high ripple and current that are highly nonsinusoidal [1]. A dc voltage produced by the rectifier is quite large and need to be regulated to a required value. Intended to this reason, a dc to dc converter are used to regulate an actual dc voltage with actual current waveform shape and low output ripple [2]. Moreover, this technique enhanced to PFC with low harmonic distortion [3].

There are various of dc-dc converter topologies used in PFC circuit. SEPIC converter is popular due to its advantages over another dc to dc converter. This converter produces an output voltage that is less or more than the input voltage, but with no polarity reversal [1, 4]. However, SEPIC converter is a 4th order converter since it has 4 storage elements in converter make it seldom uses due to difficulty in design the controller [5]. Nevertheless, this converter offers a surplus advantage compared to 2nd order converter where a lower input current ripple is possible to achieve [5, 6].

Literature studies state that a normal bridge SEPIC converter rectifier produces high conduction loss at input bridge diode hence reduces overall efficiency of the converter. This is due to a bridge rectifier consists of 4 diodes that produce high conduction loss during operation. It is possible to eliminate this high conduction loss with bridgeless converter. The efficiency of these converters is improved by removing the input bridge diode of the conventional bridge SEPIC converter. In the bridgeless converter number of

elements conduct during each cycle are reduce as compare to the bridge rectifier. This significantly reduces losses in the circuit as reported in [7-14]. The Bridgeless SEPIC converter offer reduction of cost, light, increases efficiency at the same time maintaining near unity power factor performance. It is possible for the converter to operate in CCM and discontinuous conduction mode (DCM) depends on its application.

In CCM, the inductor current is always positive while for DCM inductor current is characterized by current returning to zero during every period. DCM causes large voltage stress, consequently gives impact on electromagnetic interference (EMI) into line [5]. Furthermore, at high power application, current stress and voltage stress in DCM become too large which affecting the efficiency of the converter [5, 15]. Hence, DCM normally used for low power application usually less than 200 W while CCM popularly used for medium and high power application [16-18]. This is due to CCM has lower conducted noise, lower conduction losses in the semiconductors and inductor, and lower inductor core loss [8, 18]. Additionally, it has low output voltage ripple. However, the design of CCM controller is more complex as compared to DCM. DCM has properties of self PFC since its capability to give higher power factor by the nature of their topologies [19, 20]. Hence, DCM has simple control and can achieve PFC by using simple control system. CCM required complex control system and required closed loop control to achieve PFC.

Current mode control typically work for converter operate in CCM. Among all current control mode, ACMC offers several advantages such as the ability to sense and control average inductor current while offering immunity to noise [21]. In PFC application, another significant feature of ACMC near the zero crossing of the line voltage, the converter operates with the maximum duty cycle. As a result, the dead angle period which encounter in peak current mode control is greatly reduced [22, 23]. Most of PFC applications has been widely adopte AMMC as a control technique for CCM converters [24, 25].

Bridgeless SEPIC converter in [7-12] focus at low power application operated in DCM using voltage control. This controller design is simple since all zero and pole are located at left hand plane make a tuning process easier. However, this controller provides high current and voltage stress for medium power application which cause some power loss to converter.

In this paper, CCM with ACMC applied to bridgeless SEPIC converter proposed in [9, 10] are studied. This paper is organized as follows. The bridgeless SEPIC converter detail circuit operation with average current controller are discussed in Section 2. The proposed circuit parameter, simulation result and preliminary result of hardware prototype are presents in Section 3. Finally, the conclusion is present in Section 4.

2. RESEARCH METHOD

2.1. Circuit operation

Bridgeless SEPIC converter as proposed in [9, 10] as in Figure 1, are simulated in CCM with an average current mode controller. The circuit consist of three inductors, three capacitors, two diode and two MOSFET apart from a resistor as its load.

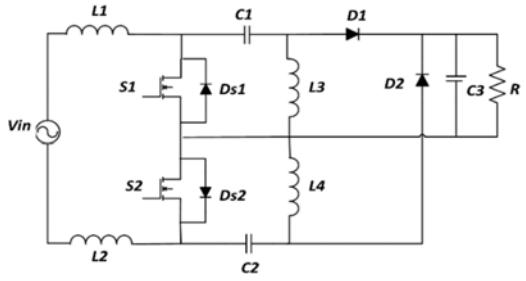

Figure 1. Bridgeless SEPIC circuit

This circuit has the same operation in both cycles, where each switch will only turn on in positive or negative half cycle. During the positive half cycle, only nine elements conduct which is L1, L2, S1, Ds2, C1, L3, D1, C3 and R as shown in Figure2. In negative half cycle L1, L2, S2, Ds1, C2, L3, D2, C3 and R are conduct as shown in Figure 3. This bridgeless SEPIC converter reduced number of component conduction during half cycle. At each half cycle of bridgeless SEPIC converters, it operates as basic dc-dc SEPIC converter.

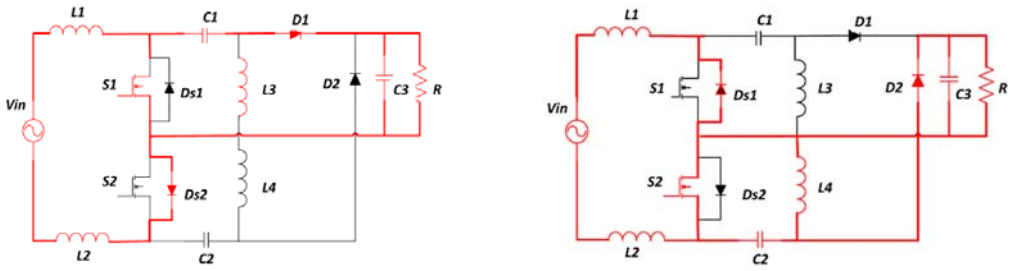

Figure 2. Operation of the bridgeless SEPIC converter in: (a) positive half cycle (b) negative half cycle

Bridgeless SEPIC operate in CCM and it consists of two mode operation per cycle. For positive half cycle it is operated in mode 1 and mode 2 as shown in Figure 3. The waveform of voltage and current operation for bridgeless SEPIC converter are shown in Figure 4.

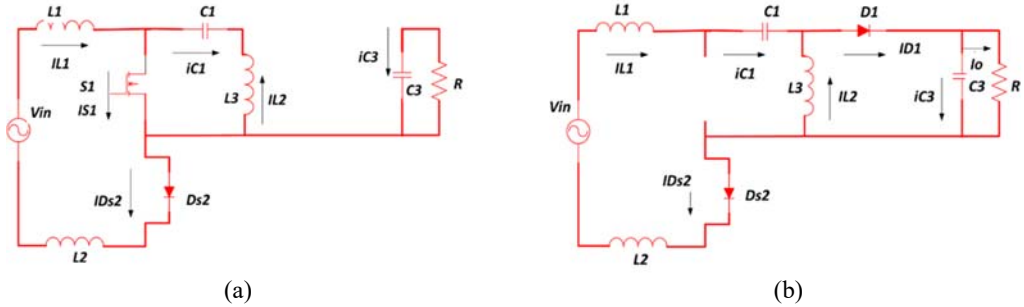

Figure 3. Positive half cycle operation in (a) mode 1 (b) mode 2

In mode 1, S1 and Ds2 are operate, current will flow through S1 and Ds2. L1 and L2 charge and are increase linearly to its peak depends on its duty cycle. In mode 2, S1 will turn off and D1 turn on, which allow current through it. Current across L1 decrease linearly due to discharging process through the C1, C3 and load. Since the circuit operation is symmetrical, the modes of operation for the negative half cycle are not shown here. Symmetrical feature of the converter in CCM is discussed in detail in [9, 10].

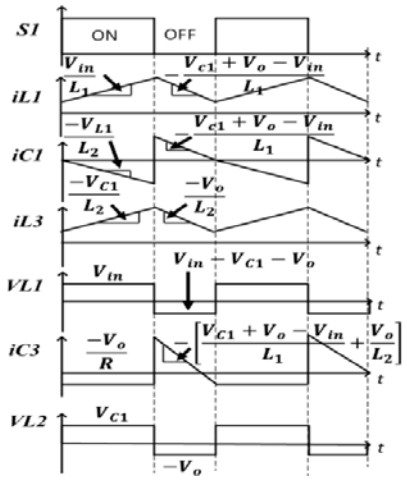

Figure 4. Waveform of current and voltages

In mode 1, S1 and Ds2 are operate, current will flow through S1 and Ds2. L1 and L2 charge and are increase linearly to its peak depends on its duty cycle

The voltage across inductor, L1

$$L_1 \frac{diL_1}{dt} = Vin \quad (1)$$

The voltage across inductor, L2

$$L2 \frac{diL_2}{dt} = V_{C1} \quad (2)$$

The current across series capacitor, C1

$$C_1 \frac{diV_{C1}}{dt} = -i_{L2} \quad (3)$$

The current across output capacitor, C3

$$C_3 \frac{dV_{C3}}{dt} = -\frac{V_o}{R} \quad (4)$$

In mode 2, S1 will turn off and D1 turn on, which allow current through it. Current across L1 decrease linearly due to discharging process through the C1, C3 and load. Since the circuit operation is symmetrical, the modes of operation for the negative half cycle are similar as in positive cycle but in opposite direction.

The voltage across inductor, L1

$$L_1 \frac{diL_1}{dt} = V_{in} - V_{C1} - V_o \quad (5)$$

The voltage across inductor, L2

$$L_2 \frac{diL_2}{dt} = -V_{C3} \quad (6)$$

The current across series capacitor, C1

$$C_1 \frac{dV_{C1}}{dt} = i_{L1} \quad (7)$$

The current across output capacitor, C3

$$C_3 \frac{dV_{C3}}{dt} = i_{L1} + i_{L2} - \frac{V_o}{R} \quad (8)$$

2.2. Mathematical model

In order to design the controller, it is mandatory to obtain the transfer function based on mathematical model to simplified controller tuning. Based on mode of operation of bridgeless SEPIC converter in CCM, the state space averaging modelling technique [25-27], are applied based on KCL and KVL of circuit during turn ON and turn OFF state as in equation (1-8).

Steady state dc model:

$$0 = AX + BU \quad (9)$$

$$Y = CX$$

AC small signal model:

$$\check{x} = A\tilde{x} + B\tilde{u} + B_d\tilde{d} \quad (10)$$

$$\hat{y} = C\tilde{x}$$

$\tilde{x}$ - Vector of state variable
$\hat{y}$ - Vector of output system(I_{L1}, V_o)
A -State vector ($\widetilde{iL_1}, \widetilde{iL_2}, \widetilde{C_1}, \widetilde{V_O}$)
B - Input matrix
C - Matrix which connect output to the state variable
$\tilde{u}$ - Input variable (V_{in})
$B_d.\tilde{d}$- Duty ratio variation for CCM [27]

The average matrices for steady state and liner small signal state space equation of bridgeless SEPIC converter based on (9) and (10) obtain as bellow:

$$\frac{d}{dt}\begin{bmatrix}\widetilde{iL_1}\\ \widetilde{iL_2}\\ \widetilde{C_1}\\ \widetilde{V_O}\end{bmatrix} = A.\begin{bmatrix}\widetilde{iL_1}\\ \widetilde{iL_2}\\ \widetilde{C_1}\\ \widetilde{V_O}\end{bmatrix} + B.\tilde{d} + B_d.V_{in} \quad (11)$$

$$\frac{d}{dt}\begin{bmatrix}\widetilde{iL_1}\\ V_O\end{bmatrix} = C.\begin{bmatrix}\widetilde{iL_1}\\ \widetilde{iL_2}\\ \widetilde{C_1}\\ \widetilde{V_O}\end{bmatrix} \quad (12)$$

Where:

$$\mathbf{A}=\begin{bmatrix}\mathbf{0} & \mathbf{0} & -\frac{\mathbf{1-D}}{\boldsymbol{L_1}} & -\frac{\mathbf{1-D}}{\boldsymbol{L_1}}\\ \mathbf{0} & \mathbf{0} & \frac{\boldsymbol{D}}{\boldsymbol{L_2}} & -\frac{\mathbf{1-D}}{\boldsymbol{L_2}}\\ \frac{\mathbf{1-D}}{\boldsymbol{C_1}} & \frac{\boldsymbol{D}}{\boldsymbol{C_1}} & \mathbf{0} & \mathbf{0}\\ \frac{\mathbf{1-D}}{\boldsymbol{C_3}} & \frac{\mathbf{1-D}}{\boldsymbol{C_3}} & \mathbf{0} & -\frac{\mathbf{1}}{\boldsymbol{RC_3}}\end{bmatrix}, \mathbf{B}=\begin{bmatrix}\frac{\boldsymbol{V_O}}{\boldsymbol{L_1 D}}\\ \frac{\boldsymbol{V_O}}{\boldsymbol{L_2 D}}\\ -\frac{\boldsymbol{V_O}}{\boldsymbol{RC_3(1-D)}}\\ -\frac{\boldsymbol{V_O}}{\boldsymbol{RC_3(1-D}}\end{bmatrix}, B_d=\begin{bmatrix}\frac{\mathbf{1}}{\boldsymbol{L_1}}\\ \mathbf{0}\\ \mathbf{0}\\ \mathbf{0}\end{bmatrix}, \mathbf{C}=\begin{bmatrix}\mathbf{1} & \mathbf{0} & \mathbf{0} & \mathbf{0}\\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{1}\end{bmatrix}$$

(11) and (12) consists of the ac perturbation. By using Laplace transformation in (11) and (12), yield a form of transfer function of bridgeless SEPIC converter.

$$Y(s) = \begin{bmatrix}I_{L1}(s)\\ V_o(s)\end{bmatrix} = C(sI_4 - A)^{-1}B_d.D(s) + C(sI_4 - A)^{-1}.BV_{in} \quad (13)$$

Where $\boldsymbol{I_4}$ is a unity matrix, based on expansion and solving of equation 13, the transfer function of inner loop and outer loop are:-

$$G_{id} = \frac{I_{L1}(s)}{D(s)} = \frac{aa(s^3+a_1s^2+a_2s+a_3)}{s^4+b_1s^3+b_2s^2+b_3s+b_4)} \quad (14)$$

$$G_{vi} = \frac{V_o(s)}{I_{L1}(s)} = \frac{-ab(s^3-a_4s^2+a_5s-a_6)}{s^3+a_1s^2+a_2s+a_3} \quad (15)$$

With:

$$a_1 = \frac{1}{RC_2}\left[D\left(\frac{1+C_3}{C_1}\right)+1\right], a_2 = \frac{D}{L_2C_1}\left[1+\left(\frac{L_2}{C_3R^2}\right)\right], a_3 = 2D[RL_1C_3C_1], a_4 = (1-D)^2\frac{R}{L_1D}\left[1+\frac{L_1}{L_2}\right], a_5 = \frac{D}{L_2C_1}$$

$$a_6 = \frac{R(1-D)^2}{DL_1L_2C_1}, b_1 = \frac{1}{RC_2}, b_2 = \frac{1}{L_1C_1}\left[\left(\frac{L_1}{L_2}D^2\left(\frac{C_1}{C_3}\right)(1-D)^2\right) + \left((1-D)^2\frac{C_1}{C_3}\right)\right], b_4 = \frac{(1-D)^2}{L_1L_2C_1C_3}$$

$$aa = \frac{v_O}{L_1D}, ab = -\frac{L_1D}{RC_3(1-D)}$$

2.3. Control method

Average current mode control is employed to control the bridgeless SEPIC converter operated in CCM. In [9, 10] the converter is operated in DCM using voltage control and suitable to be used at lower power application. The proposed controller for the converter mainly focus on medium power application is illustrated in Figure 5. Average current mode controller consists of two loops (cascade). Inner loop is for current controller while outer loop is for voltage controller.

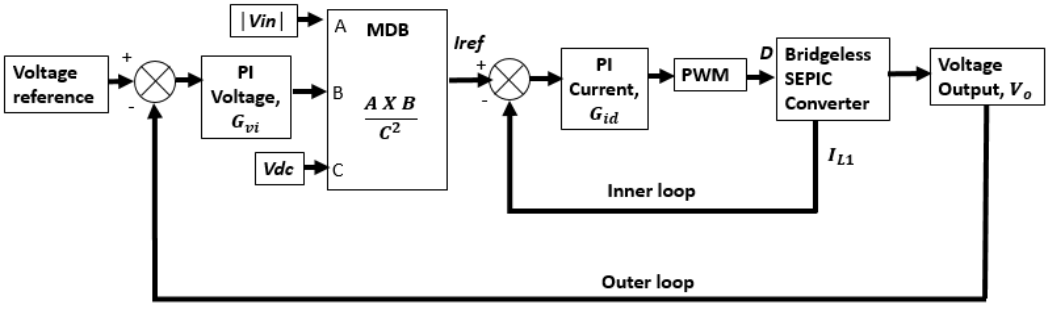

Figure 5. Average current mode control for bridgeless SEPIC using PID controller

In outer loop, the reference and actual output voltage of converter are compared, and the error is fed to generate the inductor current reference for inner loop. Outer loop also regulate voltage and to maintain it preferred set point. Meanwhile for inner loop the main purposed is to ensure the wave shaping inductor current with lead to improve input power factor. In inner loop, the actual inductor current is compared with the reference current produced by outer voltage. Any changes in inductor current, the current loop compensator will alter the duty ratio to ensure the output voltage remains as its desired value [28]. Output from inner loop is compared with saw tooth carrier to generated fixed frequency pulse width modulation (PWM) signal.

Since the converter operates in CCM, multiplication and dividing signal (MDB) are used to obtain the reference current input. It is an easy way to obtain high power factor by using this method since the reference current waveform is proportional to the input voltage waveform based on multiplier technique [24, 29]. MDB consist of multiplier and dividing of voltage input rectified, $\left|\text{Vin}\right|$, PI voltage error and average component of input rectified voltage, Vdc.

The controller is design using SISO tool in MATLAB/Simulink to obtain desired PI controller for inner and outer loop. By using transfer function as in section 2.2, the inner loop bandwidth is designed to be one decade lower from switching frequency to ensure high stability of control signal. Since that converter switching frequency is 25 kHz, then the inner loop is design to be 2.5 kHz. Outer loop bandwidth is set to be 20 Hz. The controller is design to have a low voltage ripple and fast dynamic response.

3. RESULTS AND ANALYSIS

3.1. Design parameter

The proposed circuit is design based on the parameter as in table 1. All parameter are designs based on [30, 31] to achieve CCM operation of the bridgeless SEPIC converter. Simulation work using MATLAB/Simulink on the proposed converter is being done based on the controller and design parameter.

Table 1: Design Parameter of the Circuit

Parameters	Values
Line Frequency, f_l	50 Hz
Switching Frequency, f_s	25 kHz
Input Voltage, V_{in}	120 Vrms
Input inductor, L_1, L_2	25.5 mH
Intermediate inductor, L_3 & L_4	12.3 mH
Intermediate Capacitor, C_1&C_2	2 uF
Output Capacitor, C_3	480 0uF

Output Resistor, R	34 Ω
Output Voltage, V_o	100V dc
Power Output,P_o	300 W

3.2. Simulation result

Figure 6 shows the input current and input voltage of proposed converter. Both input current and input voltage are in phase and power factor of the converter is 0.98. This signify that the proposed converter work perfectly as PFC. Figure 7, the input current operates in CCM. It successfully achieves theory of CCM by using the proposed average current mode control. The output voltage shown in Figure 8 achieve the target with 5% voltage ripple. The current output of proposed converter is shown in Figure 9 with 5% current ripple. The average output power of the bridgeless SEPIC converter successfully achieves 300 W as anticipate.

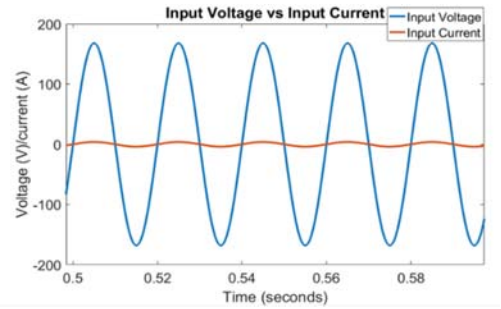

Figure 6. Input voltage and input current

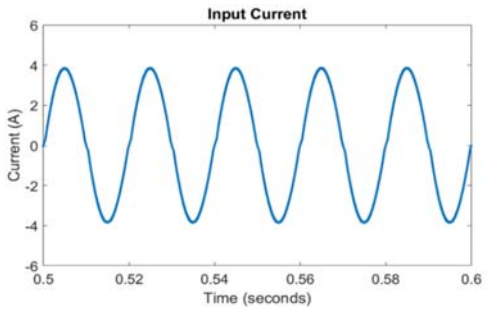

Figure 7. Input current (*iL1*)

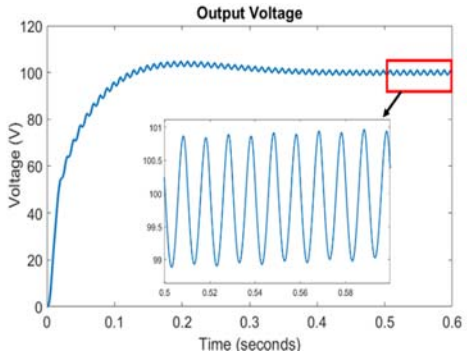

Figure 8. Output voltage

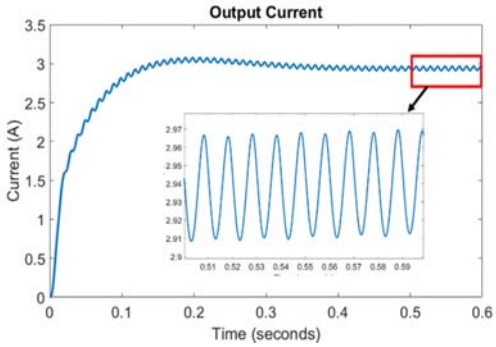

Figure 9. Output current

3.3. Preliminary hardware result

Based on simulation, the prototype of bridgeless SEPIC converter have been implement to verify the operation of converter in CCM. DS1104 digital signal processing and control engineering (dSPACE) controller board and basys3 field programmable gate array (FPGA) are used as controller interface to perform ACMC. dSPACE Controldesk control and sense the input voltage, input current and output voltage as proposed. However, dSPACE restricted on lower sampling time with make the accuracy and precision of prototype defer from simulation. By combining dSPACE and FPGA 35us sampling time are achieved. The preliminary result for input current, input voltage, output current and output voltage are shown in Figure 10.

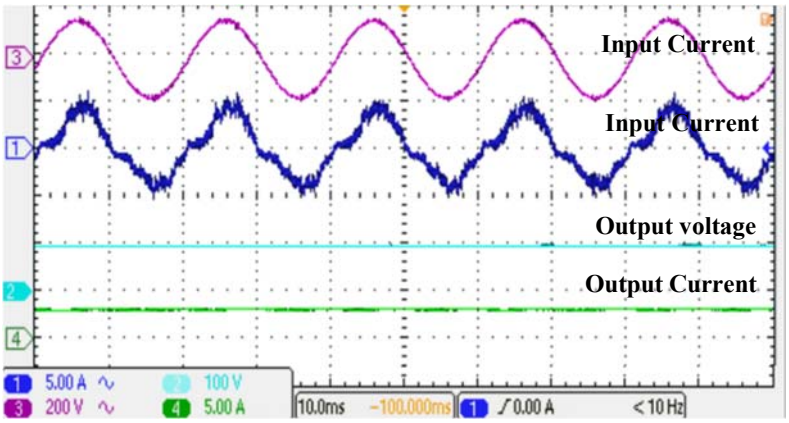

Figure 10. Input voltage, Input current, Output voltage and Output current

The experiment result shows that, the input current and input voltage are in phase and its shape are nearly sinusoidal as simulation result. The output current and voltage ripple is about 5% same as simulation but slightly have some loss in the hardware test. More detail analysis of the waveform and efficiency performance of the bridgeless SEPIC converter will be discussed in future work.

4. CONCLUSION

In this paper, an average current mode controller for asingle phase PFC bridgeless SEPIC converter operated in CCM is proposed and verifed through simulation studies in MATLAB/Simulink. It is shown that the controller is successfully achieved unity power factor for a medium power application (300 W). A prototype of converter is built to verify the performance of theoretical design. Based on the preliminary result, the input current and voltage show a good agreement with 0.92 power factor while at the output side, a smooth dc current and dc voltage with approximately 5% ripple are obtained.

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