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Multilevel inverter with MPWM-LFT switching strategy for voltage THD minimization

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ABSTRACT

This paper presents a proposed modified pulse width modulation – low frequency triangular (MPWM-LFT) switching strategy for minimization of voltage THD with implementation of asymmetric multilevel inverter (AMLI) topology on the reduced number of switching devices (RNSD) circuit structure. Principally, MPWM-LFT able to produce optimum angle of the output voltage level in order to minimize total harmonic distortion (THD). In this study, 5-level reduced number of switching devices circuit structure is selected as a circuit configuration for asymmetric (7-level structure) multilevel inverter. For switching strategy, MPWM used low switching frequency in producing signal and needs higher output voltage levels to achieve low total harmonic distortion. In contrast, sinusoidal pulse width modulation used high switching frequency in order to minimize total harmonic distortion. By optimizing angle at the output voltage using MPWM-LFT switching strategy, the voltage THD is lower as compared to MPWM and SPWM switching strategies. MPWM-LFT switching strategy obtains 11.6% of voltage THD for the 7-level asymmetric topology as compared to MPWM and SPWM switching strategies with the voltage THD are 21.5% and 17.5% respectively from the experimental works

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1. INTRODUCTION

Generally, power inverters are one of converter that converting direct current (DC) to alternating current (AC) for any systems that required this type of power conversion [1]. Multilevel inverters (MLI) have become a selection for uses in electric utility and for medium to high power industrial applications. In a recent number of years, the industry has begun to request greater power equipment, which now reaches the megawatt level and start to grow even further. For these causes, MLI have been developed as the key for working with higher voltage levels. Generally, MLI consists of an array of power semiconductors and direct current (DC) voltage sources, then the output voltages with stepped waveforms will be generated. MLI consists of three main different topologies, i.e., neutral point clamp multilevel inverter (NPCMLI), flying capacitor multilevel inverter (FCMLI) and cascaded H-bridge multilevel inverter (CHBMLI) [2]. Specifically, multilevel inverter has the advantages of generating better output quality by consideration number of level and modulation technique used [3].

Basically, the primary objective in creating multilevel inverters is to maintain a low harmonic distortion (THD) at output side by considering less numbers of semiconductor devices [4, 5]. Several improvements had been done in order to produce high efficiency converter. For example, several researchers are focusing on reducing semiconductor devices by rearranging the circuit configuration [6, 7]. Several topologies had been introduced in order to reduce the number of semiconductor devices [8, 9] such as

symmetric multilevel inverter (SMLI) and asymmetric multilevel inverter (AMLI) which improve conventional multilevel inverter structures. The obvious difference between symmetric and asymmetric is the DC sources. Whereby, in symmetric topology all DC sources voltage are same, meanwhile in asymmetric topology each DC source voltage is different [10].

Harmonics is one of the issues [11, 12] considered because it may cause overheating, increasing of voltage stress in the passive components and maloperation in the electronic devices. In short, it can lead to the reduction of the equipment's lifespan. Therefore, some standards must be complied with, such as the IEEE Std 519-1992 [13]. According to IEEE Std 519-1992, harmonic voltage on power system of 69 kV and below must be limited to 5% THD with each maximum individual harmonic is 3%, while IEC standard [13, 14] shows the THD that limits to 8% for low voltage application. In multilevel inverter, input voltage and current are chopped based on the switching signal which generates the desired output waveforms. The output voltage and current have harmonics at the switching frequency, which can be reduced by using passive filters. Basically, the switching frequency and passive filters have a significant role in reducing the harmonics. By decreasing the switching frequency until 50 Hz, the harmonics can be reduced and the quality of the output voltage can be improved as well. In addition, the filter size and switching loss are reduced.

This paper presents the proposed MPWM-LFT switching strategy for minimization of voltage THD with implementation of AMLI topology on the RNSD circuit structure. MPWM-LFT switching strategy able to enhance the minimization of the voltage THD by optimizing the angle at the output voltage in open-loop system as compared to MPWM and SPWM switching strategies. In addition, it also able to reduce the switching loss and increased the efficiency of the converter. Therefore, it shows that the MPWM-LFT switching strategy is the best switching strategy for open-loop system in order to get the lower voltage THD and reduced the switching loss as well.

2. VOLTAGE THD MINIMIZATION BY MPWM-LFT AND ASYMMETRIC TOPOLOGY WITH RNSD CIRCUIT STRUCTURE

2.1. Principle of asymmetric topology

The common advantage of asymmetric topology is that it is able to generate a high level of output voltage by using the same structure of symmetric topology [15, 16]; as an example, asymmetric topology with different DC voltages, i.e., Vdc1 = Vdc, Vdc2 = 2Vdc, Vdc3 = 4Vdc, Vdc4 = 8Vdc as compared to the DC source voltage of symmetric topology, i.e., Vdc1=Vdc2=Vdc3. Asymmetric topology has different values of DC source voltage and the modulation technique is complex and the level can be upgraded up to two levels higher. Figure 1 shows the circuit structure that has been selected for AMLI. Based on the selected circuit structure, it is able to produce five levels of output voltages. By applying the asymmetric principle in this structure, it is able to produce up to 7 level of output voltages. Therefore, the number of switching devices and semiconductor losses are reduced.

2.2. RNSD circuit configuration

The selected circuit structure is the RNSD structure [17], which is the improvement of the cascaded H-bridge structure. Basically, the structure is divided into two parts, which are S1 and S2 as part 1 and SA, SB, SC and SD are part 2 or also known as H-bridge. Part 1 acts as the main part for producing the level and part 2 operates for the positive and negative of the output voltage. This selected structure can produce five levels of output voltage when it follows the cascaded and symmetric principles. But the selected structure can also operate in producing seven levels of output voltage when the binary method of asymmetric topology is implemented. Figure 1 shows the proposed structure for a 5-level symmetric and 7-level asymmetric MLI. Comparing the number of switching devices of cascaded structure with the selected structure, the 5-level cascaded structure contains eight units of switches while the proposed RNSD circuit structure using symmetric topology only requires six unit of switches and produces the same level as the cascaded circuit structure. For a 7-level cascaded circuit structure, 12 units of switches are needed for the structure while only six switches are required for the proposed RNSD circuit structure using the binary method of asymmetric topology and produces the same level of output voltage as the cascaded circuit structure.

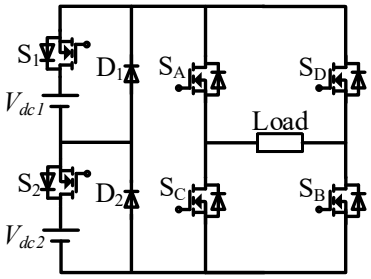

Figure 1. Reduced number of switching devices circuit structure

2.3. Optimum angle at the output voltage level

Voltage THD can be minimized by increasing the level of output voltage and using SPWM switching strategy. Other than that, with optimum angle at the output voltage level, the voltage THD is minimized and is better than the SPWM switching strategy [18]. The most common method to determine the optimum angle at the output voltage is using selective harmonic elimination (SHE), where it needs a close-loop system [19] and is more complicated [20, 21]. Therefore, the optimal angle at the output voltage level for the minimization of voltage THD using the MPWM switching strategy can be determined by improvements of MPWM and SPWM switching strategies. From the principle of improved switching strategy based on MPWM and SPWM switching strategies, the angle at the output voltage level or known as alpha angle can be generated and applied in order to get lower voltage THD than the SPWM switching strategy. It is easier and less complicated to use MPWM switching strategy as compared to the SPWM switching strategy. The switching control for the hardware setup is easier using MPWM switching strategy as compared to SPWM switching strategy and reduces the cost [22]. Figure 2 shows the example of the angle at the output voltage level for a 7-level MLI using MPWM switching strategy. The width, *W* for each staircase must differ in order to produce lower voltage THD than the SPWM switching strategy.

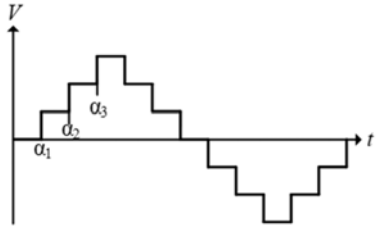

Figure 2. Example of angle at the output voltage level for voltage THD minimization

2.4. Voltage thd minimization by proposing modified pulse width modulation with low frequency of triangular wave (MPWM-LFT)

Basically, the principle of the proposed modified pulse width modulation with low frequency of triangular wave (MPWM-LFT) switching strategy is the same with the principle of the SPWM switching strategy [23] where it compares the triangular wave with the sine wave. The difference is the switching frequency that is applied in the triangular wave is 50 Hz and shifted 90º as shown in Figure 3, which is different with the typical SPWM switching strategy that usually uses more than 1 kHz. However, the modulation signal generated from the 50 Hz of triangular wave is the same with the MPWM principle. The signal can be applied for the multilevel inverter structure in order to get the optimum point of the angle at the output voltage level. One of the advantages of using low switching frequency is that it reduces the switching losses compared to SPWM switching strategy, which uses a high switching frequency[24]. Theoretically, the switching losses for this technique will be the same as the MPWM switching strategy. Figure 3 shows the modulating method for the 7-level asymmetric multilevel inverter. By using this modulation signal, the output voltage levels generated are automatically at the optimum angle at the output voltage level and observed by the percentage of voltage THD.

It has been proved by the simulation and experiment that the voltage THD obtained by this method is lower than the SPWM and MPWM switching strategies. The waveform of the staircase output voltage is the nearest to the sine waveform. So, it is proved that the voltage THD is the lowest among the other switching strategies. The angle at the output voltage level can be determined by using simultaneous equation:

$$\alpha = \frac{360^{o}}{0.02} \times t_{level} \quad (1)$$

Where t_{level} is the time of the exchange level, i.e., time from level one to level two. The α is the angle at the output voltage level. The simulation results for the modulation signal that compares the triangular wave with the sine wave is shown in Figure.4 which is in MPWM switching strategy form. Therefore, it shows that the theory and principle of this method have been modified from SPWM switching strategy principle. The modulation signals in Figure 4 need to be rearranged same as the switching sequence of MPWM switching strategy that follow the mode of operation of the RNSD structures. Figure 5 shows the simulation result for the 7-level asymmetric topology with the proposed MPWM-LFT switching strategy. It is proved that using the principle of SPWM switching strategy can generate the MPWM-LFT switching strategy. The result also includes the sine wave as the reference in order to observe that the staircase can be easily filtered and form a sine wave. It is also proved that the output voltage is the nearest form to sine wave compared to the MPWM and SPWM switching strategies.

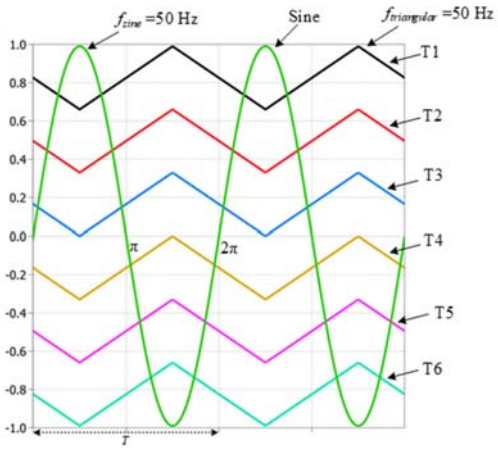

Figure 3. Method of modulation

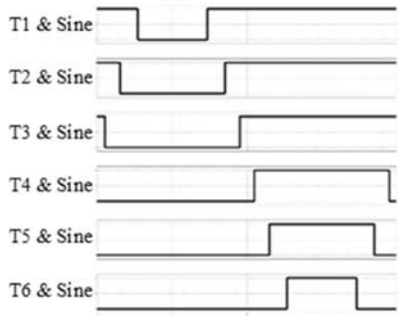

Figure 4. Modulation signals

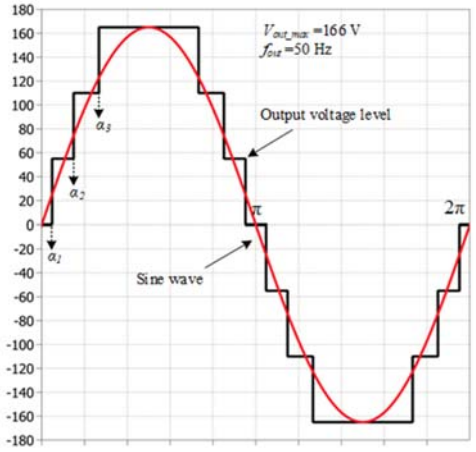

Figure 5. Simulation results of output voltage using the proposed MPWM-LFT switching strategy

3. RESULTS AND ANALYSES

Total harmonic distortion (THD) of the output voltage is an important parameter that is observed either in the principle, simulation or hardware. Several factors affect the voltage THD, such as in a multilevel inverter, increasing the number of output voltage level generated and using the correct switching strategy can produce a lower voltage THD than the conventional MLI [7]. Therefore, the implementation of asymmetric topology is able to increase the level of the output voltage and maintains the structure in order to reduce the THD of the output voltage. Another factor that can reduce the voltage THD is the suitability of the switching strategy applied. This study focuses on three types of switching strategies, which are the MPWM, SPWM and MPWM-LFT switching strategies. Theoretically, SPWM switching strategy can produce much lower voltage THD [25] as compared to MPWM switching strategy. But, by optimizing the angle at the output voltage level using MPWM-LFT switching strategy, the voltage THD is lower than SPWM switching strategy.

Figure 6 shows the result of the experiment for the 7-level asymmetric topology using the MPWM switching strategy while Figure 8 shows the result of the experiment for the 7-level asymmetric topology using the SPWM switching strategy. The number of the output level is the same for all results and it shows that the selected structure operates well even in experiment and proves that asymmetric topology can be implemented. The voltage THD of the output voltage using MPWM and SPWM switching strategies are 21.5% and 17.5% respectively as shown in Figure 7 and Figure 9. it can be said that, the voltage THD is minimized when SPWM switching strategy is applied in the RNSD circuit structure with the same number of output voltage level.

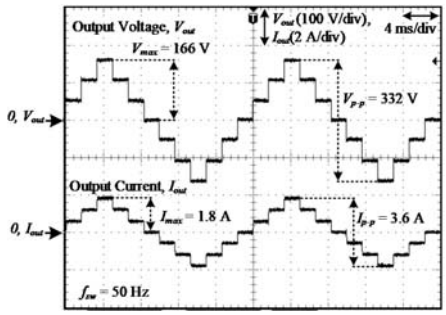

Figure 6. Output voltage level of experimental results using MPWM switching strategy

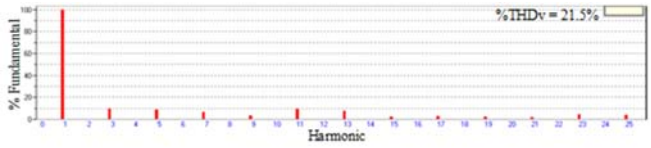

Figure 7. Frequency spectrum of output voltage using MPWM switching strategy

The second comparison is between the MPWM switching strategy and the proposed MPWM-LFT switching strategy based on the experimental results. Figure 6 and Figure 10 show the waveforms difference between MPWM switching strategy and the MPWM-LFT switching strategy. The width of each staircase is not the same for the MPWM-LFT switching strategy due to the optimum angle at the output voltage level generated where triangular wave is overlapping with the reference wave, which is the sine wave. Some of the pulses in the MPWM-LFT are wider and some are smaller than the common MPWM switching strategy. Hence, the THD at the output voltage is reduced and is better than in the SPWM switching strategy. It is also proved that in the open-loop system, minimum voltage THD can be achieved by calculation and estimation of angle at the output voltage level. In addition, finding the optimum angle at the output voltage level is able to minimize the voltage THD better than the SPWM switching strategy which is well known as the common modulation technique for the multilevel inverter. Basically, the staircase of the MPWM-LFT switching strategy is different from the maximum voltage to zero. The width from the maximum voltage towards zero slightly changes depending on the optimum angle at the output voltage level for minimum voltage THD. The voltage THD of the output voltage using SPWM and MPWM-LFT switching strategies are 17.5% and 11.6%

respectively as shown in Figure 9 and Figure 11. it can be said that, the voltage THD is minimized when MPWM-LFT switching strategy is applied in the RNSD circuit structure with the same number of output voltage level.

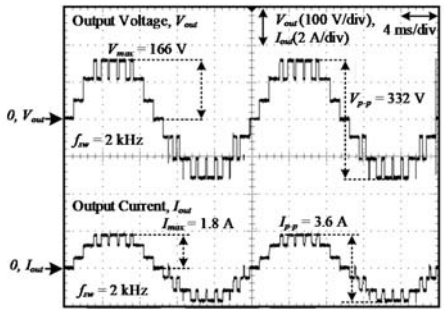

Figure 8. Output voltage level of experimental results using MPWM switching strategy

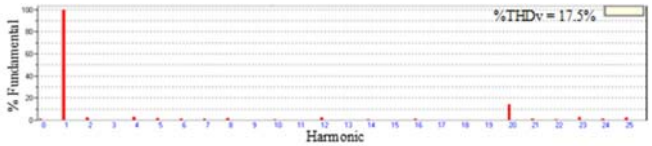

Figure 9. Frequency spectrum of output voltage using SPWM switching strategy

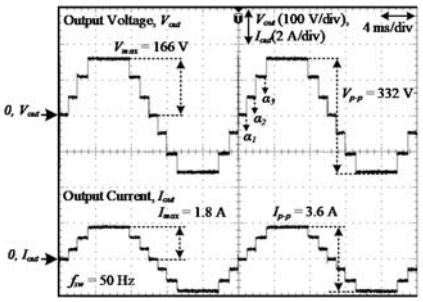

Figure 10. Output voltage level of experimental results using MPWM-LFT switching strategy

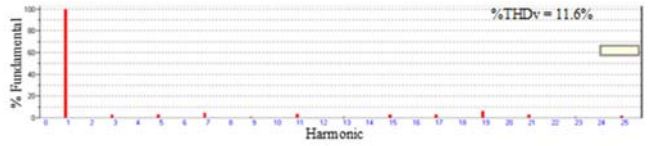

Figure 11. Frequency spectrum of output voltage using MPWM-LFT switching strategy

Conceptually, by increasing the number of output voltage level, the volume and size of filter are reduced significantly due to the minimization of voltage THD. Therefore, it can be concluded that by optimizing angle at the output voltage level using MPWM-LFT switching strategy able to minimize the voltage THD at the output voltage better than MPWM and SPWM switching strategies. In addition, the switching loss reduction using the proposed MPWM-LFT switching strategy is significant as compared to typical SPWM switching strategy.

4. CONCLUSION

Basically, by comparing the MPWM and SPWM switching strategies, SPWM switching strategy shows a better voltage THD quality as compared to MPWM switching strategy for the multilevel inverter. In this paper, a switching strategy is proposed to improve the minimization of the voltage THD. The proposed MPWM-LFT is by improving the principle of SPWM by applying 50 Hz switching frequency at the triangular wave and phase-shifted 90^o. By comparing with sine wave and triangular 50 Hz, the signal generated will be in MPWM form and also with optimum angle at the output voltage level. This switching strategy obtains 11.6% of voltage THD for the 7-level asymmetric topology as compared to MPWM and SPWM switching strategies with the voltage THD are 21.5% and 17.5% respectively. It can be concluded that the THD at the output voltage level can be reduced by determining the optimum angle at the output voltage level using MPWM-LFT switching strategy. Three switching strategies have been applied and MPWM-LFT shows the lowest voltage THD that been obtaion at the output voltage. Therefore, it can be concluded that MPWM-LFT switching strategy shows better results by achieving low voltage THD as compared to SPWM switching strategy and low switching frequency is applied in order to achieve a lower THD at the output voltage level.

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