International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 11, No. 1, March 2020, pp. 169~177
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v11.i1.pp169-177

Implementation of the conventional seven-level single-phase symmetrical cascaded H-Bridge MLI based on PSIM

Hassan Salman Hamad
Technical Electrical Department, Technical Instructors Training Institute, Middle Technical University, Iraq

Article Info

Article history:

Received Jun 18, 2019
Revised Jul 8, 2019
Accepted Aug 8, 2019

Keywords:

Cascaded H-bridge inverter
PSIM
MLI
THD

ABSTRACT

Researchers have found interest in the multilevel inverters (MLI) owing to the low total harmonic distortion (THD) associated with their output voltage, as well as their low electromagnetic interference (EMI). The MLI represents an effective and feasible solution for enhancing power demand and minimizing AC waveforms' harmonics as they generate a preferred level of output voltage as inputs from varying levels of DC voltages. In this paper, the performance of a seven-level cascaded H-bridge MLI with an asymmetrical number of power switches was evaluated. The simulation performance is shown to validate the operating principle of the single-phase cascaded H-bridge inverter. To control the MLI, a pulse width modulation approach was utilized. The operating principle of the MLI was verified via simulation using PSIM software.

This is an open access article under the CC BY-SA license.

Corresponding Author:

Hassan S. Hamad,
Technical Electrical Department,
Middle Technical University,
Muasker Al Rashid Street, 7F7P+JG Baghdad, Baghdad, Al Zafranyia, Iraq.
Email: hassan111hamad@gmail.com

1. INTRODUCTION

The generation of electricity from renewable sources has attracted much attention recently. In this regard, solar energy from photovoltaic (PV) systems have received the most attention from researchers due to their numerous benefits like no fuel costs, no emission, no noises, and requiring little care. Solar PV panels are among the rapidly increasing source of energy globally, especially in grid-connected applications (about 80% of the global market in 20108 were reserved for grid-connected applications) [1].

The recent years witnessed tremendous growth in the global renewable energy demand. As such, solar power has contributed significantly to clean energy generation, thereby playing a major role in meeting the global electricity demand. However, the major issue in this regard is the optimal incorporation of PV energy resources into the prevailing power distribution network. Consequently, more studies have been dedicated recently to grid-tied PV power conversion systems. The major aim of these converters is to improve on the power fed to the power grid through suitable tracking of the PVs' maximum power point (MPP); this is achievable by minimizing losses as well as harmonic distortion (HD) whereas ensuring high consistency [2].

Much interest has been focused on MLI due to their numerous advantages, such as low switching device stress, low output total harmonic distortion (THD), and minimal switching stress [3]. The interest in renewable energy sources, especially solar energy, is elicited by the impending exhaustion of fossil fuel reserves and the associated environmental problems from the conventional power generation techniques. Within the last 25 years, the demand for solar-sourced energy has intensified by 20%–25% per annum,

especially in the grid-connected applications [4, 5]. The market increase in grid-connected PV systems have consequently increased interest in grid-connected PV systems. Based on diverse arrangements of the PV system, the 5-inverter groups can be well-defined as string inverters, multi-string inverters, AC-module inverters, central inverters, and cascaded inverters.

Regarding the MLI, three basic structures have been presented: "diode-clamped multilevel inverter," "flying capacitor multilevel inverter," and "cascaded multilevel inverter" [6]. The cascaded MLI has numerous single-phase H-bridge inverters besides it categorized depend on the DC voltage level of the sources into symmetric and asymmetric groups. The symmetric group has H-bridges with equal DC voltage source magnitude while the reverse is the case for the asymmetric group.

These structures are advantageous because of their low range of DC voltage sources that considers the most significant parameter when determining an inverters' cost. Contrarily, some of them require a several insulated gate bipolar transistors due to the involvement of several bidirectional power switches and this is a major drawback of such topologies. A study by [7] has presented an asymmetric topology whose main challenge is associated to their switches of bidirectional power. These switches made the cost higher and the number of inverters IGBTs is increased.

Power conversion is emerging as a solution for both high and medium voltage transformerless systems; multilevel converters are represented as a boundary for grid-connected PV systems. A configuration of the (CHB) specifically embodies a vital solution towards the connection of each H-bridge cell to a specified DC source [8, 9]. This circuit topology has the ensuing advantages: (i) an adaptable modular structure suited for different power and voltage levels, thereby permitting the sharing of voltage boosting between H-bridge cells; (ii) an expandable multilevel waveform which can be extended to several voltage steps based on the number of cells used. The increased number of voltage levels equally lower the THD; it also better-quality output currents and voltages compared to the traditional converters [10, 11]. Consequently, the output filter demands are weaker to ensure agreement with the standards for grid harmonics [12]. The CHB circuit topology also allows separate control of each DC links' voltage to ensure an improved MPPT quality which maximizes PV power extraction and enhances the efficiency of the system [13, 14].

This paper projected a new cascaded MLI topology for increasing the number of output voltage levels and reducing the number of driver circuits, power switches, and the overall inverter cost. It should be observed that the proposed topology utilized unidirectional power switches and has been compared to other topologies from different perspectives, including the number of IGBTs, DC voltage sources, differences in the values of the DC voltage sources, as well as blocking voltage value for each switch. Lastly, the proposed topology was evaluated for performance in generating all voltage levels through a 7-level inverter. The performance was verified through simulation using a PSIM software.

This work presents the operation of a single-phase circuit configuration without a transformer or a DC-DC boost stage. The major drawback is the necessity to have a higher total DC link voltage compared to the peak value of the grid voltage so as to feed active power from the PV panels into the power grid. Another problem is the need to adopt an adequate multilevel modulation technique.

2. DESCRIPTION OF THE PROPOSED 7-LEVEL INVERTER SYSTEM

Figure 1 depicts the degrees of the sources of DC voltage of the projected seven-level inverter which are determined thus [15]:

$$V_1 = V_{dc} \quad (1)$$

$$V_2 = 2V_{dc} \quad (2)$$

focusing on (1), (2), and Table I, the projected topology can produce 0, ±Vdc, ±2Vdc, and ±3Vdc at the output.

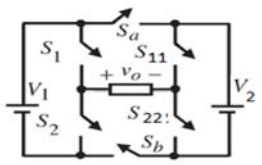


Figure 1. Topology of the cascaded H-bridge MLI for PV systems

Table 1. Output voltages of the proposed seven-level inverters

No.	S_1	S_2	S_{11}	S_{22}	S_a	S_b	v_o
1	1	0	0	1	0	1	V1
2	1	0	0	1	1	0	V2
3	1	0	1	0	0	1	V1-V2
4	1	0	1	0	1	0	0
5	0	1	1	0	1	0	-V1
6	0	1	1	0	0	1	- V2
7	0	1	0	1	1	0	-(V1-V2)

The configuration of the cascaded MLI is made up of n H-bridge converters which are serially connected as depicted in Figure 2. A short string of PV panels feeds each DC link rather than a DC supply [16, 17]. The 4 switches in each H-bridge can be combined in different ways to generate the following three output voltage levels: $-V_C$, 0, or $+V_c$. A cascaded MLI with n input sources can offer 2n+1 level to generate the AC output waveform. With this (2n+1)-level voltage waveform, the harmonics in the generated current is reduced, thereby minimizing the output filters.

The cascaded MLI, as shown in Figure 2 is connected to the grid using an L filter to ensure a reduction in the switching harmonics [18]. A local load is also parallel connected. The delivery of the PV power to the grid is dependent on the conditions of the system operation.

The CHB multilevel converter is usually made up of a number of serially connected N H-bridge cells. This circuit topology is important for either string or module fed to the grid. The illustration of a single phase 2N+1 levels CHB inverter of PV AC module fed to the grid is depicted in Figure 2 [19]. Each of the PV generators is directly connected to an H bridge inverter whose outputs (v_{Hi}) are serially connected to the grid to generate the expected AC output waveform. Each H bridge can generate three voltage levels as presented in Table I based on the diverse modes of the switching devices.

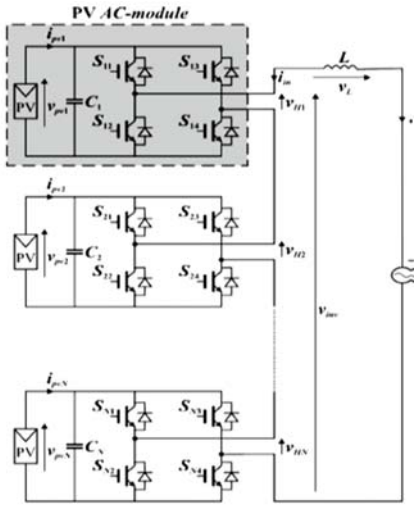


Figure 2. The topology of the grid-connected system

3. CH-B MODULATION STRATEGY

The modulation strategy proposed in this study is a combination of the staircase and unipolar PWM where each CHB converters' cell can be in any of the following 4 states presented in Table II. The cell is bypassed in the first state, but inserted in the second and third stages such that its output voltage is $+v_{pvi}$, and $-v_{pvi}$ respectively [20, 21].

The technique proposed in this study is basically based on the partitioning of the grid voltage into different *N* regions. Note that the lowest number of cells required to create the multilevel waveform must at least be equivalent to the adjoining integer, but more than the *v̂grid / vpv_min,* instead, the operation can be considered in the modulation linear region with the intent of defining each cells' minimum DC link voltage appropriate for this purpose.

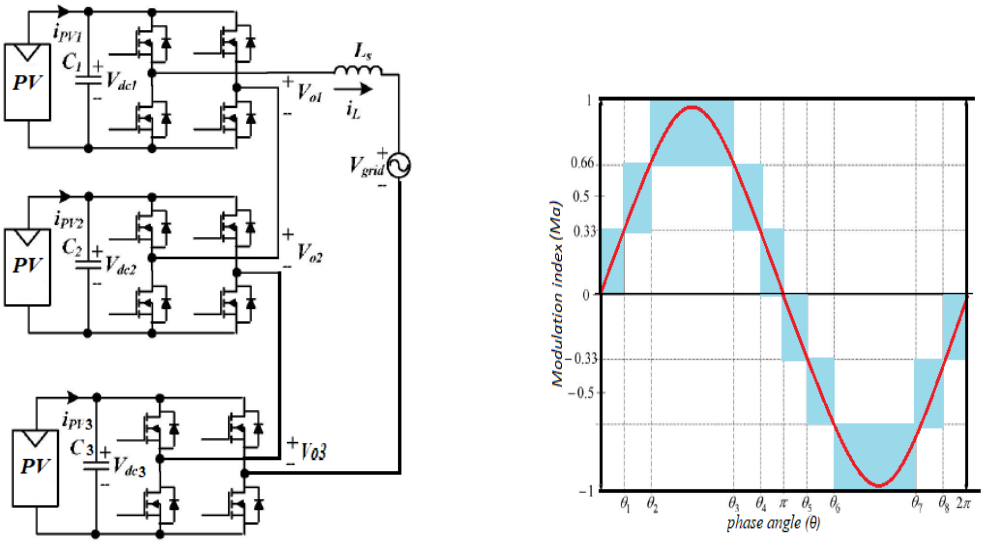
3.1. Basic principles of operation

The CMI is a series of conventional 2-level bridges with serially connected AC terminals to generate the output waveforms. The power circuit for the proposed seven-level inverter with 3 cascaded cells is depicted in Figure 3(a). Several independent DC sources are needed in the CMC and they can be sourced from the from batteries, solar cells or fuel cells [22]. Each converter level can produce 3 different voltage output (+VdC, 0, -Vd) through the combination of the 4 switches of each cell in different manners. The sum of all the inverter outputs gives the AC output. The number of output- phase voltage levels is defined as n = 2N+1, where N represents the number of DC sources. For example, in Figure 3 (a), the output range ranges from -2Vd to +2Vd with 5 levels. The projected inverter functioned through 6 modes for each fundamental frequency cycle. Figure 3(b) depicts the per unit output-voltage signal per cycle while the 6 modes are described thus:

Mode 1 : $0 < \omega t < \theta 1$ and $\theta 4 < \omega t < \pi$;
Mode 2 : $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$;
Mode 3 : $\theta 2 < \omega t < \theta 3$;
Mode 4 : $\pi < \omega t < \theta 5$ and $\theta 8 < \omega t < 2\pi$;
Mode 5: $\theta 5 < \omega t < \theta 6$ and $\theta 7 < \omega t < \theta 8$;
Mode 6: $\theta 6 < \omega t < \theta 7$.

3.2. Control scheme (CS)

The CS for the control of a single H-bridge inverter is based on the classical scheme. From Figure 4, DC input voltage is the source of DC power devices; the multilevel inverter (7-level) changes the DC voltage to AC voltage while the gating signal control system generates the pulse that controls the switching pattern of the H-bridge MOSFET switches [23, 24].



(a) (b)

Figure 3. 7-level output voltage (V_{ab}) Cascaded MLI with (a) separate DC sources, (b) and switching angles

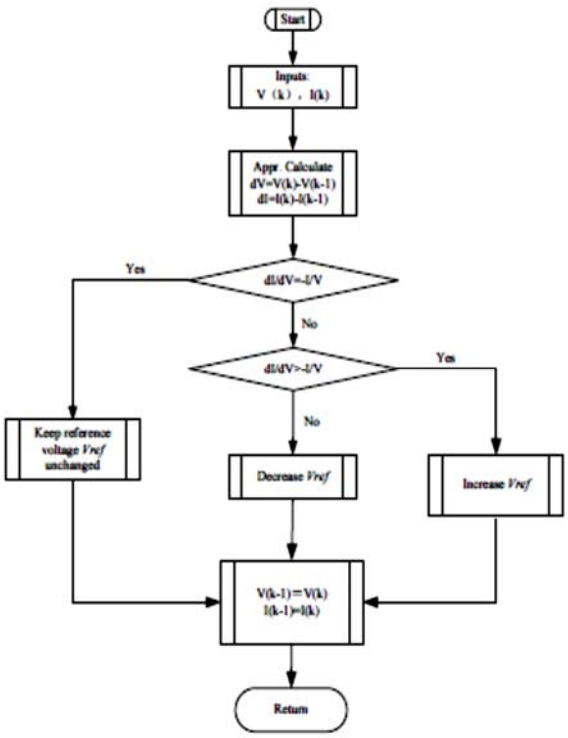


Figure 4. Multi-user Distributed Massive MIMO transceiver model system

The PI controller is used in the CS of the projected cascade H-bridge MLI. This PI controller is popular owing to its simple framework and ease of use for industrial control applications. Figure 5 shows the control circuit of the projected system while the governing for the control action law of a PI controller is represented [25, 26].

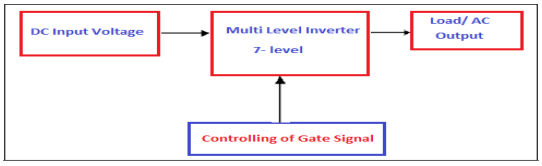


Figure 5. The control circuit of the PI controller

4. DESIGN SIMULATION, ANALYSIS & RESULTS

This section illustrated the simulation of the cascaded H-Bridge MLI circuit using PSIM. The associated figures illustrated for all levels the simulated output voltage, trigger switching pulses, THD, and current analysis, as well as the output voltage with equal step waveform for the proposed technique. PSIM is among the currently available and fast system-level simulators, meaning that the hypotheses can be tested easily and early to ensure a rapid transition from design to implementation. The PSIM can simulate complex power converter and control systems within a short period. The PSIM was used to validate the working principle of the single-phase CHB-MLI as depicted in Figure 6. The complete list of the simulation parameters for the suggested single-phase CHB-MLI is presented in Table II. At first, we set $V_{dc1} = V_{dc2} =$ 100 V to evaluate the attributes of the suggested inverter. Figure 6 demonstrates the outcome of the simulation process for the CHB-MLI upon balancing 2 modules. The DC-link voltage of the 2 MLI modules is balanced by controlling the shoot-through duty cycle. The output phase voltage, as depicted in Figure 6, is 220 Vrms with seven-levels. Figure (7-a & b) show the output current and voltage, while Figure 8 explain the 12 PWM signal for IGBT. Figure (9-a & b) represent the THD for the output voltage signal. The THD of the

phase voltage is 2.80 %. The peak DC-link voltage of the two MLI modules is equivalent to the voltage of the capacitor (200 V). The 7 -level switching of the CHB MLI is illustrated in Table 2.

Table 2. 7 -Level CHB MLI switching

Time	Positive Half Cycle			Negative Half Cycle		
Output	V1	V1+V2	V1+V2+V3	V1	V1+V2	V1+V2+V3
Bridge A Sa 1	1	1	1	1	1	1
Sa 4	1	1	1	1	1	1
Bridge B Sb 1	0	1	1	0	1	1
Sb 4	1	1	1	1	1	1
Bridge C Sc 1	0	0	1	0	0	1
Sc 4	1	1	1	1	1	1
Bridge D Sd 1	0	0	0	0	0	0
Sd 4	1	1	1	1	1	1
Inversion Sp1	1	1	1	0	0	0
Bridge Sp2	0	0	0	1	1	1
Sp3	0	0	0	1	1	1
Sp4	1	1	1	0	0	0

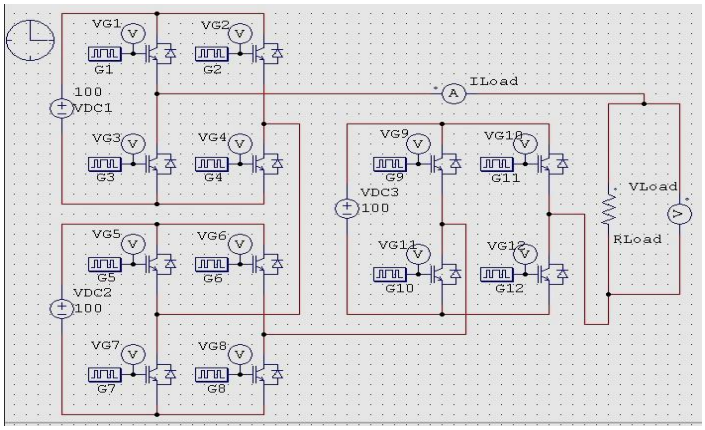


Figure 6. Simulation outcomes of the projected single-phase CHB under the same voltage condition source, $V_{dc1} = V_{dc2} = 100$ V.

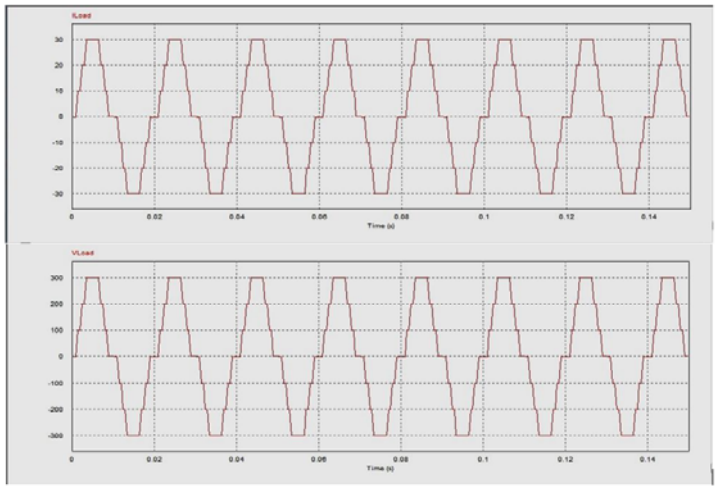


Figure 7. Current output phase (a), Voltage output phase (b)

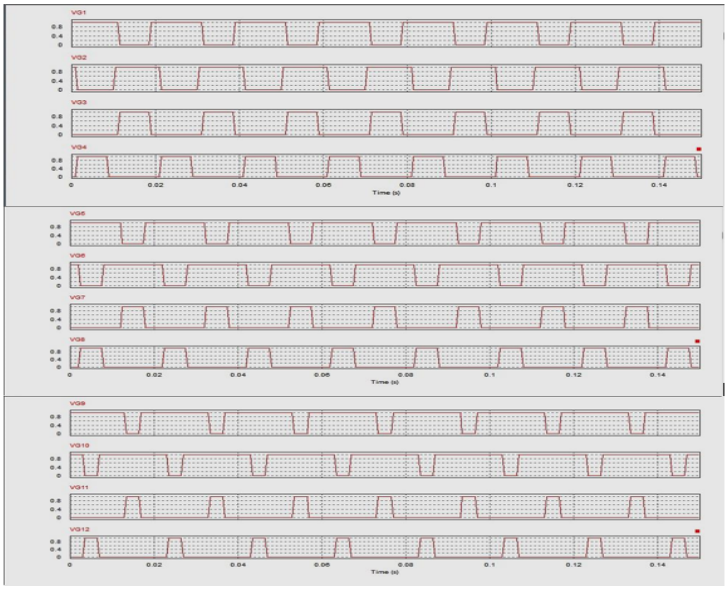


Figure 8. Triggering pulses for seven levels symmetric CHB MLI.

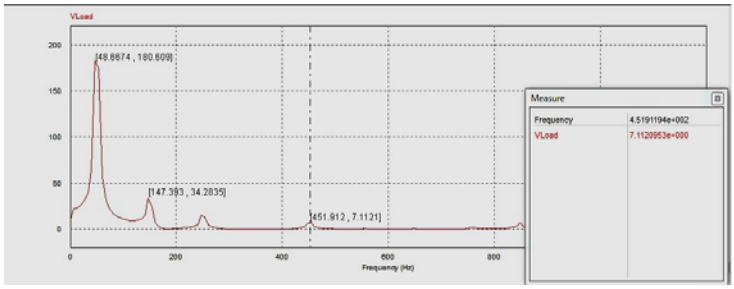


Figure 9. (a) Analysis of FFT CH-Bridge MLI

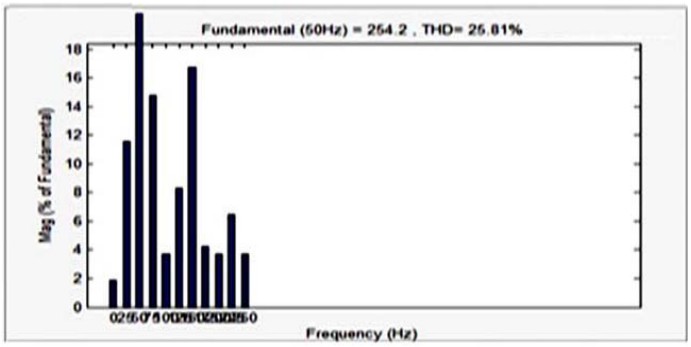


Figure 9. (b) Analysis of FFT CH-Bridge MLI

PSIM simulation has been demonstrated as a CH-bridge topology of MLIs with emphasis on 7-levels. Efforts on this topology have been detailed in this article with emphasis on the main parameters like the generated gating pulses of PWM, the THD, the switching power devices used, and the current and voltage stresses.

5. CONCLUSION

The single-phase cascaded H-bridge inverter was discussed in this paper with respect to its operating principles and performance analysis. This structure of the multilevel inverter and its fundamental principles were analyzed. Furthermore, the basic topology for MLIs was proposed for the generation of 7-voltage levels at the output. Any number of output levels can be developed from the basic topologies. The MLIs guarantees lower THD and enhanced output waveforms. Meanwhile, the suggested topology consists of a higher number of varying DC voltage sources compared to the others. The proposed topology was evaluated in terms of performance accuracy using PSIM simulation. The PWM was used for controlling the H-bridge cascaded MLI to advance the performance in terms of reducing the THD. Since the AC output voltage of the inverter is higher than the source DC input voltage, the proposed topology is suitable for photovoltaic, FACTS and UPS applications.

REFERENCES

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl*., vol. 41, No. 5, pp. 1292-1306, Sep/Oct 2005.

[2] M. K. Nguyen and T. T. Tran, "Quasi cascaded H-bridge five-level boost inverter," *IEEE Trans. Ind. Election*., vol. 64, No. 11, pp. 8525-8533, Nov. 2017.

[3] Ali A. Abdulrazzaq and Adnan H. Ali, "Performance Investigation of Grid Connected Photovoltaic System Modelling Based on MATLAB Simulation," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 8, No. 6, pp. 4847-4854, 2018.

[4] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular Cascaded H-Bridge Multilevel PV Inverter with Distributed MPPT for Grid-Connected Applications," *in IEEE Transactions on Industry Applications*, vol. 51, No. 2, pp. 1722-1731, Mar-Apr 2015.

[5] Ali A. Abdulrazzaq and Adnan H. Ali, "Efficiency Performances of Two MPPT Algorithms for PV System with Different Solar Panels Irradiances," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, No. 4, pp. 1755-1764, Dec 2018.

[6] Ali, A.H and Abdul-Wahid, S.N, "Analysis of self-homodyne and delayed self-heterodyne detections for tunable laser source linewidth measurements," *IOSR J. Eng*, vol. 2, no. 10, pp. 1-6, 2012.

[7] S. Mekhilef and M. N. Kadir, "Voltage control of three-stage hybrid multilevel inverter using vector transformation," *IEEE Trans. Power Electron*., vol. 25, No. 10, pp. 2599-2606, Oct 2010.

[8] Mohannad J. Mnati, Adnan H. Ali, Dimitar V. Bozalakov, Shahad Al-yousif, and Alex Van den Bossche, "Design and Implementation of a Gate Driver Circuit for Three-Phase Grid Tide Photovoltaic Inverter Application," *7th International Conference on Renewable Energy Research and Applications (ICRERA)*, 14-17 Oct, Paris, 2018.

[9] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid- Connected Photovoltaic Systems," *in IEEE Transactions on Industrial Electronics*, vol. 56(11), pp. 4399-4406, Nov 2009.

[10] Hussein A M and Adnan H A, "Effect of some security mechanisms on the Qos VoIP application using OPNET", *International Journal of Current Engineering and Technology*, vol. 3, No. 5, 2013.

[11] M. Coppola, F. Di Napoli, P. Guerriero, D. Iannuzzi, S. Daliento and A. Del Pizzo, "*An FPGA-Based Advanced Control Strategy of a Grid-Tied PV CHB Inverter," in IEEE Transactions on Power Electronics*, vol. 31, No. 1, pp. 806-816, Jan 2016.

[12] Adnan H. Ali, *Simultaneous measurements for tunable laser source linewidth with homodyne detection,* Computer and Information Science, 2011.

[13] G. Grandi, C. Rossi, D. Ostojic and D. Casadei, "A New Multilevel Conversion Structure for Grid-Connected PV Applications," *in IEEE Transactions on Industrial Electronics*, vol. 56, No. 11, pp. 4416-4426, Nov 2009.

[14] MJ Mnati, A Hasan, AH Ali, and DV Bozalakov, "Design and Implementation A Smart Monitoring and Controlling System of Three-Phase Photovoltaic Inverter Based on LoRa," *IOP Conference Series: Materials Science and Engineering 518, (2nd International Conference on Sustainable Engineering Techniques 2019)*.

[15] Adnan H. Ali and Ali A. Abdulrazzaq," Evaluating the performance and efficiency of MPPT algorithm for PV systems," *International Journal of Engineering & Technology*, vol. 7, No. 4, pp. 2122-2126, 2018.

[16] Ahmed J. Abid, Fawzi M. Al-Naima, and Adnan H. Ali, "Comprehensive Modeling of Photovoltaic Array based on Proteus Software," *International Journal of Applied Engineering Research*, vol. 13, No. 6, pp. 4440-4447, 2018.

[17] Ihsan J. Hasan, Nahla A.Salih, and Nadhir I. Abdulkhaleq, "Three-phase photovoltaic grid inverter system design based on PIC24FJ256GB110 for distributed generation," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, No. 3, pp. 1215-1222, Sep 2019.

[18] Adnan H. Ali and Farhood, A.D. "Design and Performance Analysis of the WDM Schemes for Radio over Fiber System with Different Fiber Propagation Losses," *Fibers,* vol. 7, No. 3, 2019.

[19] AJ Abid and AH Ali, "Smart monitoring of the consumption of home electrical energy," *International Journal of Computer Trends and* Technology, vol. 47, No. 2, pp. 142-148, 2017.

[20] Hussain M. Bassi, "A Modulation Scheme for Floating Source Multilevel Inverter Topology with Increased Number of Output Levels," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 6, No 5, pp. 1985-1993, Oct 2016.

[21] Adnan H. Ali, Ali N. Abbas, and M. H. Hassan,"Performance Evaluation of IEEE802.11g WLANs Using OPNET Modeler," *(AJER)*, vol. 02, No 12, pp-09-15, 2013.
[22] Tila Muhammad, Adnan U. Khan2, Hanif Jan, M. Yasir Usman, Junaid Javed, and Arsalan Aslam, "Cascaded Symmetric Multilevel Inverter with Reduced Number of Controlled Switches," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 8, No. 2, pp. 795-803, June 2017.
[23] Thiyagarajan V and Somasundaram P, "A New Seven Level Symmetrical Inverter with Reduced Switch Count," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, No. 2, pp. 921-925, Jun 2018.
[24] M. M. Kareem, M. Ismail, N. Arsad, M. F. Mansor, and Adnan. H. Ali, "Grid Based Clustering Technique in Wireless Sensor Network using Hierarchical Routing Protocol," *in 2018 IEEE 4th International Symposium on Telecommunication Technologies (ISTT)*, pp. 1-5, 2018.
[25] Adnan H. Ali, Hassan S. Hamad, Ali A. Abdulrazzaq, "An adaptable different-levels cascaded h-bridge inverter analysis for PV grid-connected systems," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, No. 2, pp. 831-841, Jun 2019.
[26] K. Ramani, M.A. Sathik, and S Sivakumar, "A New Symmetric Multilevel Inverter Topology Using Single and Double Source Sub-Multilevel Inverters," *Journal of Power Electronics*, vol. 15, No. 1, pp.96-105, 2015.