

## Design a nine-level modular multilevel converter for DC railway electrification system

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### ABSTRACT

A recuperating converter is highly demanded in traction power substation to deliver the braking energy generated by a traction vehicle. Conventional voltage source inverter had been implemented in the traction power station. However, large AC line filters must be installed to improve the quality of AC voltages and currents. This paper proposes to install a nine-level Modular Multilevel Converter (MMC) as a recuperating converter. The main aim is to eliminate the need of AC line filters while producing good quality of AC voltage and current waveforms. The MMC is designed and modelled using MATLAB/Simulink Simulation tool. A centralized control of balancing all the sub-module capacitor voltage level is proposed with Third Harmonic Voltage Injection Level Shifted Pulse Width Modulation (THVI-LSPWM) technique. The simulation results prove that with the application of MMC, good quality of ac voltages and currents are being produced. The Total Harmonic Distortion indexes are found less than 3.5 % without using any AC line filters in the system. In addition, the classic DC link capacitance has also being eliminated.

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## 1. INTRODUCTION

Electric trains draw massive power from the utility grid to accelerate from standstill. They are then worked as generators upon reaching next passenger station. It is predicted that approximately 50% of the regenerative braking energy can be reproduced [1-3]. The regenerative energy had been stored using onboard or wayside energy storage system [4-7]. These systems are fully equipped with different energy sotrage modules, such as batteries, fuel cell, flywheels, and ultracapacitors.

Alternatively, the regenerative energy can be transmitted back to the power grid without using energy storage elements [8-10]. Figure 1 (a) illustrates one of the recuperative converter system proposed in [8]. Although a conventional Voltage Source Inverter (VSI) is capable to deliver the energy back to the power grid, an installation of AC filters is a must. These filters are used to suppress undesired harmonics components. In order to eliminate the AC filters, this paper proposes to replace the conventional VSI with a Modular Multilevel Converter (MMC) as shown in Figure 1 (b).

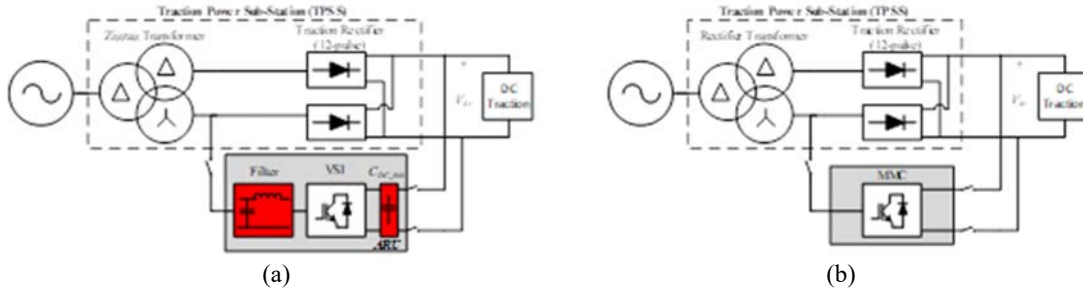


Figure 1. (a) Reciprocating converter system proposed in [8], (b) Proposed recuperating converter system using modular multilevel converter (MMC)

## 2. MODULAR MULTILEVEL CONVERTER

Modular Multilevel Converter had been widely used in High Voltage Direct Current (HVDC) transmission and medium voltage drives applications [11, 12]. The modular structure of the MMC offers high scalability to reach higher range of powers and voltages. In addition, some bulky and costly components in the power conversion system such as transformer, dc-link capacitance and passive filters can be eliminated. Lately, application of MMC had been extended to railway electrification system [13]. MMC has been integrated in AC railway electrification system as Static Frequency Converter (SFC) or Railway Power Conditioner (RPC) [14, 15]. This paper will present the application of MMC as a recuperating converter in DC railway electrification system. The following section will briefly introduce the operational principal with its control and modulation technique.

### 2.1. Operational principal

The power circuit of a nine-level Modular Multilevel Converter is illustrated in Figure 2. A three-phase MMC consists of six equivalent arms. Each arm of the converter contains four units of identical sub-module and a unit of arm inductance,  $L_{arm}$ . These components are connected in series. The arm inductance is used to limit the changing rate of AC current,  $i_a$ . A unit of sub-module is configured by one pair of IGBT switch and a capacitor. Figure 2 (b) illustrates the power circuit of a sub-module. In general the IGBTs are switched complementarily. By turning on  $S_x$  (gate switching control signal is set to logic 1), the sub-module voltage level is equivalent to the capacitor voltage level ( $v_{SM} = v_c$ ). Conversely, the sub-module voltage is equal to zero volt if  $S_x'$  is triggered on. Since all the sub-module is connected in series, the arm voltages,  $v_{RS}$  and  $v_{TU}$  can be determined as:

$$v_{RS} = \sum_{i=1}^4 v_{SM_{pui}} \quad (1)$$

$$v_{TU} = \sum_{i=1}^4 v_{SM_{pli}} \quad (2)$$

Where  $p$  represents phase-leg a-b-c. The pole voltage of each phase can be derived as:

$$v_{po} = \left( \frac{V_{dc}}{2} - v_{Larm} - v_{RS} \right) = \left( -\frac{V_{dc}}{2} + v_{Larm} + v_{TU} \right) \quad (3)$$

The AC current for phase leg-a can be expressed in

$$i_a = i_{ua} - i_{la} \quad (4)$$

It is highlighted that a total of six modulating waves are used to control each arm of the MMC. The concept of generation third harmonic voltage injection modulation waves, level shifted pulse width modulation and capacitor voltage balancing control method will be further explained in the following sub section.

### 2.2. Third harmonic voltage injection modulation wave

Third harmonic voltage injection pulse width modulation technique is basically extended from the classic Sinusoidal Pulse-Width-Modulation (SPWM). As illustrated in Figure 3 (a), the third harmonic voltage injection wave,  $v_{ref3}$  is produced by summing up the pure sinusoidal wave,  $v_{a1}$ , that normally used in SPWM with its third order harmonic components [16, 17]. The main advantage is to increase the maximum

output voltage amplitude without introducing additional sideband harmonics. It is noted that, the conventional Sinusoidal Pulse-Width-Modulation (SPWM) technique has limited the linear modulation range to:

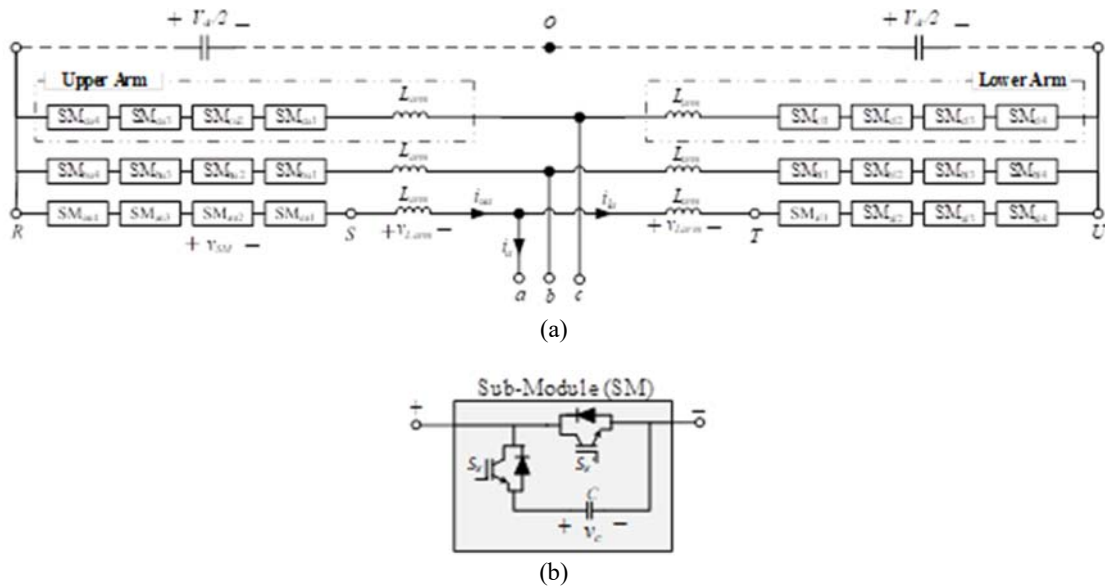


Figure 2. Power circuit of (a) nine-level modular multilevel converter (MMC), (b) Sub-module (SM)

$$0 < m_a \leq 1.0 \tag{5}$$

Where  $m_a$  indicates the amplitude modulation index. By introducing the new modulating wave,  $v_{ref}$ , the fundamental component,  $v_{a1}$ , can be raised up to 15 % greater. This is mainly due to the compensation of third order harmonic component,  $v_{a3}$ , to regulate  $v_{ref}$  within the range of 1.0. Therefore, in THVI-PWM technique, the linear modulation range is extended to:

$$0 < m_a \leq 1.15 \tag{6}$$

The six units modulating waves which are demanded for MMC modulation can be derived as:

$$\text{Upper arm modulating wave, } v_{ref,pu} = -(v_{p1} + v_3) \tag{7}$$

$$\text{Lower arm modulating wave, } v_{ref,pl} = v_{p1} + v_3 \tag{8}$$

The pure sinusoidal wave equations for each phase,  $v_{p1}$ , are:

$$\begin{aligned} v_{a1} &= V_m \sin(2\pi f_m t) \\ v_{b1} &= V_m \sin\left(2\pi f_m t - \frac{2\pi}{3}\right) \\ v_{c1} &= V_m \sin\left(2\pi f_m t + \frac{2\pi}{3}\right) \end{aligned} \tag{9}$$

The approximated expression of third order harmonic component,  $v_3$ , is as followed [18]:

$$v_3 = -\frac{\max\{v_{a1}, v_{b1}, v_{c1}\} + \min\{v_{a1}, v_{b1}, v_{c1}\}}{2} \tag{10}$$

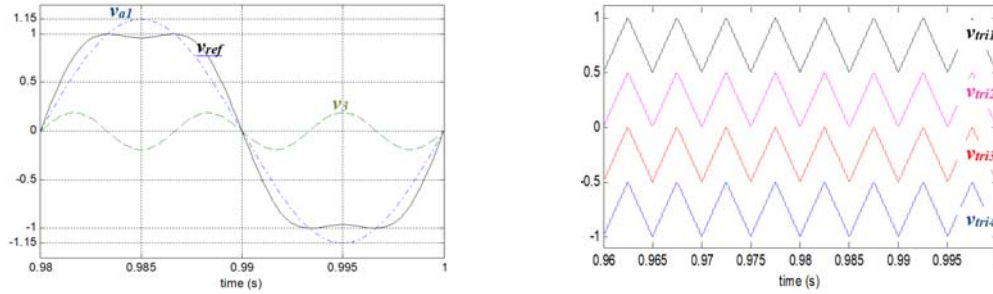


Figure 3. (a) Third harmonic voltage injection modulating wave (phase-a),  
(b) Level shifted carrier waves to be used for a nine-level MMC

### 2.3. Level shifted pulse width modulation and capacitor voltage balancing control

The number of demanded triangular carrier wave,  $v_{tri}$ , is depended on the number of sub-module connected in one arm. In this paper, four unit of carrier waves will be used. These carrier waves are shifted vertically in same phase. The amplitude of each carrier wave is equally divided as follows:

$$\hat{v}_{\Delta i} = \frac{2}{N} \quad (11)$$

Where  $N$  represents the total number of sub-module per arm. The frequency of the carrier waves is set according to the MMC switching frequency,  $f_{sw}$ . Figure 3 (b) shows the carrier waves needed for a nine-level MMC. The gate switching control signals,  $G_{pui}$  and  $G_{pli}$  will be produced when the following conditions are matched:

$$v_{ref\_pu} > v_{tri_i}, G_{pui} = 1 \text{ else } G_{pui} = 0 \quad (12)$$

$$v_{ref\_pl} > v_{tri_i}, G_{pli} = 1 \text{ else } G_{pli} = 0 \quad (13)$$

In general, only four sub-modules will be triggered on per phase leg at every instant. The switching decision of each sub-module will be defined by Capacitor Voltage Balancing (CVB) controller.

The control objective of the CVB controller is to regulate the voltage level of each floating capacitor in permitted voltage range. In order to achieve this, all capacitor voltages,  $v_c$ , and arm currents,  $i_{arm}$ , will be sampled periodically. Each arm capacitor voltage values will then be sorted in ascending order. If the respective arm current is found greater than zero ampere ( $i_{ua}$  or  $i_{ia} > 0$  A), the gate switch-on commands will be prioritized to the sub-module which capacitor voltage value ranked first. The capacitor of this sub-module will start being charged up upon triggering on. Conversely, by determining a negative arm current ( $i_{ua}$  or  $i_{ia} < 0$  A), the sub-module which capacitor voltage value is ranked at bottom will be turned on for discharging. The capacitor voltage balancing control is executed in parallel for all arms in MMC.

## 3. SYSTEM MODELLING AND RESULTS VERIFICATION

In order to evaluate the feasibility of the proposed converter, two simulation models are constructed as shown in Figure 4 (a) and (b). In Figure 4 (a), the conventional Voltage Source Inverter (VSI) is implemented as a recuperating converter. The power circuit of the VSI can be referred from [17]. Whereas, Figure 4 (b) shows the integration of the proposed Modular Multilevel Converter as a recuperating converter.

The regenerative power produced by a braking railway is modelled as a controllable voltage source. Literatures had documented that the dc voltage may rise up to 1 kV with approximately 1.5 kA dc current produced in braking mode. On the other hand, the traction power substation as shown in Figure 1 is simplified as a three-phase star connected RL load. The resistive load value is set by try and error to meet the regenerative braking current limit given in [19]. Conversely, the modelling of the inductive load is referring to the field data [19]. As the generator impedances and reactors information are not given, the impedance of the zigzag transformer is used to estimate the traction substation total impedance. Table 1 presents the parameters of the transformer. Since the proposed inverter will be integrated to the secondary star winding of the transformer (Figure 1), the primary winding to secondary star winding % impedance,  $\%Z_{sY}$ , is used to estimate the reactance of the transformer. By neglecting the resistance of the transformer,  $X_{sY}$ , is estimated as 21.81 m $\Omega$  using (14).

$$\%X_{sY} = \frac{PX_{sY}}{V_{\phi}^2} \times 100\% \tag{14}$$

Where,  $P$  and  $V_{\phi}$  represent the rated power in volt-ampere and the nominal phase voltage in volt. By using (15) the reactance of the transformer is estimated approximately 70  $\mu$ H. The simulation parameters are summarized in Table 2.

$$L_{sY} = \frac{X_{sY}}{2\pi f} \tag{15}$$

Table 1. Parameters of the zigzag transformer [19]

Parameter	Value
Rated power, $P$	3300 kVA
Rated nominal frequency, $f$	50 Hz
Rated nominal voltage – primary, $V_{p,rms}$	33 kV
Rated nominal voltage – secondary, $V_{s,rms}$	$2 \times 585$ V
Primary winding to secondary delta winding % impedance, $\%Z_{\Delta\Delta}$	6.86 %
Primary winding to secondary star winding % impedance, $\%Z_{YY}$	7.01 %

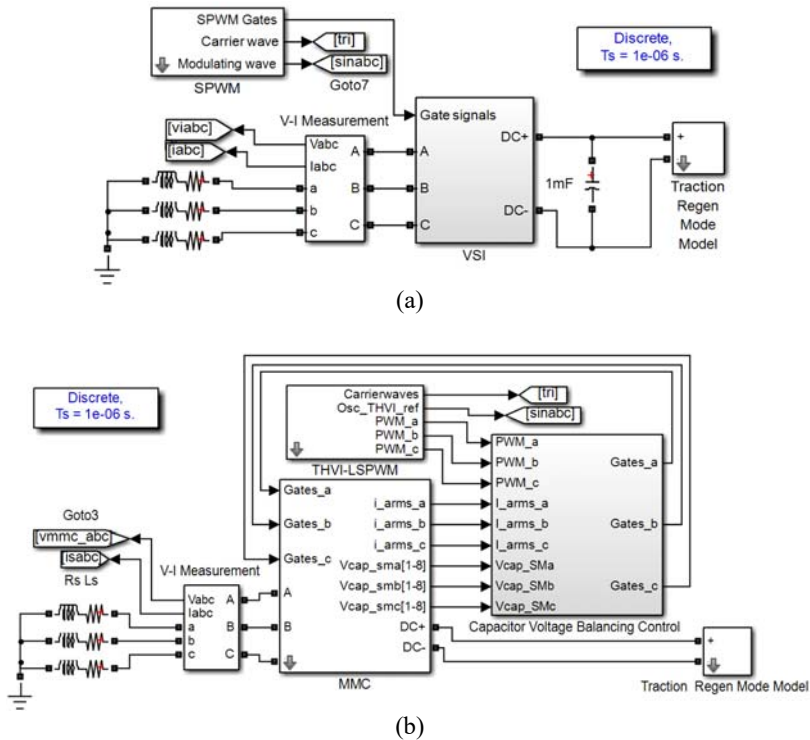


Figure 4. Simulation model of recuperating converter system: (a) Voltage source inverter (VSI), (b) Modular multilevel converter (MMC)

Table 2. Simulation parameters

	Voltage Source Inverter (VSI)	Modular Multilevel Converter (MMC)
DC link Voltage, $V_{dc}$	960 V	820 V
DC link capacitor, $C_{dc}$	1 mF	NA
Number of power cell per arm, $N$	NA	4
Capacitance per sub-module, $C_{SM}$	NA	18 mF
Arm inductor, $L_{arm}$	NA	0.5 mH
Resistive Load per phase, $R$	0.4 $\Omega$	0.4 $\Omega$
Inductive Load per phase, $L$	70 $\mu$ H	70 $\mu$ H
Switching Frequency, $f_{sw}$	1000 Hz	1000 Hz
Amplitude Modulation Index, $m_a$	1.00	1.15
Amplitude ratio of triangular waves, $\hat{v}_{tri}$	1	0.5

The recuperating converter system using VSI is much simple compare to MMC. All the gating signals are generated from the sinusoidal pulse-width-modulation (SPWM) block. Figure 5 (a) shows the simulation results of the three-phase modulating waves and a triangular wave produced inside the SPWM block. The peak of all sinusoidal waves and the triangular wave are set to 1.0 p.u. ( $m_a = 1.0$ ). The sinusoidal wave frequency is set to 50 Hz (referring to Table 1, AC load modeling) and the triangular wave frequency is set equivalent to the switching frequency, i.e. 1 kHz. A dc link capacitor of 1 mF is integrated to stabilize the dc link voltage (produced by the traction rail in regeneration mode). In this simulation, the dc link voltage is controllable (assumed outer control loop [20] is applied). Therefore the dc link voltage is regulated at 960 V. With that the line-to-line voltage is regulated at 585 V.

On the other hand, MMC gates signals are first being determined using the THVI-LSPWM modulation technique (third harmonic voltage injection level shifted pulse width modulation). Figure 5 (b) and (c) shows the carrier waves and modulation waves being generated for upper and lower arms of the MMC. Since four units of sub-modules are connected in series in each arm of MMC, four units of triangular waves are demanded. These triangular waves are identical in amplitude and phase. The modulation waves which consist of the third harmonic voltage component allow an increasing of additional 15% to the modulation index. The main advantage would be decreasing the dc link voltage level to 820 V while maintaining the effective line-to-line voltage at 585 V. The dc link capacitor (1 mF) is not demanded with the integration of MMC as recuperating converter. This is mainly due to the dc link voltage can be stabilized through the switching activities on each sub-module either to insert or bypass an appropriate number of sub-modules for each phase leg. Thus, capacitor voltage balancing control is essential to maintain the proper operation of the MMC.

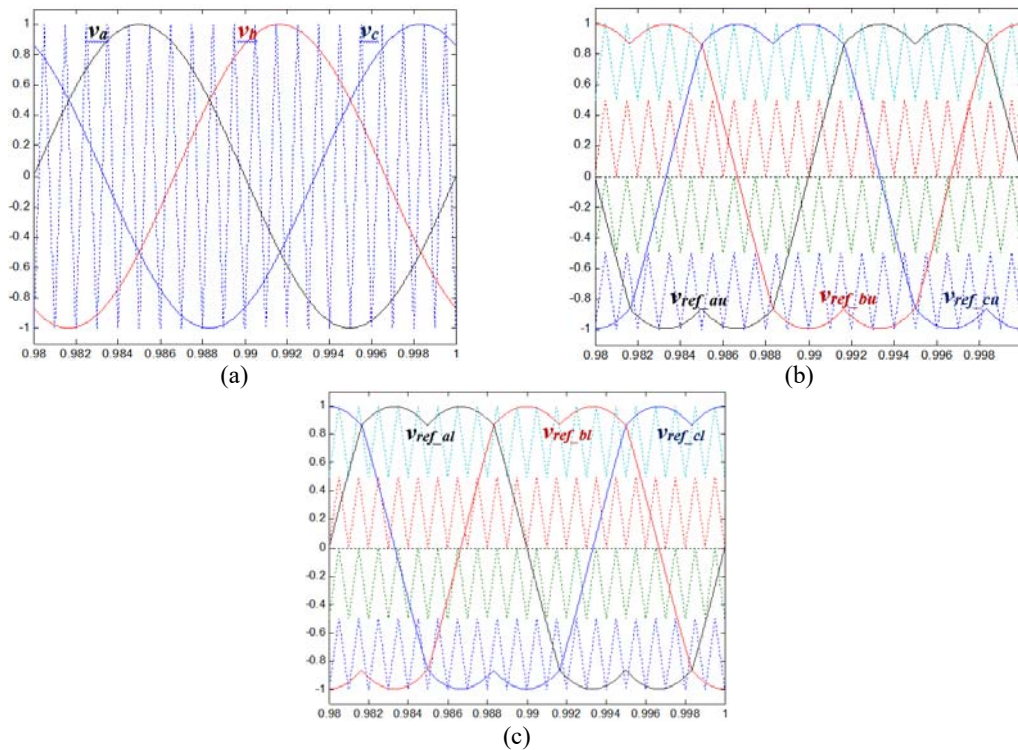


Figure 5. (a) Sinusoidal Pulse Width Modulation (SPWM) for VSI, (b) Third Harmonic Voltage Injection Level Shifted Pulse Width Modulation (THVI-LSPWM) for upper arm MMC, (c) THVI-LSPWM for lower arm MMC

As shown in Figure 4(b), the Capacitor Voltage Balancing Control block will sample the arm currents and each sub-module capacitor voltage values periodically. After executing the capacitor voltage balancing control algorithm, appropriate gate signals will then be distributed to the correspondence sub-modules. Figure 6 i. illustrates the trajectories of upper and lower arm currents in phase leg-a. When

the controller identifies a positive arm current, the capacitor voltage of all sub-modules in that particular arm will vary in an increasing trend. A sharp decline of these capacitor voltages happen when negative arm current is detected. These behaviors are clearly depicted in Figure 6 ii. The zoom-in view of capacitor voltage waveforms for sub-modules located in upper and lower arms (phase-a) are shown in Figure 6 iii and iv. The results confirm that the capacitor voltage balancing control algorithm had been modelled successfully since all the capacitor voltage levels in one arm are alternately increased or decreased.

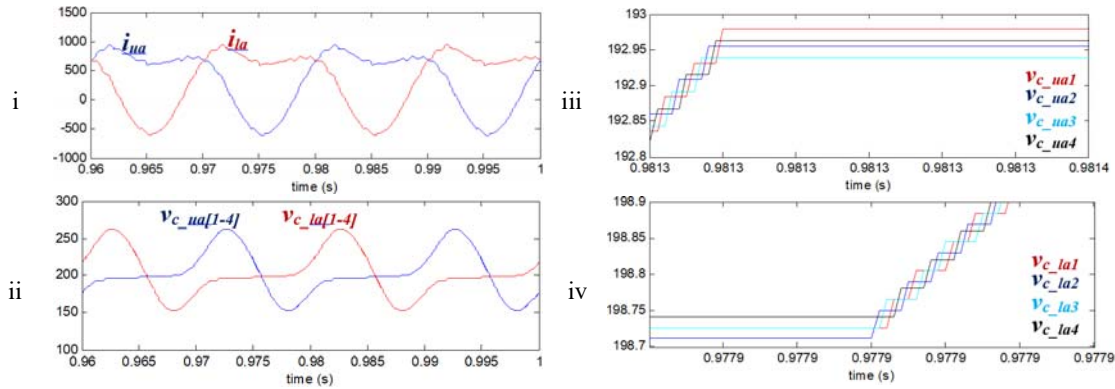


Figure 6. Simulation results for phase-a: i) arms' currents, ii) capacitor voltage of sub-modules located in phase leg-a, iii) zoom in view of  $v_{c\_ua[1-4]}$  at time instant 0.9813s, iv) zoom in view of  $v_{c\_la[1-4]}$  at time instant 0.9779s

The steady state three phase voltages and currents waveforms are presented in Figure 7. For ease of comparison, the results produced by VSI are tabulated in column (a) while column (b) is reserved for MMC results. As shown in Figure 7 (a) i., the phase voltages generated by the conventional VSI are balance but distorted. They are switched from  $-2/3V_{dc}$  to  $2/3V_{dc}$  while the line-to-line voltage waveform is triggered from  $V_{dc}$  to  $-V_{dc}$ . Their THD indexes are captured using the MATLAB Powergui FFT Anaysis Tool as 68.70 %. The AC currents also contain large ripple and a lot of sideband harmonics components. The THD indexes for all phases are closed to 33.51 %. In order to mitigate these harmonic distortion, AC filters [21, 22] must be implemented.

However, this power quality issue can also be solved by implementing MMC as a recuperating converter in TPSS. As shown in Figure 7 (b) i., MMC manages to produce sinusoidal phase voltages and line-to-line voltage waveforms with small ripples. These voltages distortion indexes are recorded less than 3.5 %. In addition a clean and good quality line currents had also been generated with the THD index as low as 2.37 %. All the THD indexes for waveforms shown in Figure 7 are summarized in Table 3.

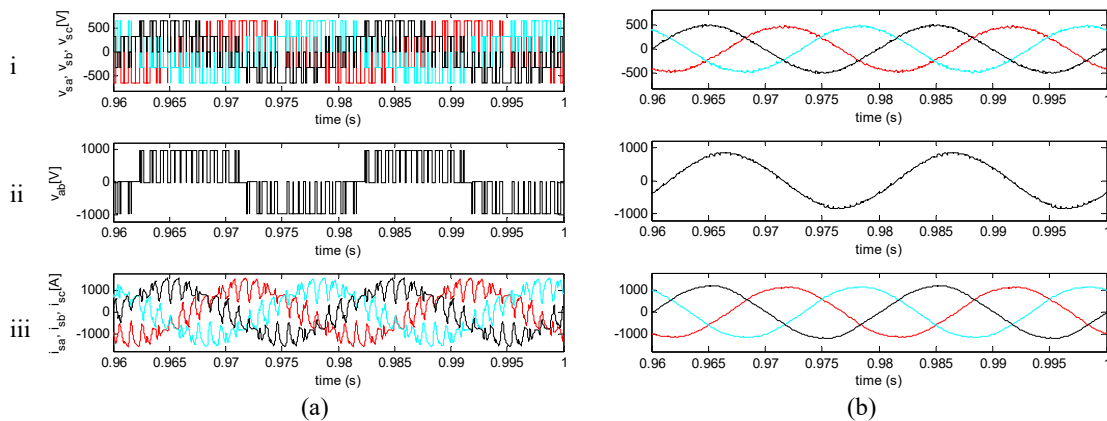


Figure 7. Simulation results for (a) VSI, (b) MMC. The sub-plots show: i) phase voltage waveforms, ii) line-to-line voltage,  $v_{ab}$ , waveform, and iii) phase current waveforms

Table 3. Total harmonic distortion indexes comparison between voltage source inverter (VSI) and modular multilevel converter (MMC)

	VSI	MMC
Phase voltage distortion, $THD_v$	68.70 %	3.29 %
Line-line voltage distortion, $THD_{ll}$	68.71 %	3.14 %
Phase current distortion, $THD_i$	33.51 %	2.37 %

#### 4. CONCLUSION

This paper proposes to replace a conventional recuperating converter system with a nine-level Modular Multilevel Converter (MMC). The operational principal of the MMC had been presented in brief together with a feasible control and modulation technique. Authors choose to balance the voltage level of the capacitor in each sub-module as the main control objective. A simple control algorithm had been proposed to keep all the capacitor voltages fluctuate within a tolerated band. Besides, the concept of third harmonic voltage injection level shifted pulse width modulation (THVI-LSPWM) technique had been discussed. The simulation results of the MMC has confirmed that the AC line filter and dc link capacitor are possible to be eliminated. The produced voltages and currents are nearly sinusoidal with the Total Harmonic Distortion (THD) indexes recorded less than 3.5 %.

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