International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 13, No. 1, March 2022, pp. 39~46
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v13.i1.pp39-46

Nine-level inverter with lesser number of power semiconductor switches using dSPACE

Sumit Raj, Rajib Kumar Mandal, Mala De, Ashutosh Kumar Singh
Department of Electrical Engineering, National Institute of Technology Patna, Patna, India

Article Info

Article history:

Received Jul 24, 2019
Revised Jan 20, 2022
Accepted Jan 27, 2022

Keywords:

DC-AC converter
Multilevel inverter
Sinusoidal PWM
Total harmonic distortion

ABSTRACT

In this paper, a single-phase nine-level multilevel inverter (MLI) topology is created in which reduced number of switches, diodes and gate driver circuits can be used so as to obtain higher output voltage levels. Due to this configuration, the blocking voltage value across the switches will also get reduced. In this proposed single-phase MLI topology, increase in output voltage levels can be observed whenever there is increment in the number of switches in the configuration. Proper mathematical modeling and analysis of the voltage waveform of the proposed inverter have been done for a 9-level MLI. MATLAB platform is used for modeling and simulation of the MLI. Modulation index is varied in order to observe various outcomes through simulation. The proposed nine-level inverter configuration is experimentally evaluated in the laboratory for various modulation indices so as to validate the simulation results. Comparison of this topology is done with the classical MLIs in order to illustrate its advantages.

Corresponding Author:

Sumit Raj
Department of Electrical Engineering, National Institute of Technology Patna
Patna-800005, India
Email: sumitraj165@gmail.com

1. INTRODUCTION

It has been 35 years since the introduction of multilevel inverters (MLIs) [1] and still this area of study fascinates researchers and industrialists all around the world. MLI produces a higher output voltage levels in comparison with conventional 2-level inverters. These higher output voltage level waveforms have inherently lesser harmonic content, lesser switching losses, high voltage compatibility, enhanced power quality with better electromagnetic compatibility. MLIs are used in motor drives, reactive power support, and renewable energy sources (RES) [2]–[4]. The main objective of MLI is to obtain the desired AC waveform using several DC sources and power electronic switches [5], [6].

Numerous topologies of MLIs have been created including the classical topologies of neutral point clamped (NPC) MLI [7], [8]. Flying capacitor (FC) MLI [9], [10] and cascaded H-bridge (CHB) MLI [11], [12]. Unequal sharing of voltage among the capacitors connected in series and requirement of clamping diodes are the problems associated with NPC MLI. The storage capacitors are subjected to unbalance voltages and also the bulky circuits are the demerits in FC MLI configuration. CHB MLIs require the least number of power electronic components (IGBT, capacitors, and diodes) among the classical topologies [13]–[15]. But they require separate H-bridge for each of the DC sources [16], [17].

A new type of MLI with reduced no of semiconductor power switches has been proposed [18]. This MLI topology requires additional number of bidirectional semiconductor power switches. Also, the magnitude of blocking voltage is higher across these bidirectional semiconductor power switches. Some MLIs with reduced switches, single isolated DC source having other DC sources replaced with capacitors and control techniques are presented [19]. Single DC source CHB (SDC-CHB) with control algorithms such as one-

dimensional feed forward phase shift modulation technique and space-vector modulation (1DFF-SVM) technique is presented [20]. The MLI topologies using the half bridge and T-type converter has been proposed [21]. Various modulation techniques are available in literature for the modulation of MLI [22]. Among them, the high-frequency pulse width modulation (PWM) technique such as level-shifted PWM and carrier phase-shifted PWM technique [23], [24], space vector modulation techniques (SVM) have been used [25]. Furthermore, synchronous optimal PWM [26], [27], active harmonic elimination [28], selective harmonic elimination [29], and nearest level control [30] methods are described as low semi-conductor switching-frequency modulation technique.

In this article, a novel topology of symmetrical MLI with lesser number of power electronic switches in comparison with classical topology, is presented. The proposed inverter optimizes the inverter for attainment of various objectives like minimization of IGBTs, power diodes, and gate drivers resulting in reduced cost, higher efficiency and simple control techniques. The proposed 9-level MLI structure is simulated in MATLAB platform and then the output results have been validated experimentally in the hardware set up for both resistive and inductive loads at various modulation indexes.

2. PROPOSED MULTI-LEVEL INVERTER CONFIGURATION

Figure 1 represents the proposed topology of the MLI. It uses ten power electronic switches (S_a, S_b, S_{L1}, S_{L2}, S_{L3}, S_{L4}, S_{R1}, S_{R2}, $S_{R3,}$ and S_{R4}) and four isolated DC voltage sources (V_{L1}, $V_{L2,}$ and V_{R1}, V_{R2}). Four identical dc sources, V_{L1}, V_{L2}, $V_{R1,}$ and V_{R2}, are used to provide DC voltage to the proposed MLI. The inverter generates 9-levels if the ratios of the input isolated DC voltages (V_{L1}: V_{L2}: V_{R1}: V_{R2}) is chosen as 1: 1: 1: 1.

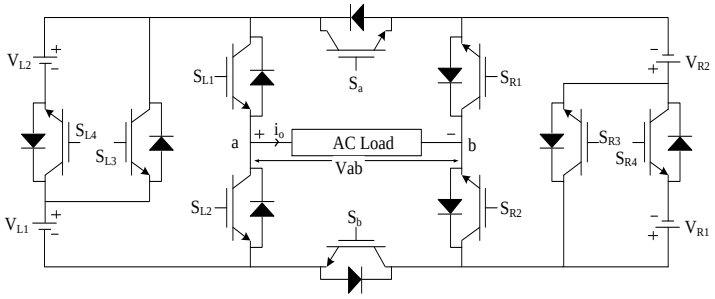


Figure 1. Configuration of the proposed MLI

2.1. Generation of output voltage levels

Table 1 represents the switching sequence of the proposed MLI. Here, 1 and 0 respectively represent the ON and OFF states of the switches. The various modes of operation of this MLI are clearly represented in Figure 2. specified. It can be observed in Figures 2 (a) and 2 (b) that a zero level can be obtained by switching ON the upper switches $S_{L1,}$ $S_{R1,}$ and S_a or the lower switches $S_{L2,}$ $S_{R2,}$ and S_b. We will get the positive voltage level V_{L1} by turning ON the switches S_{L3}, S_{L1}, S_{R2} and S_b as shown in Figure 2 (c). The figure represents only the positive current flow through the load but it works for negative current flow as well. To get a level having double the value of DC voltage used, we turn ON the switches S_{L4}, S_{L1}, S_{R2} and S_b which is shown in Figure 2 (d). In Figure 2 (e), we can observe another level getting added up as another DC source comes in the picture when we turn ON the switches S_{L4}, S_{L1}, S_{R1}, $S_{R3,}$ and S_b. Another level is achieved by turning ON switches S_{L4}, S_{L1}, S_{R1}, $S_{R4,}$ and S_b which gives us four times the value of DC voltage which is represented in Figure 2 (f). This completes our positive half cycle of the output which is shown in Figures 2 (b) to 2 (f). Using the same mechanism, the negative half cycle can be generated which is shown from the Figures 2 (g) to 2 (j).

The voltage levels in output (N_{level}), no. of IGBTs (N_{IGBT}) and maximum output voltage ($E_{o,max}$) is given by:

$$N_{level} = 2m + 1 \quad (1)$$

$$N_{IGBT} = 2(m + 1) \quad (2)$$

$$E_{O,max} = mE \quad (3)$$

Here *'m'* is the total number of dc voltage sources.

Table 1. Output voltage of the proposed nine-level inverter

S_{L1}	S_{L2}	S_{L3}	S_{L4}	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_a	S_b	Vab
1	0	0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0	1	0
1	0	1	0	0	1	0	0	0	1	V_{L1}
1	0	0	1	0	1	0	0	0	1	$V_{L1}+V_{L2}$
1	0	0	1	1	0	1	0	0	1	$V_{L1}+V_{L2}+V_{R1}$
1	0	0	1	1	0	0	1	0	1	$V_{L1}+V_{L2}+V_{R1}+V_{R2}$
0	1	1	0	1	0	0	0	1	0	$-V_{L1}$
0	1	0	1	1	0	0	0	1	0	$-(V_{L1}+V_{L2})$
0	1	0	1	0	1	1	0	1	0	$-(V_{L1}+V_{L2}+V_{R1})$
0	1	0	1	0	1	0	1	1	0	$-(V_{L1}+V_{L2}+V_{R1}+V_{R2})$

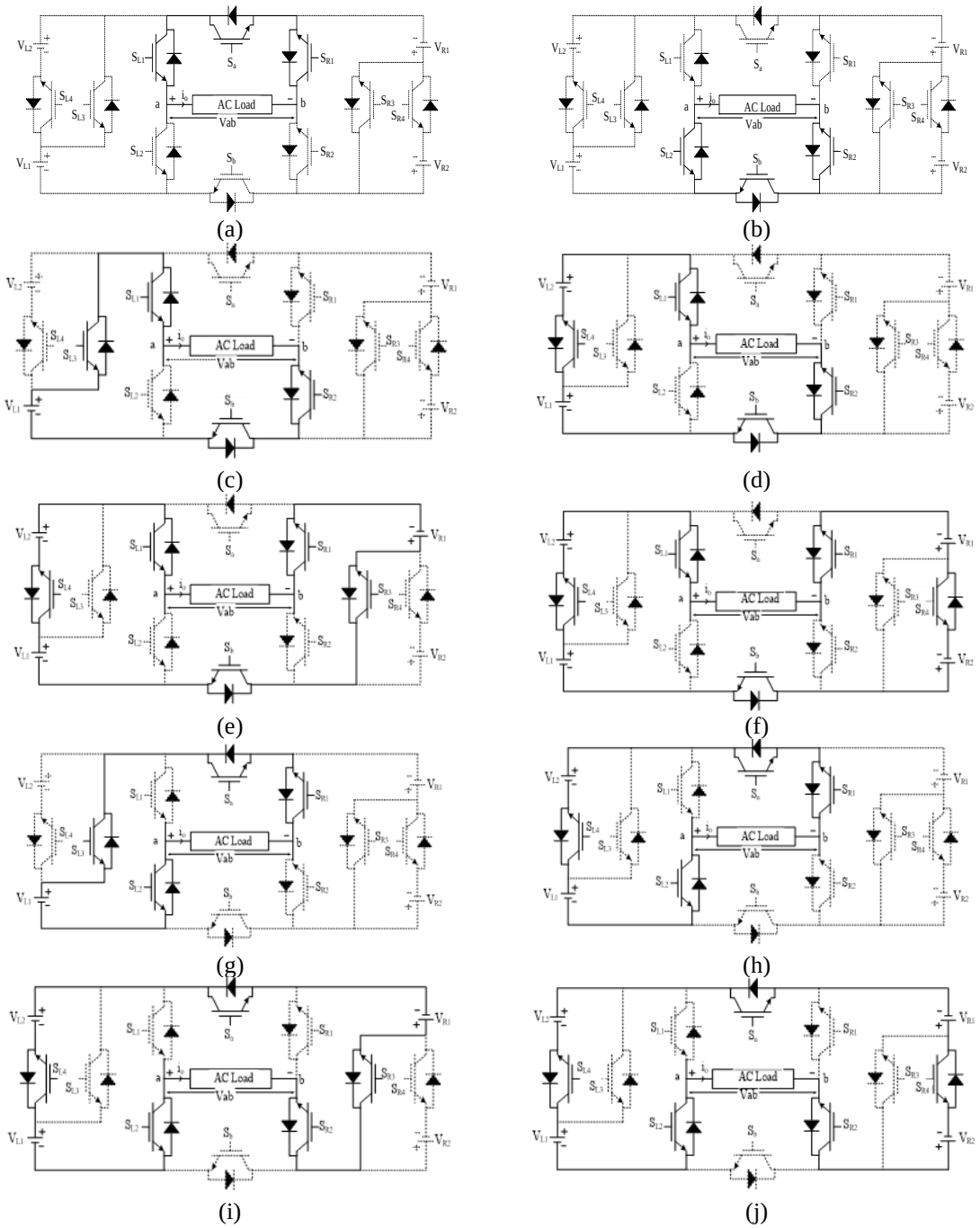


Figure 2. Operating modes of the proposed 9-level MLI for (a) Vab=0, (b) Vab=0, (c) Vab=V_{L1}, (d) Vab=$V_{L1}+V_{L2}$,, (e) Vab=$V_{L1}+V_{L2}+V_{R1}$, (f) Vab=$V_{L1}+V_{L2}+V_{R1}+V_{R2}$, (g)Vab=$-V_{L1}$, (h) Vab=$-(V_{L1}+V_{L2})$, (i) Vab = $-(V_{L1}+V_{L2}+V_{R1})$, and (j) Vab=$-(V_{L1}+V_{L2}+V_{R1}+V_{R2})$

2.2. Modulation & control technique for the proposed MLI

For generation of gate pulses for the switches, various methods like the fundamental switching frequency method, sinusoidal PWM (SPWM) method, space vector PWM method, can be implemented. Here, we are using SPWM technique is implemented for generation of the pulses for the switches of the proposed inverter. PD-PWM (phase disposition PWM), a level shifted PWM technique is used here. In this technique, a sinusoidal reference waveform at the fundamental frequency is compared with eight triangular carrier signals of very high frequency to generate the PWM switching signal for the proposed 9-level MLI. These eight signals are Vcr4-, Vcr3-, Vcr2-, Vcr1-, Vcr1+, Vcr2+, Vcr3+, and Vcr4+ as represented in Figure 3. The pulses obtained through this method are combined with appropriate digital logic gates to obtain the gate pulses are shown in Figure 4.

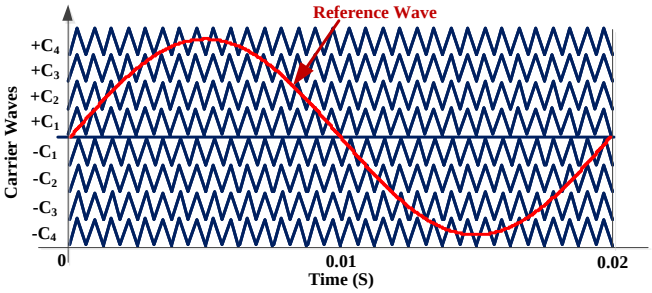


Figure 3. Reference and multi-carrier waveforms of the proposed topology

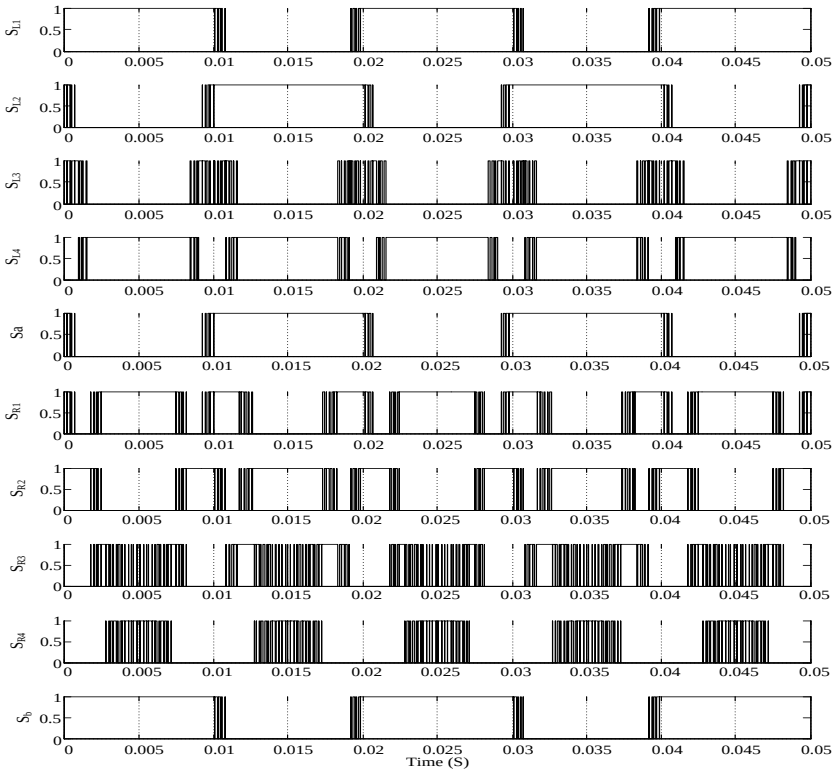


Figure 4. Switching pulses for the proposed 9-level MLI

3. RESULTS AND DISCUSSION

The simulation of the proposed single-phase nine-level MLI is performed in MATLAB platform to investigate the output results. The value of 'E' i.e., each isolated DC voltage source for the inverter is taken as 21 V. The output terminals of the proposed MLI is fed to an inductive load with $R = 25\Omega$ and $L = 10\ mH$ taken for both simulation and experimental confirmation. The switching frequency of the MLI (f_s) is taken 10 KHz.

The output voltage waveform along with the FFT analysis for different modulation indexes (MI) is shown in Figure 5. The simulated results of the inverter voltage and the FFT analysis corresponding to the nine-level can be seen here. The variation in fundamental component of the output voltage and total harmonic distortion (THD) can be observed with the change in M.I. As shown in Figure 5 (a), the output voltage obtained is 79.77 V with THD 11.10% by keeping the value of M.I.=1. If we change the value of M.I. to 0.7, output voltage obtained is 55.47 V with THD 17.82% as shown in Figure 5 (b). Further decreasing the value of M.I. to 0.3, output voltage obtained is 39.24 V with THD 22.20% as per Figure 5 (c).

In order to verify the proposed MLI, a hardware set up has been made as per the block diagram in Figure 6. The hardware prototype of the simulated MLI is developed as shown in Figure 7. Full bridge rectifiers act as isolated DC sources to the MLI. Level shifted PWM method generates the gate pulses for the IGBTs of the MLI. dSPACE DS 1103 real time controller feeds the control signals to the IGBTs in hardware. The specification of the components used is given in Table 2.

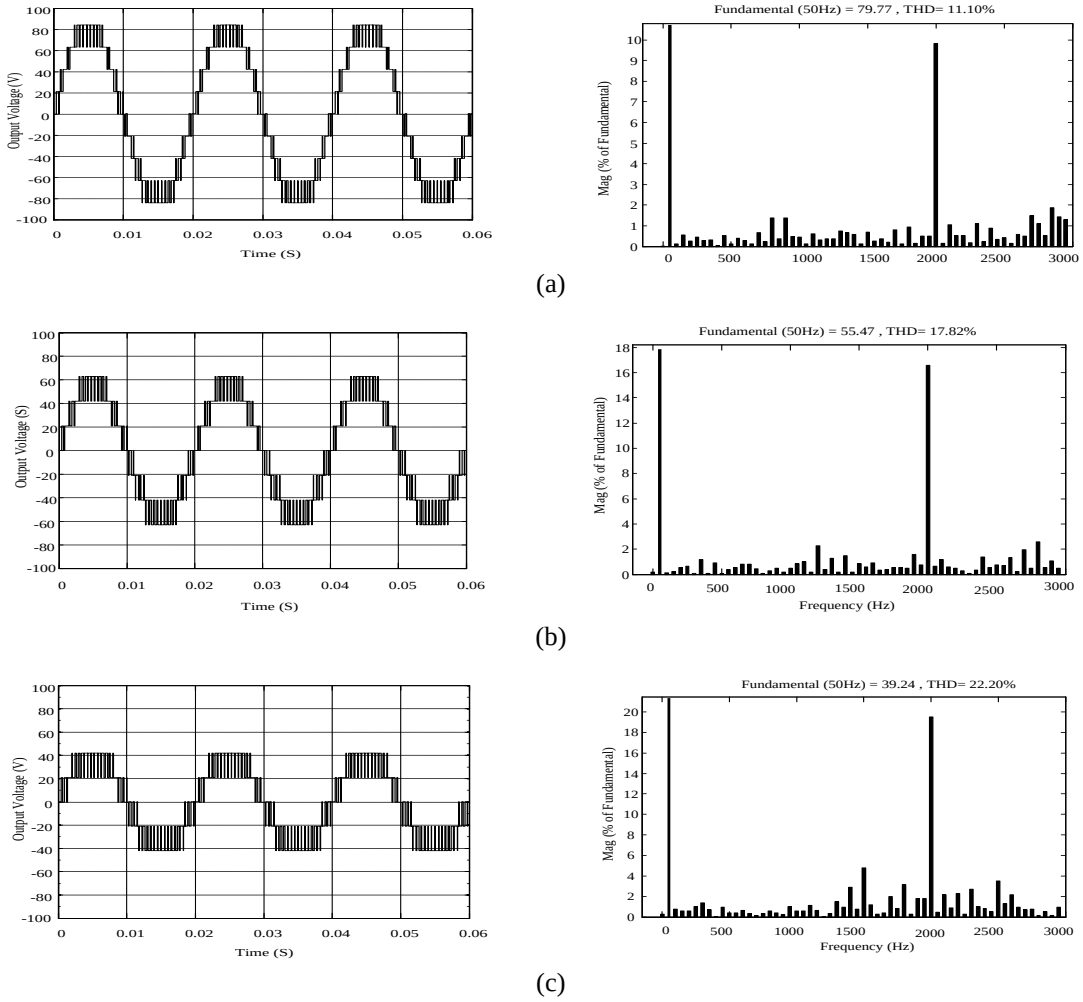


Figure 5. Simulated results of output voltage with corresponding THD (a) M.I.=1, (b) M.I.=0.7 and (c) M.I.=0.3

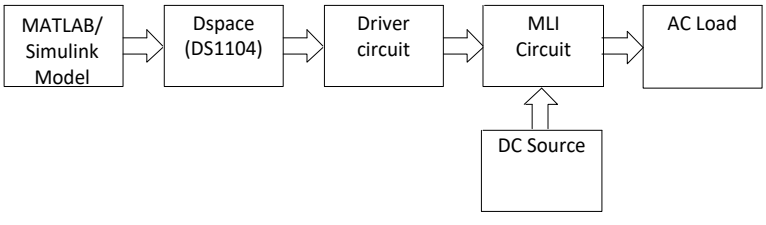


Figure 6. Block diagram for hardware setup of the 9-level MLI

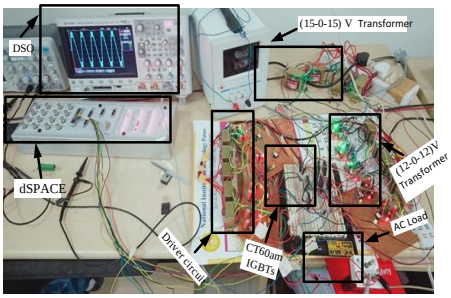
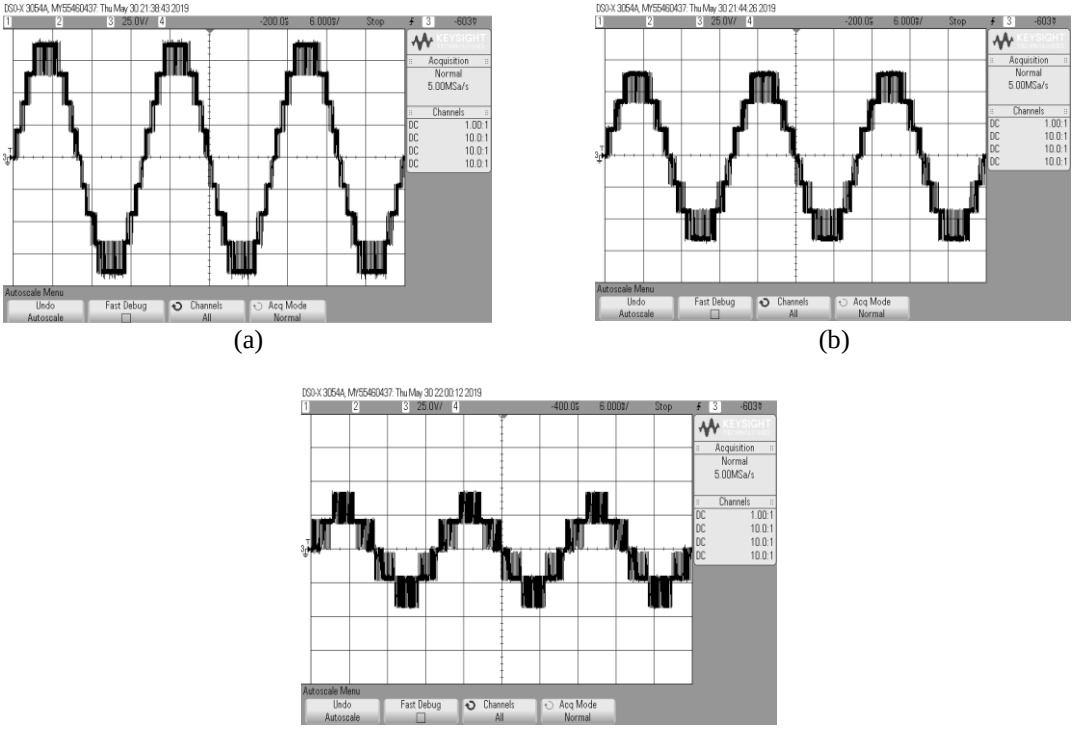


Figure 7. Experimental setup of the proposed technology

Table 2. Components used for a nine-level inverter hardware setup

Components	Specification
IGBTs (CT60AM)	900 V, 60 A
Transformer (Step down)	12-0-12 V, 1 mA
Voltage Regulator	7912,7812
Diode (IN4007)	1 kV, 30 A, 3 W
Capacitor	1000 µF and 100 µF, 25 V
Opto-Coupler (TLP 250)	10-35 V, ±1.5 A

The experimental results of output voltage waveform of the proposed MLI for different values of M.I. (0.5, 0.7 and 1.0), are given in Figures 8 (a), 8 (b) and 8 (c) respectively. Clearly, the magnitude of the output voltage changes by variation of the M.I. Also, the output voltage levels were decreasing and hence the THD was increasing by decreasing the values of M.I. Comparison of other symmetrical MLIs with the proposed MLI is shown in Table 3 for any generalized level 'N_{level}'. Also, the comparison of various 9-level MLI topologies as per Figure 9 shows the superiority of the proposed topology.



(a) (b)

(c)

Figure 8. Hardware result of output voltage for (a) M.I.=1, (b) M.I.=0.7 and (c) M.I.=0.3

Table 3. Comparison of other symmetrical topologies with proposed symmetrical MLI topology

Topology	Main switching devices	Main diodes	Clamping diodes	Balancing capacitors
FCMLI [7]	$2(N_{level}-1)$	$2(N_{level}-1)$	0	$0.5(N_{level}-1)(N_{level}-2)$
NPCMLI [9]	$2(N_{level}-1)$	$2(N_{level}-1)$	$(N_{level}-1)(N_{level}-2)$	0
CHBMLI [11]	$2(N_{level}-1)$	$2(N_{level}-1)$	0	0
[15]	$3(N_{level}-1)/2$	$3(N_{level}-1)/2$	0	0
[17]	$N_{level}+3$	$N_{level}+3$	0	0
Proposed MLI	$N_{level}+1$	$N_{level}+1$	0	0

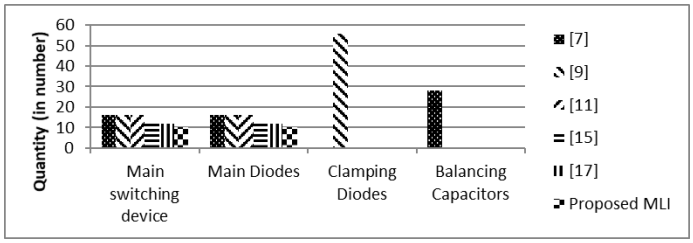


Figure 9. Comparison of nine-level MLI topologies

4. CONCLUSION

In this article, a novel 9-level symmetrical MLI topology with lesser number of power electronic devices, in comparison with classical MLI topologies, is proposed. The proposed inverter optimizes the inverter for attainment of various objectives like minimization of IGBTs, power diodes, and gate driver circuits resulting in reduced cost, higher efficiency and simple control techniques. The simulation of MLI is performed in MATLAB software. The results of simulation are then verified with the experimental results obtained in the laboratory through the hardware set up for resistive and inductive loads with different values of modulation indexes.

REFERENCES

[1] R. Stala, "A Natural DC-Link Voltage Balancing of Diode-Clamped Inverters in Parallel Systems," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 5008-5018, 2013, doi: 10.1109/TIE.2012.2219839.

[2] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," *IEEE Transactions on Industry Applications*, vol. 36, no. 3, pp. 834-841, 2000, doi: 10.1109/28.845059.

[3] R. Alonso, E. Roman, A. Sanz, V. E. Martínez Santos, and P. Ibanez, "Analysis of Inverter-Voltage Influence on Distributed MPPT Architecture Performance," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3900-3907, 2012, doi: 10.1109/TIE.2012.2189532.

[4] M. N. Abdul Kadir, S. Mekhilef, and H. W. Ping, "Voltage vector control of a hybrid three-stage 18-level inverter by vector decomposition," *IET Power Electron.*, vol. 3, no. 4, pp. 601-611, 2010, doi: 10.1049/iet-pel.2009.0085.

[5] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," *Power Engineering Society Summer Meeting (Cat. No.00CH37134)*, 2000, pp. 1271-1274 vol. 2, doi: 10.1109/PESS.2000.867569.

[6] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Zhong Du, "Control of a multilevel converter using resultant theory," *IEEE Transactions on Control Systems Technology*, vol. 11, no. 3, pp. 345-354, 2003, doi: 10.1109/TCST.2003.810382.

[7] R. Stala, "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 4185-4195, 2011, doi: 10.1109/TIE.2010.2093477.

[8] Z. Pan, F. Z. Peng, V. Stefanovic, and M. Leuthen, "A diode-clamped multilevel converter with reduced number of clamping diodes," *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition APEC '04*, 2004, pp. 820-824 vol. 2, doi: 10.1109/APEC.2004.1295917.

[9] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, vol. 1, pp. 397-403, doi: 10.1109/PESC.1992.254717.

[10] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," *The 2010 International Power Electronics Conference - ECCE ASIA*, 2010, pp. 492-501, doi: 10.1109/IPEC.2010.5544625.

[11] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Electric Power Systems Research*, vol. 77, no. 8, pp. 1073-1085, 2007. doi: 10.1016/j.epsr.2006.09.012.

[12] K. Sivakumar, A. Das, R. Ramchand, C. Patel, and K. Gopakumar, "A Hybrid Multilevel Inverter Topology for an Open-End Winding Induction-Motor Drive Using Two-Level Inverters in Series With a Capacitor-Fed H-Bridge Cell," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 11, pp. 3707-3714, 2010, doi: 10.1109/TIE.2010.2040565.

[13] M. G. Hosseini Aghdam, S. H. Fathi, and G. B. Gharehpetian, "Comparison of OMTHD and OHSW harmonic optimization techniques in multi-level voltage-source inverter with non-equal DC sources," *7th Internatonal Conference on Power Electronics*, 2007, pp. 587-591, doi: 10.1109/ICPE.2007.4692456.

[14] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 769-778, 2012, doi: 10.1109/TIE.2011.2157290.

[15] Gui-Jia Su, "Multilevel DC-link inverter," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 848-854, 2005, doi: 10.1109/TIA.2005.847306.

[16] P. K. Chaturvedi, S. Jain, and P. Agarwal, "Reduced switching loss pulse width modulation technique for three-level diode clamped inverter," *IET Power Electron.*, vol. 4, no. 4, pp. 393-399, 2011. doi: 10.1049/iet-pel.2010.0311.

[17] W. Choi and F. Kang, "H-bridge based multilevel inverter using PWM switching function," *INTELEC 2009 - 31st International Telecommunications Energy Conference*, 2009, pp. 1-5, doi: 10.1109/INTLEC.2009.5351886.

[18] E. Babaei, "A Cascade Multilevel Converter Topology With Reduced Number of Switches," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2657-2664, 2008, doi: 10.1109/TPEL.2008.2005192.

[19] H. Vahedi, P. Labbé, and K. Al-Haddad, "Sensor-Less Five-Level Packed U-Cell (PUC5) Inverter Operating in Stand-Alone and Grid-Connected Modes," *IEEE Transactions on Industrial Informatics*, vol. 12, no. 1, pp. 361-370, 2016, doi: 10.1109/TII.2015.2491260.

[20] J. D. Barros, J. F. A. Silva, and É. G. A. Jesus, "Fast-Predictive Optimal Control of NPC Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 619-627, 2013, doi: 10.1109/TIE.2012.2206352.

[21] U. Choi, K. Lee, and F. Blaabjerg, "Diagnosis and Tolerant Strategy of an Open-Switch Fault for T-Type Three-Level Inverter Systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 495-508, 2014, doi: 10.1109/TIA.2013.2269531.
[22] W. Qian, F. Z. Peng, and L. M. Tolbert, "Development of a 55 kW 3X dc-dc converter for HEV systems," *IEEE Vehicle Power and Propulsion Conference*, 2009, pp. 433-439, doi: 10.1109/VPPC.2009.5289814.
[23] R. M. B. Moritz, and A. L. Batschauer, "Capacitor voltage balancing in a 5-L full-bridge flying capacitor inverter," *Brazilian Power Electronics Conference (COBEP)*, 2017, pp. 1-6, doi: 10.1109/COBEP.2017.8257234.
[24] C. Kumar, B. Mahato, R. Raushan, T. Maity, and K. C. Jana, "Comprehensive study of various configurations of three-phase Multilevel inverter for different levels," *3rd International Conference on Recent Advances in Information Technology (RAIT)*, 2016, pp. 310-315, doi: 10.1109/RAIT.2016.7507922.
[25] B. Singh, B. P. Singh, and S. Dwivedi, "Dsp based implementation of vector control scheme for permanent magnet synchronous motor drive," *IETE Journal of Research*, vol. 53, no. 2, pp. 153-164, 2007. doi: 10.1080/03772063.2007.10876131.
[26] A. Majed, Z. Salam, and A. M. Amjad, "Harmonics elimination PWM based direct control for 23-level multilevel distribution STATCOM using differential evolution algorithm," *Electric Power Systems Research*, vol. 152, pp. 48-60, 2017, doi: 10.1016/j.epsr.2017.06.022.
[27] J. C. Wu, K. Der Wu, H. L. Jou, and S. K. Chang, "Small-capacity grid-connected solar power generation system," *IET Power Electron.*, vol. 7, no. 11, pp. 2717-2725, 2014. doi: 10.1049/iet-pel.2014.0015.
[28] S. N. Rao, D. V. A. Kumar, and C. S. Babu, "New multilevel inverter topology with reduced number of switches using advanced modulation strategies," *International Conference on Power, Energy and Control (ICPEC)*, 2013, pp. 693-699, doi: 10.1109/ICPEC.2013.6527745.
[29] M. S. A. Dahidah, G. Konstantinou, and G. V. Agelidis, "SHE-PWM and optimized DC voltage levels for cascaded multilevel inverters control," *2010 IEEE Symposium on Industrial Electronics and Applications (ISIEA)*, 2010, pp. 143-148, doi: 10.1109/ISIEA.2010.5679479.
[30] R. Gupta, A. Ghosh, and A. Joshi, "Switching Characterization of Cascaded Multilevel-Inverter-Controlled Systems," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1047-1058, 2008, doi: 10.1109/TIE.2007.896274.

BIOGRAPHIES OF AUTHORS

Sumit Raj has completed his B.Tech. in Electrical Engineering from GNIT Kolkata in 2015 and M.Tech. in Power Electronics & Drives from NIT Jamshedpur in 2019. Currently, he is pursuing his PhD from NIT Patna. His area of research includes multilevel inverter, renewable energy sources and DC-DC converter. He can be contacted at email: sumitraj165@gmail.com.

Rajib Kumar Mandal has received his BE from MACT (REC), Bhopal in 1999 and ME from Jadavpur University in 2004. He has completed his PhD from NIT Patna in 2018. He is presently working as an Assistant Professor in the Department of Electrical Engineering, NIT Patna. He can be contacted at email: rajib@nitp.ac.in.

Mala De has received her BE in Electrical Engineering from Jalpaiguri Government Engineering College in 2000. She has completed M.Tech. in Power and Energy Systems from NIT Silchar in 2007 and consequently PhD from Jadavpur University in 2012. She is presently working as an Assistant Professor in the Department of Electrical Engineering, NIT Patna. She can be contacted at email: mala.de.power@gmail.com.

Ashutosh Kumar Singh is pursuing Ph. D. from National Institute of Technology, Patna, India. He received the B.Tech. degrees in electrical and electronics engineering from Motihari College of Engineering, Motihari, and M.Tech. degrees in electrical engineering from National Institute of Technology, Patna, India, in 2016 and 2019, respectively. His research interests switched capacitor power electronic converters. He can be contacted at email: ash170723@gmail.com.