International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 11, No. 3, September 2020, pp. 1449∼1458
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v11.i3.pp1449-1458

Using sigma-delta quantizer based PI for inductive power transfer systems

Dhafer J. Almakhles[1], Akshya Swain[2], Hou Yuefeng[3]
[1]Renewable Energy Lab, Communications and Networks Engineering, Prince Sultan University, Saudi Arabia
[2]Department of Electrical and Computer Engineering, University of Auckland, New Zealand
[3]Electric and Instrument Section, Beijing Haunqiu Corporation, China

Article Info

Article history:

Received Aug 2, 2019
Revised Dec 2, 2019
Accepted Mar 21, 2020

Keywords:

Inductive power transfer (IPT)
Proportional integral (PI)
Single-delta quantizer

ABSTRACT

In this paper, a Sigma-Delta Quantizer (Σ△-Q) based Proportional and Integral control is proposed for a wireless power transfer control system, namely inductive power transfer system. The proposed control topology employs Σ△-Qs to convert the conventional signals (analog/digital signals) into bitsreatm signals (1-bit per sample time). Considering the oversampling feature of Σ△-Q, field programmable gate array is utilized in the implementation of the control system. To evaluate the effectiveness of the presented control topology, it is compared with an inductive power transfer control system using the conventional proportional and integral controller. For the sake of simplicity, the comparison is carried out using hardware in Loop. Both control systems exhibit almost identical responses. However, the bitstream feature of the proposed PI controller significantly helps in reducing the hardware resources (logic elements) in field programmable gate array. In addition, less wire routing and computational complexity is achieved due to absence of multipliers.

Corresponding Author:
Dhafer J. Almakhles
Renewable Energy Lab, Communications and Networks Engineering,
Prince Sultan University,
P.O.Box No. 66833 Rafha Street, Riyadh 11586 Saudi Arabia.
Email: dalmakhles@psu.edu.sa

1. INTRODUCTION

Due to the large consumption of fossil fuel in the world, many countries have actively involved in the usage of renewable energy for sustainability and the pollution reduction. The weakness of using renewable energy, especially solar energy, is that it is intermittent and variable [1]. This intermittent nature requires conventional power plants or massive storage facilities such as battery banks as reservations. With the developments of electric vehicle (EV), a novel technology so-called vehicle to grid (V2G) system attract the attention of both academia and the industries [2, 3]. With V2G technology, the energy can be stored in the EVs' battery. The huge amount of car batteries could be integrated to a battery bank for power grid. In order to achieve the V2G system, the EVs have to plug in and out very often and convenient. Dragging charging cables everywhere is not an appropriate solution. With the recent development of power electronics technologies, a fascinating wireless power transfer system, so-called bidirectional inductive power transfer (BIPT) system is shown to be ideally suited for the V2G systems. Generally speaking, BIPT can be operated automatically and effectively used in as a wireless charger and discharger system. In the literature, it is recommended to make BIPT systems operate at a range of frequency between 10 and 40 kHz in order increase the efficiency of the

entire system [4–8]. Further, the performance of the BIPT system could be enhanced by combining it with compensations. However, the BIPTs together with the compensations inevitably become more complicated with high-order resonant networks; and thus a robust controller with simple topology is required.

Typical discrete controllers, designed for power electronics, are often implemented on field programmable gate array (FPGA) due to the high speed and parallel processing FPGAs offer [9, 10]. Thus, all the interfacing signals with BIPT including the signals in the processors have to be converted to digital signals with 8-bit, 16-bit, or 32-bit signed fixed-point representation. Mixed-signals integrated circuits such as analog/digital, referred to as A/D and digital/analog, referred to as D/A converters are important to be used the proposed BIPT control system. Most A/D converters consists of uniform multi-level static quantizer which in turn require multi-wires to transfer data. Transmission of multi-bit word could be disordered when the transmission becomes sophisticated. Furthermore, general arithmetic operation including summation or multiplication, are processed simultaneously (parallel computing), which results in high routing consumption in FPGAs and complicated signal processing. One widely dynamic A/D converters equipped, so-called Sigma-Delta modulation ($\Sigma\triangle$-Q) has attracted the mixed-signal circuits designers due to its feature in the reduction of the data transmissions, routing, wiring and signal processing [11, 12]. One of the main advantages of using $\Sigma\triangle$-Q is that it converts the input signals to single-bit signals (1-bit per sampling time) which provides unique features over in any digital signal processors [13, 14].

In the signal processing field, using $\Sigma\triangle$-Q offers many important advantages including the nature of its output signals which is represented by single-bit (boolean logic signals). Representing signals by bitstream signals (one-bit by sampling time) highly reduce the data-transmission and routing to single wire per each single-bit signal. Secondly, single-bit signals are inherently digital signals and therefore, signal conversion from single-bit signals to their equivalent digital signals to interface with digital signal processor is not needed any more. Thirdly, the single-bit signal processing are not only simpler than conventional Nyquist rate processor but also consumes less energy and hardware resources (logic gates) [15-17]. In the control filed, several papers [18, 19] showed that the $\Sigma\triangle$-Q can effectively be employed to control power drivers directly as a replacement of PWM, which is often the case in many applications such as DC-DC converters and DC-AC inverters. Recent researches combing conventional PID and generalized proportional integrals (GPI) controllers driven by single-bit signals have been studied in [20-23], respectively. The stability of such control systems has been analyzed using sliding mode theory, and such system has been made feasible in controlling the DC motor.

In this paper, motivated by the above features of using single-bit signal processing, a proposed PI that interface with single-bit signal i.e., using single-bit signal processing technique, is programmed on so called field programmable gate array (generally abbreviated as FPGA) to control a the power flow in typical BIPT system. The single-bit feature of the proposed PI controller helps in reducing the hardware resources (logic elements) in FPGA. In addition, less wire routing and computational complexity is achieved due to absence of multipliers. The paper is presented as follows: Section II introduce the dynamic of typical BIPT system and its control problem. Section III show how the simple system of $\Sigma\triangle$-Q to derive single-bit PI. In the result section, simulation and experimental results of the closed-loop BIPT system are presented shoing the advantages of using $\Sigma\triangle$-Q in the hardware reduction with some conclusions presented in the final part of the paper, Section V.

2. TYPICAL BIPT SUBSYSTEMS

The topology of a typical BIPT is a well-established system and shown in Figure 1. As can be seen, the BIPT allows the the power to flow with no physical contacts from the primary subsystem to secondary subsystem and vice versa. The secondary subsystem of the shown BIPT is connected through H-bridge. When the power flows wirelessly through the air-gap from primary subsystem to pickup subsystem, then primary subsystem acts as an inverter whereas pickup-subsystem acts as a reversible rectifier. Similarly, the primary subsystem behaves as the reversible rectifier and the pickup subsystem operates on inverting mode when the power wirelessly transfers from the pickup subsystem to the primary subsystem. The objective of the primary subsystem converter mainly is to generate a constant track current with high-frequency in windings of the the primary subsystem L_{pt} whereas the main goal of of the pickup converter is to manage and direct the power transmission between both subsystems. Note that both sides of the system , i.e., primary and pickup subsystem comprise inductor-capacitor-inductor LCL resonant networks to track the current generated by the the converter employed in the primary subsystem. Furthermore, the parallel compensation for the BIPT

essentially acts as the energy source with efficiency reach up to 94%[5].

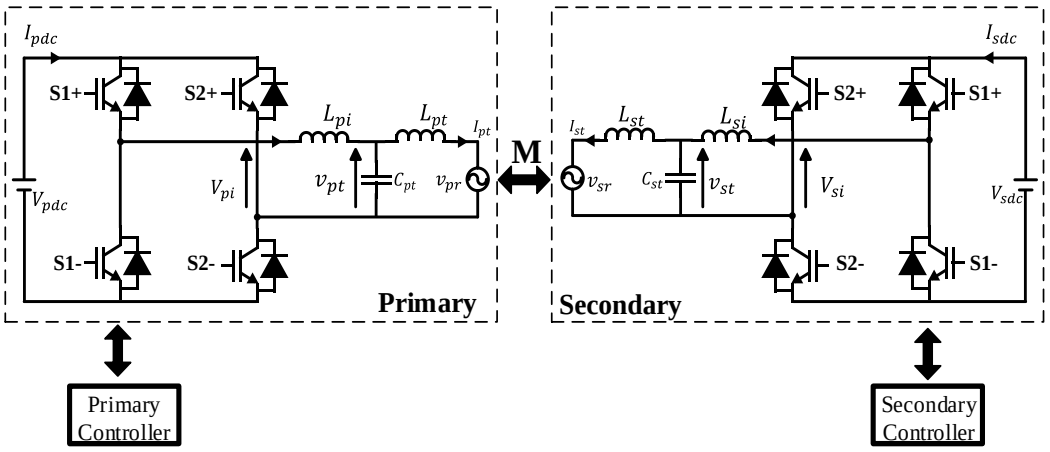

Figure 1. Typical BIPT system

2.1. Operation

The BIPT system illustrated in Figure 1 is to be simplified further using the equivalent circuit in Figure 2. In the equivalent circuit, it is often considered that the primary subsysetm is connected with an AC voltage source to generate sinusoidal voltage $V_{pi}\angle 0$ with ω frequency . Similarly, the pickup converter is considered to be connected with an AC voltage source with a phase angle θ w.r.t the AC voltage source connected with the primary subsystem, which is denoted as $V_{si}\angle 0$. The maximum power transmission between the primary subsystem and secondary subsystem can only be achieved when the phase difference θ equals $\pi/2$, see [24] for more details. In the normal operation, the LCL circuit is tuned to the track frequency ω, such that $L_{pi} = L_{pt}$ and $L_{si} = L_{st}$. Therefore

$$\omega^2 = \frac{1}{L_{pi}C_{pt}} = \frac{1}{L_{pt}C_{pt}} = \frac{1}{L_{si}C_{st}} = \frac{1}{L_{st}C_{st}} \tag{1}$$

Under these assumptions, the simplified system shown in Figure 2 can be represented by what is called the π model, see Figure 3. The shown π model can be utilized to mainly determine and accordingly control and the track current I_{pt} in primary subsystem and the input current I_{si} in the the pickup subsystem. Both currents are expressed as:

$$I_{pt} = -j\frac{V_{pi}}{\omega L_{pt}} \tag{2}$$

$$I_{si} = -j\frac{j\omega M I_p t}{\omega L_p t} = -j\frac{MV_{pi}}{\omega L_{pt}L_{st}} \tag{3}$$

in which M denotes the mutual inductance between the the track coils inductance L_{pt} and pickup inductance L_{st}, given by

$$M = k\sqrt{L_{pt}L_{st}} \tag{4}$$

where k denotes coefficient of the coupling in the BIPT considered in this paper. It is also known that the converter in the pickup subsystem generates power expressed by

$$P_{si} = \mathcal{R}\left\{V_{si} \times I_{si}\right\} = -\frac{MV_{pi}\left|V_{si}\right|}{\omega L_{pt}L_{st}}\sin\left(\theta\right) \tag{5}$$

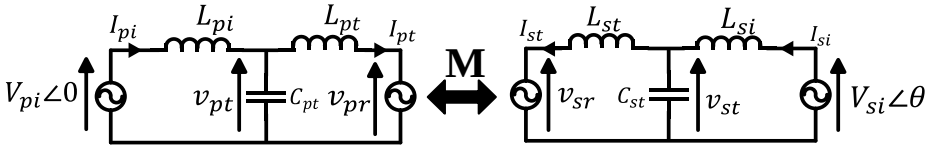

Figure 2. Simplified equivalent model of BIPT system

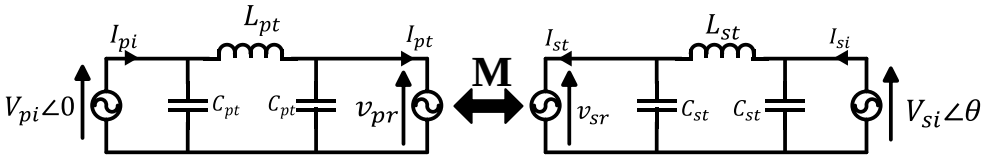

Figure 3. The π model equivalent circuit of the BIPT system

From (5), it implies that the power transmission can can be effectively optimized by controlling the phase angle θ and the output voltage V_{si}. For example, the maximum power can be obtained if the phase θ equals $\pm 90^{\circ}$. This means that the pickup subsystem is functioning at power factor (PF) equals 1. For BIPT systems, when θ equals 90°, then the power is transferring from the pickup subsystem to primary subsystem, and if θ equals -90°, then the BIPT opertaes in the reverse mode, i.e., power is transferring from the primary subsystem to the pickup subsystem, See [5] for more details. Thus, the output power in (5) is optimised by directed by controlling the phase difference between the primary subsystem and the secondary subsystem in which

$$V_{pi} = \frac{4}{\pi\sqrt{2}} V_{pdc} \sin\left(\frac{\pi D}{2}\right) = \frac{4}{\pi\sqrt{2}} V_{pdc} \sin\left(\frac{\alpha_p}{2}\right) \tag{6}$$

$$V_{si} = \frac{4}{\pi\sqrt{2}} V_{sdc} \sin\left(\frac{\pi D}{2}\right) = \frac{4}{\pi\sqrt{2}} V_{sdc} \sin\left(\frac{\alpha_s}{2}\right) \tag{7}$$

with D denotes the duty cycle of $D = \alpha_p/\pi = \alpha_s/\pi$.

Consider (6) and (7), by substitute both equations into (5), the output power from the primary susbsystem to the pickup subsystem can be measured by the following equation:

$$P_{si} = -\frac{8MV_{pdc}V_{sdc}}{\omega\pi^2 L_{pt}L_{st}} \sin\left(\frac{\alpha_p}{2}\right) \sin\left(\frac{\alpha_s}{2}\right) \sin(\theta) \tag{8}$$

in which α_p denotes the phase shift between the two converter on/off signals connected to the H-bridge in primary subsystem. Similarly, α_s denotes the phase shift between the two converter on/off signals connected to H-bridge in the pickup subsystem. Consider both (5) and (8), controlling converter in the pickup subsystem and accordingly output voltage V_{si} is to be used to regulate (control) the lead/lag phase difference between on/off signals that used to switch two legs of the converter. Therefore, the main objective of the proposed controllers in BIPT is to effectively control the phase difference between the on/off signals to optimally control of the power transmission between the two subsystems.

2.2. Control algorithm for BIPT

The control algorithms for the considered BIPT systems can be designed to control the duty cycle to control switch of the H-bridge [4, 24, 25] and the phase control [5, 3]. The controllers for both control problems are mainly known by 1) the controller connected to the primary subsystem and 2) the controller connected to a feedback pickup subsystem. The controller for the duty cycle is basically designed for the open

loop primary control subsystem and the same switch signals are used to the same H-bridge connected to the pickup subsystem controller but without a feedback loop [24]. This section illustrates the control design for duty cycle of the pickup subsystem controller.

The problem of designing controller for the duty cycle basically starts from considering (8). Thus, the control laws can be obtained by effectively controlling the phase shift α_s between two switches S_1 and S_2 of the converters in pickup subsystem. Indeed, changing the duty cycle of the switching signals connected to the converter directly changes output voltage and accordingly control the power transferring from the primary subsystem to the pickup subsystem in return. The phase delay θ between the primary subsystem and pickup subsystem is fixed at either $\pm 90^\circ$ based on the desired direction of the power transferring. The controller for primary subsystem should be designed to control the phase shift α_p in order to sustain a constant sinusoidal track current. However, to reduce the distortion of the harmonics at the minimum, the phase shift is fixed to $\alpha_p = 120^\circ$.

Figure 4 illustrates controller schematic designed for the duty cycle. Since we used a FPGA for our controller design, the all the input signals must be converted to digital signals. Therefore, we used A/D to convert the continuous-time input voltage and current connected to the pickup subsystem to digital signal. Next, both digital signals (voltage and current) are multiplied by each other to get the power value. The measured input power will be compared by the reference signal (desired) and the results (error) will be by the controller to generate control signal. A phase locked loop (PLL) is effectively designed as a clock that generated by FPGA and utilized for system synchronization by measuring the phase of the output voltage of the primary subsystem. The phase shift α_s between the two switches S_1 and S_2 of the converter connected to the pickup subsystem changes between $\pm 180^\circ$, in which 180° gives in the optimal power transfer in forward direction; and -180° gives in the optimal power transfer in the other direction.

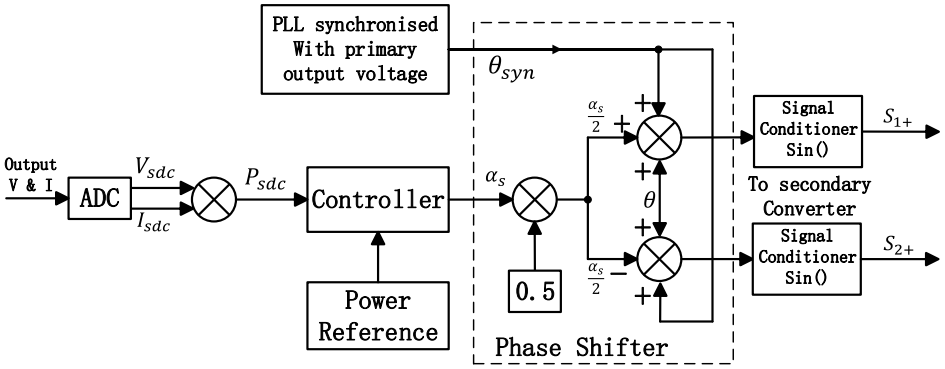

Figure 4. Control schematic for the duty cycle

3. SINGLE-BIT BASED CONTROLLER

Single-bit based control design, which uses $\Sigma\triangle$-Q significantly contributes in the reduction of the routing area and hardware resources (logic elements consumption) since there is no multiplier needed to design the controller. This section presents the concept of single-bit signals generated by $\Sigma\triangle$-Q, and the design of single-bit based proportional and integral controller for BIPT system.

3.1. Single-bit signal and $\Sigma\triangle$-Q

The single-bit signal is switching signal which represented by ON or OFF quanta denoted by $+Q$ and $-Q$. It could also represents any bipolar time domain signal. The single-bit signals are generated by various types of two-level quantizers including $\Sigma\triangle$-Q, which converts its input signals to switching signals (called here single-bit) signal. Figure 5 illustrates a typical first order $\Sigma\triangle$-Q. The dark line shows the input signal to be converted to single bit signals (dotted line). As can be seen, the output of the quantizer is expressed by

$$\delta_k = \frac{1}{2}\left(1 + \operatorname{sgn}\left(s_k\right)\right) = \begin{cases} 1 & \forall\, s_k \geq 0 \\ 0 & \forall\, s_k < 0 \end{cases} \tag{9}$$

since $\mathrm{sgn}\,(s_k) = \begin{cases} +1 & \forall\, s_k \geq 0 \\ -1 & \forall\, s_k < 0 \end{cases}$. The quantizer sensitivity is represented here by Q. [15]. See the BIPT system in Figure 1. As mentioned earlier, the steady state error is the difference between the measured power and the desired power, i.e.,

$$e = P_{ref} - P_{sdc}$$

in which P_{ref} and P_{sdc} denote the desired and measured power of the pickup subsystem, respectively. The get an optimal performance and guarantee stability of both $\Sigma\triangle$-Q and BIPT system, the quantizer gain Q should be carefully set larger than input signals to be converted, in our case e. The condition can be written as $|e| \leq Q$. However, the value of Q should selected as close to the maximum value of e as much possible as we can to avoid unnecessary quantization noise during quantisation process [21]. Optimally, Q should be set just equal the maximum boundary of e.

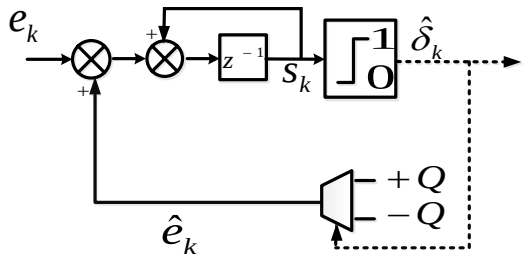

Figure 5. Delat-sigma quantizer

3.2. Single-bit based controller

The controller schematic driven by single-bit can be designed using either single-bit blocks with input/output single-bit signals or recently hybrid PI controller [15]. Employing several single-bit blocks to execute any mathematical operations requires many $\Sigma\triangle$-Qs (double number of the blocks) and thus, requires very careful deign process in selecting the proper Q values used in each block. As any quantizer, $\Sigma\triangle$-Qs introduce quantization noise and therefore, the proportional and the integral using single-bit blocks have to be carefully designed in order to minimize the quantization noise. For this reason, the hybrid single-bit PI, which is proposed to control BIPT system, is given by

$$\hat{u}_k \quad = \quad Qk_p \mathrm{sgn}\,(s_k) + k_i Q \int_t \mathrm{sgn}\,(s_k)\, dt \tag{10}$$

where k_p and k_i denote the proportional and integral gains, respectively. The controller driven single-bit based is often designed using input-output interface in boolean logic (on-off) format. In other words, a $\Sigma\triangle$-Q is designed to convert the input signals to single-bit signal which in turn , will be applied to the digital processor to execute the control law, see [15, 17] for more details. In this paper, PI controller embedded with $\Sigma\triangle$-Q is implemented on FPGA. Firs, we convert the continuous-time system into its discrete-time approximation using Euler's discretization method. The discrete-time transformation of (10) shown in Figure 6, is expressed by $\hat{u}_k = \hat{u}_k^p + \hat{u}_k^i$ in which

$$\hat{u}_k^p = \begin{cases} K_{Up} = +Qk_p & \forall\, \hat{\delta}_k = 1 \\ K_{Lp} = -Qk_p & \forall\, \hat{\delta}_k = 0 \end{cases}$$

and

$$\hat{u}_k^i = \begin{cases} K_{Ui}\rho^{-1} & \forall\, \hat{\delta}_k = 1 \\ K_{Li}\rho^{-1} & \forall\, \hat{\delta}_k = 0 \end{cases}$$

with $\rho = z - 1$ and $K_{Ui} = QT_s k_i$, $K_{Li} = -QT_s k_i$, T_s denote the sampling period. The dark line is the conventional signal whereas the thin line represents the single-bits signal, see [15].

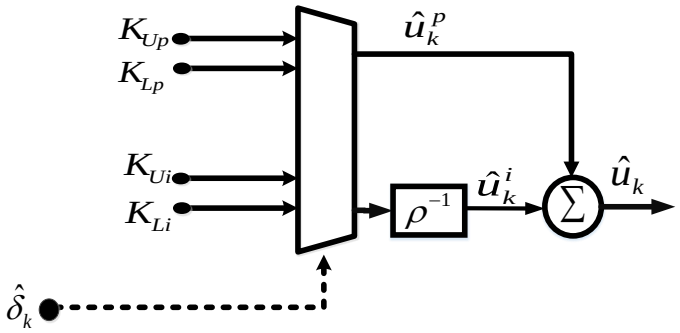

Figure 6. Hybrid single-bit PI

4. SIMULATION AND EXPERIMENTAL RESULTS

To investigate the performance of the proposed controller driven by single-bit, the controller is designed and used to effectivley control the power transferring in a BIPT system . The validation and verification are carried out though simulations and experiment. Since the PI control strategy had a good performance in simulations, the single-bit controller would use PI format, too. The system parameters of bidirectional IPT system is given in Table 1.

Table 1. Parameters of experimental prototype

Symbol	Value and SI unit	Symbol	Value and SI unit
V_{dc}	$125V$	C_T	$2.48\mu F$
L_{pi}	$46.68\mu H$	C_s	$2.47\mu F$
L_T	$22.66\mu H$	M	$8\mu H$
L_{si}	$23.45\mu H$	R_{pi}	0.0163Ω
L_{so}	$46.5\mu H$	R_T	0.0159Ω
C_{pi}	$2.53\mu F$	R_{si}	0.0166Ω
C_{so}	$2.53\mu F$	R_{so}	0.0155Ω

4.1. Simulation

The main objective of this work is to replace the conventional PI by the a PI controller driven by single-bit signals. For BIPT, the designed controller will be used mainly to control duty cycle which will result in modifying the phase difference between converter switches. Thus, the single-bit signal should switch with constant frequency. Since $\Sigma\triangle$-Q generates single-bit signals with variable frequencies, then these signals can be used to drive the BIPT converters. Therefore, $\Sigma\triangle$-Q is replaced with conventional PWM for this purpose. As can be seen in Figure 6, the control signal is conventional signal to be converted through PWM in order derive H-bridge switches.

Figure 7 compares the performances of PI controller drive by single-bit signals and the conventional PI controller. Both controllers were used to control and direct the power transferring in both forward and reverse modes. It is very clear that PI controller with the single-bit signal interface can be used as a replacement for the conventional PI controller for the power flow between the BIPT subsystem. It is also evident that there is oscillations in the transferred power when the BIPT is operated at steady-state. At high power rating, the oscillations is acceptable in single-bit PI in comparison with conventional PI controller. However, it is noted that as the magnitude of the power transferred between the primary and backup subsystem becomes less, the amplitude of oscillations increases. The oscillations are obviously caused by the quantization noise generated by $\Sigma\triangle$-Q. In this experiment, the quantizer gain Q was set to 1210 which is obviously, large enough Q to introduce more noise to the system at lower power ratings. To partially mitigate the high oscillation and improve the performance, simulations with variable Q numbers (fine Q settings) were carried out in the literature, see [26].

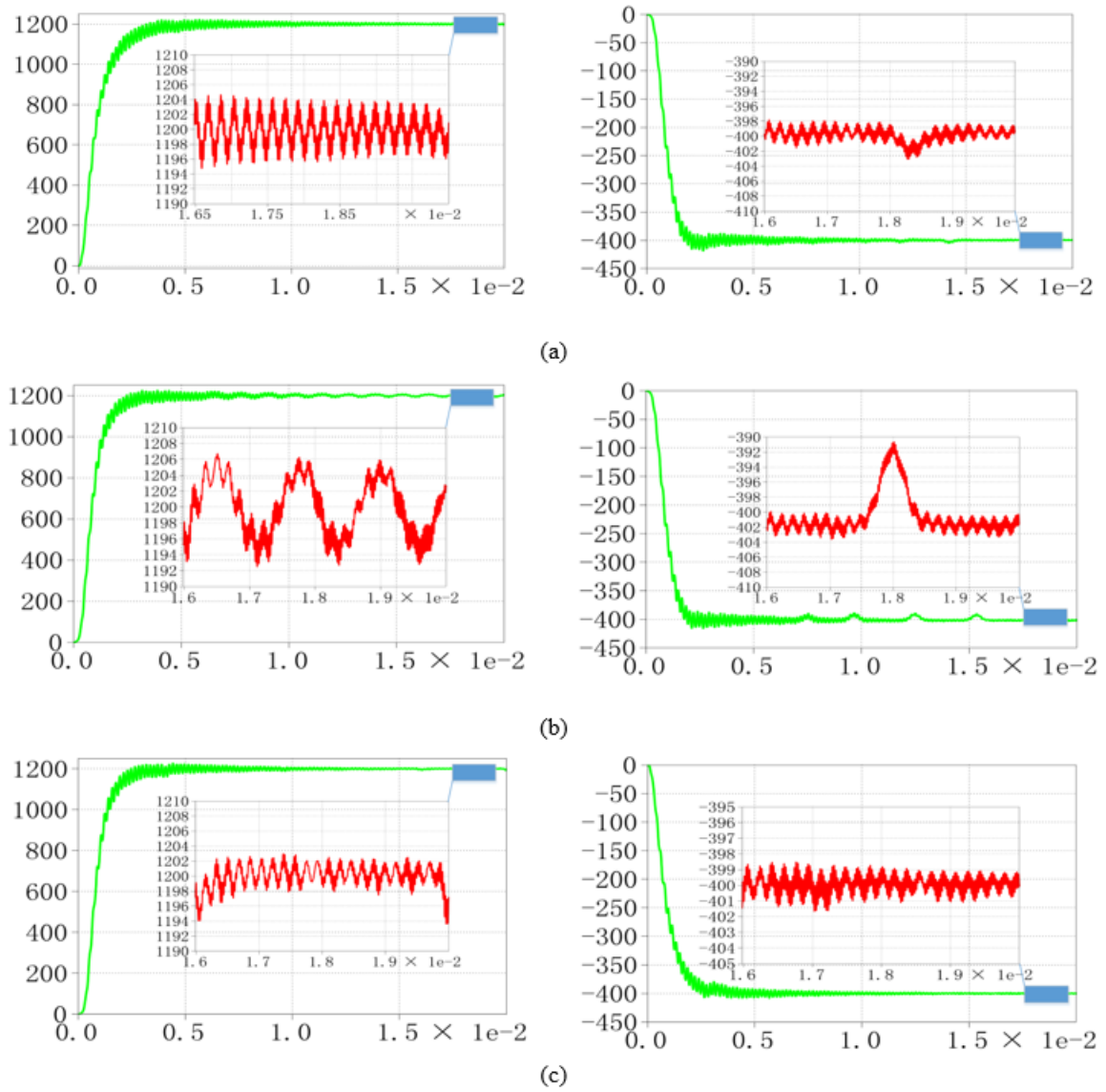

Figure 7. The performances of power flow control using, (a) Conventional PI, (b) single-bit based PI with fixed Q and (c) single-bit based PI with variable Q.

In this work, the PI controller is programmed using DE0-nano FPGA. Table 2 shows FPGA hardware consumption for both; the conventional PI controller and the PI controller embedded with $\Sigma\triangle$-Q. The consumption of hardware resources by the PI controller embedded with $\Sigma\triangle$-Q are 586 LEs and 154 dedicated Logic Registers (LRs). IHowever, the conventional PI controller consumes 1302 LEs, 182 dedicated LEs and 24 9-bit multipliers. It is evident that the single-bit based PI controller dramatically reduces hardware resources, routing and no multipliers needed by the processor.

Table 2. Hardware resources consumption

Hardware Resources	Conventional PI	Bitstream based PI
Multipliers	2	0
Multiplexers	0	2
DSP - Logic Elements	1302	586
Registers	182	154
DSP 9×9	24	0

5. CONCLUSION

In this paper, a new PI schematic with $\Sigma\triangle$-Q has been designed and tested on a prototype BIPT system. The usefulness of this PI has been verified in both simulation and HIL environment. With a proper design, the proposed controller achieve a good performances in comparison with conventional PI controller. The single-bit signals representation and multiplier-less schematic significantly simplified the design of the controller on hardware level. The compilation reports generated by FPGA software has showed a dramatic reduction in hardware resources that consumed by PI controller embedded with $\Sigma\triangle$-Q.

REFERENCES

[1] C. M. N. Mukundan, P. Jayaprakash, U. Subramaniam and D. J. Almakhles, "Binary hybrid multilevel inverter-based grid integrated solar energy conversion system with damped SOGI control," *IEEE Access*, vol. 8, pp. 37214-37228, 2020.

[2] U. K. Madawala, P. Schweizer and V. V. Haerri, ""Living and mobility"- a novel multipurpose in-house grid interface with plug in hybrid blueangle," in *2008 IEEE International Conference on Sustainable Energy Technologies*, pp. 531-536, 2008.

[3] U. K. Madawala and D. J. Thrimawithana, "Current sourced bi-directional inductive power transfer system," *IET Power Electronics*, vol. 4, no. 4, pp. 471-480, 2011.

[4] A. K. Swain, M. J. Neath, U. K. Madawala and D. J. Thrimawithana, "A dynamic multivariable state-space model for bidirectional inductive power transfer systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4772-4780, 2012.

[5] U. K. Madawala and D. J. Thrimawithana, "A bidirectional inductive power interface for electric vehicles in V2G systems," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4789-4796, Oct 2011.

[6] J. Dai and D. C. Ludois, "A survey of wireless power transfer and a critical comparison of inductive and capacitive coupling for small gap applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6017-6029, Nov 2015.

[7] K. I. Woo, H. S. Park, Y. H. Cho and K. H. Kim, "Contactless energy transmission system for linear servo motor," *IEEE Transactions on Magnetics,* vol. 41, no. 5, pp. 1596-1599, May 2005.

[8] P. Sergeant and A. V. D. Bossche, "Inductive coupler for contactless power transmission," *IET Electric Power Applications,* vol. 2, no. 1, pp. 1-7, Jan 2008.

[9] E. Monmasson and M. N. Cirstea, "FPGA design methodology for industrial control systems," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 4, pp. 1824-1842, Aug. 2007.

[10] P. S. B. Nascimento, H. E. P. de Souza, F. A. S. Neves and L. R. Limongi, "FPGA implementation of the generalized delayed signal cancelation-phase locked loop method for detecting harmonic sequence components in three-phase signals," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 2, pp. 645-658, Feb. 2013.

[11] D. A. Johns and D. M. Lewis, " Design and analysis of delta-sigma based IIR filters," *IEEE Trans Circuits Systems II, Analog Digit Signal,* vol. 40, no. 4, pp. 233-240, Apr. 1993.

[12] M. K. Kurosawa, M. Kawakami, K. Tojoj and T. Katagiri, "Single-bit digital signal processing for current control of brushless DC motor," *Proceedings of the 2002 IEEE International Symposium on,* vol. 140, no. 3, pp. 589-594, Mar. 2002.

[13] Tianjian Li and Y. Fujimoto. "Control system with high-speed and real-time communication links," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 4, pp. 1548-1557, Apr. 2008.

[14] Weibo Li, Y. Niimi, Y. Orino, S. Hirata and M. K. Kurosawa. "A frequency synchronization method for a self-oscillating PWM signal generator," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 61, no. 4, pp. 244-248, Apr. 2014.

[15] D. Almakhles, A. Swain and N. Patel, "Stability and performance analysis of bit-stream-based feedback control systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4319-4327, July 2015.

[16] X. Wu, V. A. Chouliaras, J. L. Nunez-Yanez and R. M. Goodall, "A novel $\Delta\Sigma$ control system processor and its VLSI implementation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 16, no. 3, pp. 217-228, March 2008.

[17] N. Patel, S. Nguang, G. Coghill and A. Swain, "Online implementation of servo controllers using bit-streams," *TENCON 2005 2005 IEEE Region 10,* pp. 1-6, Nov 2005.

[18] J. B. B. Bradshaw, U. Madawala and N. Patel, "Techniques for conditioning bit-stream signals for single-phase power electronics applications," *IEEE Transactions on Power Electronics,* vol. 27, no. 3, pp. 1414-1423, March 2012.
[19] N. Patel and U. Madawala, "A bit-stream-based PWM technique for variable frequency sinewave generation," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 7, pp. 2530-2539, July 2009.
[20] D. Al-Makhles, A. Swain, and N. Patel, "Delta-sigma based bit-stream controller for a d.c. motor," *TENCON 2012 - 2012 IEEE Region 10 Conference,* pp. 1-5, nov. 2012.
[21] D. Al-Makhles, N. Patel and A. Swain, "Bit-stream control system: Stability and experimental application," *Applied Electronics (AE), 2013 International Conference on,* pp. 1-6, Sept 2013.
[22] D. Almakhles, A. Swain, A. Nasiri and N. Patel, "An adaptive two-level quantizer for networked control systems," *IEEE Transactions on Control Systems Technology*, vol. 25, no. 3, pp. 1084-1091, May 2017.
[23] D. J. Almakhles, R. Sakthivel, A. Swain, U. Subramaniam and K. Almustafa, "A generalized one-bit control system using a $\Delta\Sigma$ -Quantizer," *IEEE Access*, vol. 7, pp. 117009-117018, 2019.
[24] M. J. Neath, A. K. Swain, U. K. Madawala and D. J. Thrimawithana, "An optimal pid controller for a bidirectional inductive power transfer system using multiobjective genetic algorithm," *IEEE Transactions on Power Electronics,* vol. 29, no. 3, pp. 1523–1531, March 2014.
[25] U. K. Madawala, M. Neath and D. J. Thrimawithana, "A power-frequency controller for bidirectional inductive power transfer systems," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 1, pp. 310-317, Jan 2013.
[26] D. Al-Makhles, A. K. Swain and N. Patel, "Adaptive quantizer for networked control system," *European Control Conference (ECC),* pp. 1404-1409, June 2014.