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A new space vector modulation technique for quasi Z-source B4 inverter

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ABSTRACT

A Quasi Z-Source (qZS) network has been utilized in a B4 inverter topology to provide voltage boosting effect by turning on the upper and lower switches simultaneously which is known as zero shoot-through states. However, the design of a qZS B4 inverter is not as straightforward as adding a qZS LC impedance network to the front-end of a B4 inverter. This is because there are no zero vectors available in a B4 inverter topology to insert the shoot through zero states, as in the case of a B6 inverter. This paper proposes a new Space Vector Modulation (SVM) technique for a qZS B4 inverter. Additional zero vectors have been appropriately added and distributed in the proposed SVM to avoid altering the existing volt-sec per switching cycle for the existing active vectors. The voltage vectors switching placement is carefully designed in order to enable the voltage boosting effect for this topology without altering the initial output voltage. In addition, an approach to compensate the DC-link voltage ripple has also been taken into consideration in its initial calculation to achieve balanced output voltage. The performance of the proposed modulation technique is verified using MATLAB/Simulink. It is shown that by using the proposed modulation technique, there is an overall improvement on the line to line output voltage where by it is able to produce balanced output voltages for the three-phase loads with or without boosting effect.

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1. INTRODUCTION

Over the years, various voltage source inverters (VSI) topologies have been proposed depending on industrial needs and applications. Even though the conventional six-switch three-phase (B6) VSI is broadly used, the use of reduced count switch topologies is considered in specific low power range applications to reduce cost and power losses. To accomplish that, the four-switch three-phase (B4) inverter has been proposed in [1]. Despite its advantages, the B4 inverter has several significant drawbacks. Literature studies state that the B4 inverter produces periodical fluctuations across the DC-link split capacitors [2-7]. A large DC-link capacitor is typically used to compensate the DC-link ripple, and this can be quite bulky. Thus, it is vital to compensate for the influence of the DC-link ripple on the output voltage without the expense of using large DC-link capacitors. Various modulation techniques using switching time compensations have been proposed to compensate for the voltage imbalance split capacitor [2-4, 8-10]. Furthermore, compared to a B6 inverter, it is noted that zero vectors are absent for a B4 inverter with only four available active vectors.

Hence, numerous approaches regarding zero vectors integration in a space vector pulse-width modulation (SVM) technique have been proposed to solve for the absence of zero vectors in B4 inverters [6, 11-13].

Apart from that, in any concept of standard VSI operation, the B4 or B6 inverters can only perform buck operation. Thus, the most straightforward solution is to use a DC-DC converter to boost the output voltage from the DC source. Nevertheless, by using this approach, it defeats the purpose of reducing power losses since active switches are needed in a DC-DC boost converter. Hence, an impedance network inverter has been proposed [14] as an alternative to the traditional DC-DC converter. It removes the active control switches and provides the voltage buck-boost capability by turning on the lower and upper switches simultaneously (shoot-through time). A Z-Source (ZS) and quasi Z-Source (qZS) inverter is one of the impedance network topologies. Several B4 inverters that utilize a ZS/qZS topology to boost the output voltage has been reported in [3, 9, 11, 15]. A detailed analysis on the ZS B4 inverter modulation technique has been presented in [11], where it discusses the process of zero vectors synthesis since theoretically for a B4 inverter; the zero vectors are absent. Consequently, the placement of shoot-through time has been established, based on the availability of zero vectors depending on the various possible B4-ZS inverter topologies[11]. Similar to a conventional ZS/qZS B6 inverter; a zero vector is needed to insert a shoot-through zero condition and subsequently provide a boosting effect on the output voltage [14]. Hence, it is vital to consider the concept of neutralization of active vectors in order to produce zero vectors. However, in [11], the DC-link voltage ripple has been assumed constant, and the current circulation through the two split DC-link is not considered. Therefore, to compensate for the split DC-link voltage imbalance, adaptive SVM techniques have been proposed in [3, 9]. However, the focus of these techniques is just to compensate the switching time in order to solve the DC-link voltage ripple issue without appropriately considering the zero vectors switching time distributions in its proposed algorithm. This paper proposes a new SVM technique for the qZS B4 inverter, which can provide DC-link ripple compensation through zero vector synthesis approach. It presents an investigation on the principle of the qZS B4 inverter along with the proposed SVM technique which introduces zero vectors that can accommodate the shoot-through zero states and at the same time provide the DC-link voltage ripple compensation. The accuracy of the proposed algorithm for the SVM is confirmed by analyzing the results of a simulation study conducted using MATLAB/Simulink.

2. NEW MODULATION TECHNIQUE FOR QZS B4 INVERTER

Figure 1 shows the qZS-B4 inverter, as proposed in [3]. It uses only four active switches to control a three-phase load instead of six. The one phase leg (phase A) of the load is connected to the midpoint of two split capacitors, while the four switches are controlling another two-phase leg (phase B and C). The proposed structure in [3] utilises shoot-through zero interval times to buck the DC-bus voltage, like a standard qZS three-phase six-switch (B6) inverter operation. Hence, it provides the desirable output voltage across the load by turning on the lower and upper switches simultaneously [3].

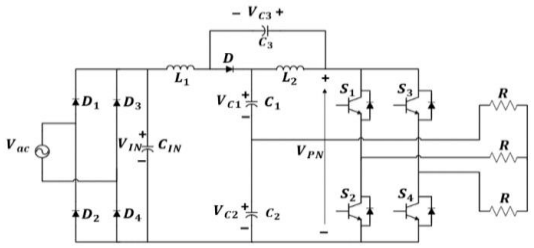

Figure 1. Quasi Z-source B4 inverter topology [2]

Conceptually for a qZS inverter structure, to measure the output voltage of the inverter bridge, it is essential to consider the peak DC-link voltage, V_{PN}. Therefore, the main required equations for a qZS B4 inverter are [3]:

$$V_{PN} = S_D \cdot \frac{1}{1-2D} \cdot V_{IN} \quad (1)$$
$$V_{C1} + V_{C2} = \frac{1-D}{1-2D} \cdot V_{IN}$$
$$V_{C3} = \frac{D}{1-2D} \cdot V_{IN}$$

$$V_{C_{eq}} = V_{C1} + V_{C2}$$
$$V_{C_{eq}} = V_1 + V_2 = (1 - D) \cdot V_{PN}$$
$$V_{PN} = \left(\frac{V_1 + V_2}{1 - D}\right)$$

Where S_D represents the inverter bridge equivalent circuit state condition. When the inverter is in short circuit condition (shoot-through zero mode), S_D is equal to zero, whereas it will become 1 when the inverter bridge is in the active state (shoot-through mode). Consequently, the shoot-through duration, D can be expressed as in [14].

$$D = \frac{T_0}{T_s} \quad (2)$$

Where

T_0 is the zero shoot-through switching time

T_s is the switching time

Considering the DC-link voltage ripple that generally occurs in a B4 inverter, it is crucial to take into account the voltage across the split capacitor ($V_{C1} + V_{C2}$) since the output voltage of phase "A" is defined byV_{C2}. The feasible voltage potentials v_{a0}, v_{b0} and v_{c0} show that the influence of voltage variations in the split capacitor has been taken into consideration. Thus, this can be used to calculate phase voltages V_{an}, V_{bn} and V_{cn} based on equations [2, 3, 16] .

$$V_{C1} = V_1$$
$$V_{C2} = V_2$$
$$V_{a0} = V_2$$
$$V_{b0} = S_1 \cdot \left(\frac{V_1 + V_2}{1 - D}\right) \quad (3)$$
$$V_{c0} = S_3 \cdot \left(\frac{V_1 + V_2}{1 - D}\right)$$

Where

V_{a0}, V_{b0}, V_{c0} are the voltage potentials across each phase respectively.

The formation of the average voltage vector V_s can be obtained by adding the five voltage vectors from the bridge inverter. This can be achieved by using Clark's transformation, where the components value of $\alpha\beta$ and the five voltage vectors are shown in the following equation [17].

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad (4)$$

$V_i = (v_\alpha + jv_\beta), i =$ 00,10,01,11, Z_{sht}

The details of the output voltage based on each voltage vector are tabulated in Table 1. The existence of the parameter V_2 illustrates the influence of voltage variations in the split capacitors on all the space vectors. Even though voltage variations have been considered in the SVM technique for a qZS B4 inverter proposed in [3], the variation in the duty cycle, D is not included in the voltage vector calculation. Thus, Table 2 presents the space vector positions that considers the variation in D and V_{C2}.

Table 1. Proposed switching vectors and the output voltages for the qZS B4 inverter

Vector				Output Voltage		
S1	S2	S3	S4	V_{an}	V_{bn}	V_{cn}
0	0	0	0	$\frac{2V_2}{3}$	$-\frac{V_2}{3}$	$-\frac{V_2}{3}$
1	0	0	1	$\frac{V_2 - V_1 - 2V_2D}{3(1-D)}$	$\frac{V_2 + 2V_1 + V_2D}{3(1-D)}$	$\frac{-2V_2 - V_1 + V_2D}{3(1-D)}$
1	1	0	0	$\frac{-2V_1 - 2V_2D}{3(1-D)}$	$\frac{V_1 + V_2D}{3(1-D)}$	$\frac{V_1 + V_2D}{3(1-D)}$
0	1	1	0	$\frac{V_2 - V_1 - 2V_2D}{3(1-D)}$	$\frac{-2V_2 - V_1 + V_2D}{3(1-D)}$	$\frac{V_2 + 2V_1 + V_2D}{3(1-D)}$
1	1	1	1	$\frac{2V_2}{3}$	$-\frac{V_2}{3}$	$-\frac{V_2}{3}$

Table 2. Proposed Switching Size of Vectors for the qZS B4 Inverter

Vector	V_α	V_β
00	$\frac{2V_2}{3}$	0
10	$\frac{V_2 - V_1 - 2V_2D}{3(1-D)}$	$\frac{V_2 + V_1}{\sqrt{3}(1-D)}$
11	$\frac{2(V_1 + V_2D)}{3(1-D)}$	0
01	$\frac{V_2 - V_1 - 2V_2D}{3(1-D)}$	$\frac{-(V_2 + V_1)}{\sqrt{3}(1-D)}$
Zsht	$\frac{2V_2}{3}$	0

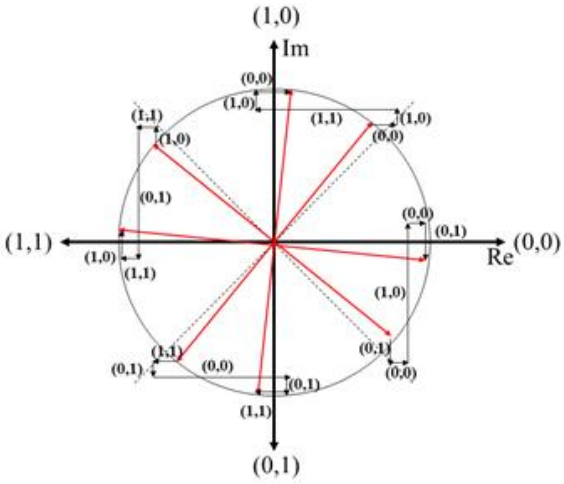

Figure 2. Switching vectors distribution and chosen vector sequences

Table 3. Proposed voltage vector switching time for sector 1 and 2

Sector	$1(-\frac{\pi}{4} \le \theta < \frac{\pi}{4})$	$2(\frac{\pi}{4} \le \theta < 3\frac{\pi}{4})$
t_{00}	$\frac{V_1 - (1-D)V_2}{V_1 + V_2} T_S + 3K\cos(\theta) - tsh$	$\frac{V_1 + V_2D}{V_1 + V_2} T_S - \sqrt{3}K\cos(\theta - \frac{\pi}{3}) - tsh$
t_{10}	$\frac{(1-D)V_2}{V_1 + V_2} T_S - \sqrt{3}KT_sV_s\cos(\theta + \frac{\pi}{6})$	$\sqrt{3}K\cos(\theta)$
t_{11}	0	$\frac{(1-D)V_2}{V_1 + V_2} T_S - \sqrt{3}K\cos(\theta + \frac{\pi}{3})$
t_{01}	$\frac{(1-D)V_2}{V_1 + V_2} T_S - \sqrt{3}K\cos(\theta - \frac{\pi}{6})$	0

Table 4. Proposed voltage vector switching time for sector 3 and 4

Sector	$3(3\frac{\pi}{4} \le \theta < 5\frac{\pi}{4})$	$4(5\frac{\pi}{4} \le \theta < -\frac{\pi}{4})$
t_{00}	0	$\frac{V_1 + V_2D}{V_1 + V_2} T_S - \sqrt{3}K\cos(\theta + \frac{\pi}{3}) - tsh$
t_{10}	$\frac{V_1 + V_2D}{V_1 + V_2} T_S - \sqrt{3}K\cos(\theta - \frac{\pi}{6}) - tsh$	0
t_{11}	$\frac{V_2 - V_1 - 2V_2D}{V_1 + V_2} T_S - 3K\cos(\theta) + tsh$	$\frac{V_2 - V_2D}{V_1 + V_2} T_S - \sqrt{3}K\cos(\theta - \frac{\pi}{3})$
t_{01}	$\frac{V_1 + V_2D}{V_1 + V_2} T_S - \sqrt{3}K\cos(\theta + \frac{\pi}{6}) - tsh$	$\sqrt{3}K\cos(\theta)$

Furthermore, to estimate the desired reference waveform, it is necessary to design the proper switching states to modulate the output pulses. Therefore, to obtain the desired reference voltage vector, V_s the inverter needs to be switched between active adjacent states over a constant switching period. During each switching, only three vectors are used in one sector and the placement of each voltage vector, V_i are supposedly as closest as possible to V_s [2]. Consequently, the switching sequence for the chosen technique is based on Figure 2, where the voltage vector arrangement is in between the centre of sequential voltage vectors. Generally, in a previously proposed modulation technique [2], only two sectors have been used to track the desired voltage vector, V_s. Thus, the point of reference tracking is quite large and could jeopardize the accuracy of obtaining the desired reference waveform where it is possible that the V_i created is far from V_s. The calculated time for each time portions is generally tabulated in Table 3 and Table 4 whereby the t_{sh} value can be obtained by using equation (2).

Where,

t_i timing interval for voltage vector;
V_s average voltage vector;
T_S switching period;

θ voltage vector position.

$K = \frac{(1-D)}{V_1+V_2} T_s V_s$

It is always essential to acknowledge the absence of zero vector in designing the switching sequence of a qZS B4 inverter [6, 9, 11-13, 18]. Similar with the conventional qZS B6 inverter, a zero vector time is needed in a qZS B4 inverter to insert a shoot-through zero condition and correspondingly give a boosting effect on the output voltage [19-21]. Tapping prior knowledge, the four active vectors are placed opposing each other as shown in Figure 3 where (0,1) and (1,0) are pointing in opposite directions vertically while (0,0) and (1,1) are pointing in opposite directions horizontally [3, 6, 11-13, 15]. Therefore, a zero vector is created in each sampling time by using this condition in the proposed SVM technique.

A clearer interpretation of the process of creating zero vector can be depicted from Figure 4. Figure 4(a) shows the initial switching states without any zero vector time interval in sector 1. Referring to the switching states of the upper switches (S1, S3), a zero state interval time is created by using the remaining time portion of the longer (0,0) of state time compared to the (1,1) state time as depicted in Figure 4(b). Consequently, the (0,0) switching state time that is equal to the (1,1) switching state time is used to generate the accurate reference phasor volt-sec. The shoot-through zero is then inserted into the zero state interval time to give a boosting effect on the output voltage, as seen in Figure 4(c). The placement of the shoot-through zero interval is in between the duration of the (0,0) and (1,1) switching states for Sector 1 and Sector 3. While in Sector 2 and Sector 4, the placement of shoot-through zero interval is in between the switching states of (1,0) and (0,1). This will ensure that the volt-sec average per switching cycle for all existing active vectors will remain unaltered.

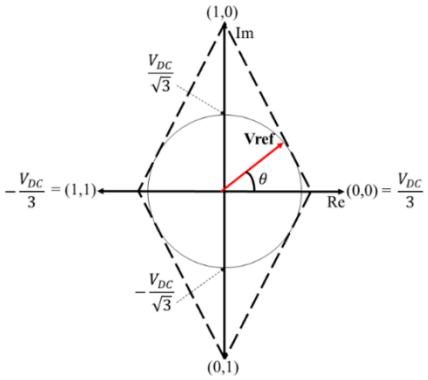

Figure 3. Vectors position on space diagram for B4 inverter

Upper Switches Lower Switches	S1,S3 S2,S4	(1,1) (0,0)	(1,0) (0,1)	(0,0) (1,1)	(0,0) (1,1)	(1,0) (0,1)	(1,1) (0,0)

(a)

Upper Switches Lower Switches	S1,S3 S2,S4	(1,1) (0,0)	(1,0) (0,1)	Zero state	(0,0) (1,1)	(0,0) (1,1)	Zero state	(1,0) (0,1)	(1,1) (0,0)

(b)

Upper Switches Lower Switches	S1,S3 S2,S4	(1,1) (0,0)	(1,0) (0,1)	(1,0) (1,1)	(0,0) (1,1)	(0,0) (1,1)	(1,0) (1,1)	(1,0) (0,1)	(1,1) (0,0)

(c)

Figure 4. The process of creating zero vector time interval, (a) Switching sequence without the zero vector time interval in sector 1, (b) Switching sequence with a *reproduction* of zero vector time interval in sector 1, (c) Shoot-through zero state position in sector 1

3. RESULTS AND ANALYSIS

The circuit configuration as shown in Figure 1 is designed based on the parameters as in Table 5. All parameters are selected based on [21] to achieve the most stable dynamic performance. Simulation work using MATLAB/Simulink has been done to verify the proposed control technique.

To analyze the performance of the proposed SVM technique for the qZS B4 inverter, a comparison is made with [11] where the voltage across the DC-link capacitor is assumed to be equal. It has been proven in [2, 9, 11, 16-18] that both split capacitor voltages are not equally divided. Hence, it is important to consider the value of the voltages across the split capacitor. Initially, the value of the modulation ratio and shoot-through zero is set to M=0.8 and D=0 respectively. By using the proposed SVM technique as observed in Table 3 and Table 4, it is noted that the amplitude of the output voltages is 77 V peak to peak for all line to line voltages V_{ab}, V_{bc} and V_{ca} as shown in Figure 5. This is because the active time for each switch has been calculated and adjusted according to the variations in V_1 and V_2. At this stage, D is set to 0; therefore, there is no boosting effect on the output voltage. From the simulation results, the line to line output voltages are balanced and consequently, less harmonic is reported. Although the output voltages in [3] are reported as symmetrical, the new proposed SVM technique has a smaller load voltage total harmonic distortion (THD) of 1.66% as shown in Figure 6 compared to 1.87% as reported in [3].

To validate the zero voltage vector distribution in the proposed SVM technique, the shoot-through zero duration D is set to 0.2 and M is reduced correspondingly to 0.65 where the buck-boost factor is determined by the correlation value between M and D [14, 22]. Figure 7(a) shows the line to line output voltages without considering the zero voltage vector distribution. By using the SVM technique in [3], when the duty ratio, D is set higher than 0.1, there is a significant voltage offset in the output voltage waveforms of all line to line voltages. The reason is due to the existence of the volt-sec error to the externally connected load where Z_{sht} time duration is inappropriately inserted in every switching time interval. Thus, the allocation time for Z_{sht} time duration is limited. In this case, zero voltage vector distribution has not been considered only in one sector, which is sector 2. However, as observed in Figure 7(a), all the sinusoidal waveforms are affected by the voltage offset. This is because the switching pattern for phases B and C are dependent on a fixed potential of phase A as depicted in Figure 1. By considering the zero-voltage vector distribution as shown in Figure 7(b), a symmetrical switching pattern is obtained when the value of D is varied from 0 to 0.2. The line to line output voltage amplitude boosted to 150 V peak to peak from 77 V peak to peak, which is greater than the initial output voltage pulse amplitude when D=0 as shown in Figure 7(b). Figure 8 shows that the Z_{sht} time duration is inserted at the point where V_{PN} is equal to 0 and proves that the boosting action is implemented [14, 22]. The simulation results have proven that the proposed SVM technique is capable of boosting the output voltage and at the same time manage to balance the voltage output compared to the results presented in [11] where the deviation of the voltage capacitor that occurs at the DC-link input bridge is neglected. Besides that, in contrast with the SVM technique in [3], the qZS B4 inverter is able to have the voltage boosting effect without altering the volt-sec per switching cycle and consequently increased the limitation of duty ratio from 0.1 to 0.2.

Table 5. Design parameter of the circuit

Parameters	Values
Line Frequency, f	50 Hz
Switching Frequency, f_S	10 kHz
qZS split capacitors, C_1, C_2	300 µF
qZS capacitor, C_3	150 µF
qZS inductor, L_1, L_2	100 µH
DC input capacitor, C_{IN}	470 µF
Output Resistor, R	20 Ω

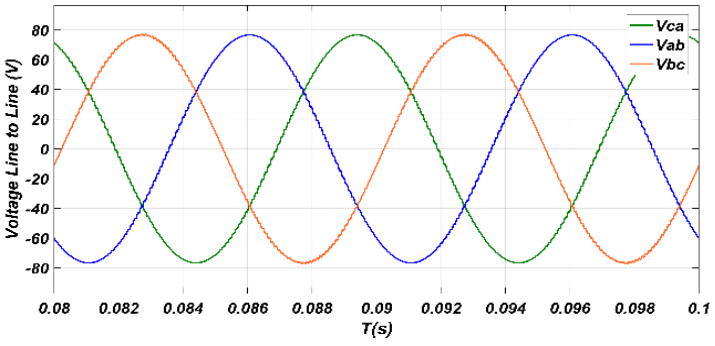

Figure 5. Line to line output voltage waveforms of the qZS B4 inverter with $M = 0.8$ and $D = 0$ using the proposed SVM technique

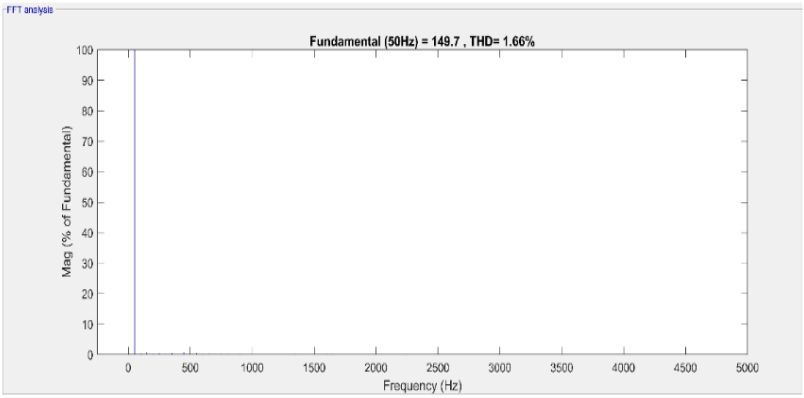

Figure 6. Total harmonic distortion for the line to line output voltage V_{bc} using the proposed SVM technique

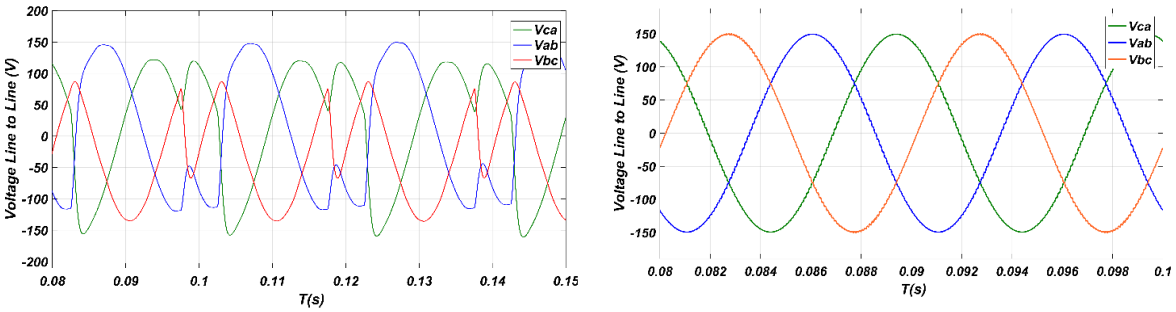

Figure 7. Line to line output voltage waveforms of the qZS B4 inverter with $M = 0.65$ and $D = 0.2$ (a) without zero-voltage vector distribution (b) with zero-voltage vector distribution

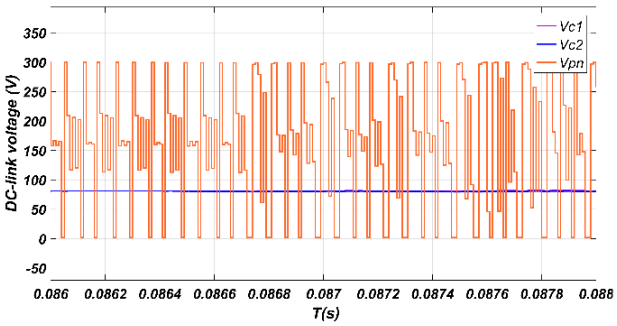

Figure 8. Voltage across the capacitors in the qZS B4 inverter with $M = 0.65$ and $D = 0.2$ using the proposed SVM technique

4. CONCLUSION

This paper has proposed a new SVM technique for a qZS B4 inverter. It offers several advantages when compared to the conventional qZS B4 inverter proposed in [2] and [8]. These advantages include a DC-link ripple compensation and a proper zero-voltage vector distribution for the shoot-through zero-time interval. Theoretical analysis for the proposed SVM technique has been discussed, and the simulation results have proven the theory. It shows that the proposed SVM technique has improved the overall phase output voltage produced by balancing the output voltages for the three-phase loads from a duty cycle of $D = 0$ to $D = 0.2$. An experimental analysis will be carried out next to further confirm the proposed SVM technique.

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