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A new multilevel DC-AC converter topology with reduced switch using multicarrier sinusoidal pulse width modulation

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ABSTRACT

Multilevel converters have a significant role in power processing control in the power system, which has some inherent features like reduced harmonics, high power & medium voltage, reduced voltage stress. In this proposed paper, a novel multilevel inverter with reduced number of switches and without passive components. The proposed inverter generates 15 level output voltage with suitable switching pulse generation using multicarrier sinusoidal pulse width modulation (MSPWM) and different level of voltages are obtained with variation of modulation index. Also coupled inductor is used to minimize the harmonic content and smoothing output current. The scheme which includes different range of unequal voltage sources. As a result, the proposed system it reduces switching control complexity and there is no voltage balancing problem. This paper elucidates the operating modes, voltage stress minimisation and harmonic reduction are discussed. The results of the proposed multilevel dc-ac converter are verified using matlab/simulink. The simulation & hardware results of the proposed inverter were verified using matlab simulink and dsPIC controller respectively, which was analysed with different voltage level and different modulation index.

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1. INTRODUCTION

As a outcome of high technologies growth, the power requirement and quality of power are better than earlier. Because of evolution in power semiconductor devices and power conversion methods [1]. The scheme which is used to transfer DC source to AC source is called inverter. The level of the inverter increases to stabilise the voltage and reduces ripple content [2]. Generally multilevel inverters are used for high power medium voltage applications, by connecting series of power switches with lower voltage dc sources to generate staircase output voltage. Multilevel inverter acts as intermediate device, which transmit power to electrical units like grid system, UPS, FACTS devices, electrical drives and others [3].

Among various multilevel inverter topologies like neutral point clamped, capacitor clamped and cascaded H-bridge, which are mostly prepared standard topologies [4, 5]. The unequal voltage balancing in the DC link capacitors lead to increase of clamping diodes as the voltage level increases, which is limitation of neutral clamped inverter [6]. And in flying capacitor inverter, capacitors act as clamping diodes and it become more complex due number of capacitor and total harmonic distortion increase based on level of inverter. In cascaded H-bridge inverter, the utilisation number of dc source increases, due to that voltage

balancing problem, unequal switching, voltage stress and redundancy phase voltage increases [7]. To reduce the THD of the above conventional multilevel inverters, either switching frequency of the system. But the system outcome leads to increase switching devices, conduction loss and minimise reliability of the system [8].

To overcome the above-mentioned limitations, the research moved towards to generate multilevel output voltage with reduced number of switches. The major objective of work is to increase the voltage level with a smaller number of power semiconductor switches [9]. In multilevel inverter, the ratio of output voltage levels and required power switches is termed as SLR (switch level ratio), which is used to design the minimum switched MLI. The SLR decides the number of switches used, cost of the system and output voltage levels [10]. Cost of system depends, the usage number of switches and passive elements like inductor & large capacitors [11, 12].

Numerous modulation strategies were developed to control converter power switches. In that, the converter with high frequency PWM methods like carrier-based modulation, trapezoidal method, sinusoidal PWM, space vector modulation and multicarrier based PWM used [13-15]. Moreover, selective & active harmonic elimination nearest vector control method and synchronous optimal PWM are used for converter with low frequency PWM techniques [16, 17]. Reduced switches MLIs are predominantly used nearest state control and multicarrier based SPWM schemes [18-20].

In this proposed work, system generates 15 level output voltage with reduced number switches. It provides better features compare conventional schemes like minimised THD, low voltage stress, controlled output current and reduces cost of the system. Power semiconductor switches used in this proposed system is controlled by multicarrier based sinusoidal pulse width modulation, which avoids the shoot through problem. In that section-2 deals about modes of operation of proposed scheme, section- 3 explains about multicarrier SPWM method and section-4 discuss simulation results.

2. POWER STAGE

2.1 Circuit Configuration

Figure 1 shows the proposed novel topology for 15 levels inverter. It consists of three dc source voltages are 10V, 20V & 40V. The MOSFET power switches S1, S2, S3, S4, S5 & S6 connected directly to dc sources, which decide the level output voltage from the proposed scheme. Then switches S7, S8, S9 & S10 performing a VSI bridge circuit, which decides the positive and negative range of output voltage levels with R load is connected across bridge network. The proposed system generates 15 level output voltage with suitable gate pulse generation. Number switches used in this proposed method decided by SLR ratio, which contains totally 10 power switches. Doesn't need of any additional converter like boost converter or any resonant converter to boost voltage or to balance the voltage.

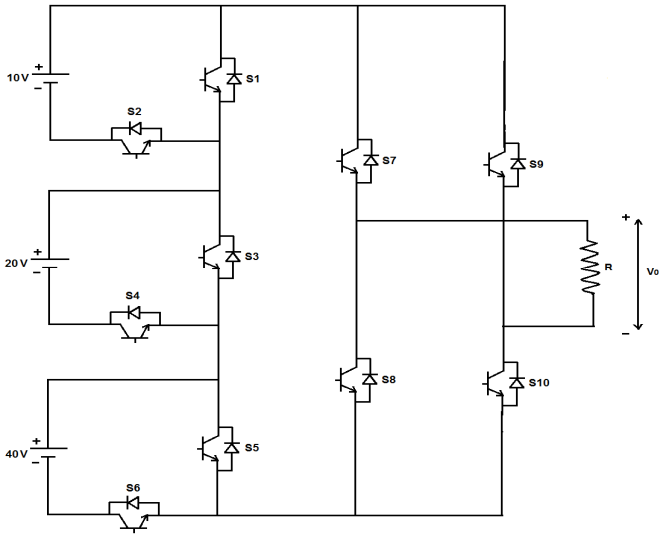


Figure 1. Circuit diagram for 15-level inverter with reduced switches

2.2. Modes of Operation

The proposed system generates 15 level output voltages (+V_{dc}, +6/7 V_{dc}, +5/7 V_{dc}, +4/7 V_{dc}, +3/7 V_{dc}, +2/7 V_{dc}, +1/7 V_{dc}, 0, -1/7 V_{dc}, -2/7 V_{dc}, -3/7 V_{dc}, -4/7 V_{dc}, -5/7 V_{dc}, -6/7 V_{dc}, -V_{dc}) are explained as follows,

1) To obtain output voltage of V_0 = +1/7 V_{dc}, switches S2, S3 & S5 kept ON to get 1/7th voltage from the power circuit and switches S7 & S10 are turned ON to get positive level. Figure 2(a) shows the current flow path for this mode and Table 1 shows various switching combinations for 15 level output voltage.
2) To acquire output voltage of V_0 = +2/7 V_{dc}, switches S1, S4 & S5 kept ON to find 2/7th voltage from the power circuit and from bridge circuit switches S7 & S10 are turned ON to get positive level. Figure 2(b) shows the current flow path for this mode.
3) To attain output voltage of V_0 = +3/7 V_{dc}, switches S2, S4 & S5 kept ON to get 3/7th voltage from the power circuit and from bridge circuit switches S7 & S10 are turned ON to get positive level. Figure 2(c) shows the current flow path for this mode.
4) To achieve output voltage of V_0 = +4/7 V_{dc}, switches S1, S3 & S6 kept ON to get 4/7th voltage from the power circuit and from bridge circuit switches S7 & S10 are turned ON to get positive output level. Figure 2(d) shows the current flow path for this mode.
5) To accomplish output voltage of V_0 = +5/7 V_{dc}, switches S2, S3 & S6 kept ON to get 5/7th voltage from the power circuit and from bridge circuit switches S7 & S10 are turned ON to get positive output level. Figure 2(e) shows the current flow path for this mode.
6) To realize output voltage of V_0 = +6/7 V_{dc}, switches S1, S4 & S6 kept ON to get 6/7th voltage from the power circuit and from bridge circuit switches S7 & S10 are turned ON to get positive output level. Figure 2(f) shows the current flow path for this mode.
7) To achieve output voltage of V_0 = + V_{dc}, switches S2, S4 & S6 kept ON to get V_{dc} voltage from the power circuit and from bridge circuit switches S7 & S10 are turned ON to get maximum positive output level. Figure 2(g) shows the current flow path for this mode.

Table.1. Switching Combinations of Proposed System for 15-Level Output Voltage

Level	Output voltage	Switches ON
1	+ V_{dc}	S2, S4, S6, S7, S10
2	+6/7 V_{dc}	S1, S4, S6, S7,S10
3	+5/7 V_{dc}	S2, S3, S6, S7, S10
4	+4/7 V_{dc}	S1, S3, S6, S7, S10
5	+3/7 V_{dc}	S2, S4, S5, S7, S10
6	+2/7 V_{dc}	S1, S4, S5, S7, S10
7	+1/7 V_{dc}	S2, S3, S5, S7, S10
8	0	S7, S9
9	-1/7 V_{dc}	S2, S3, S5, S8, S9
10	-2/7 V_{dc}	S1, S4, S5, S8, S9
11	-3/7 V_{dc}	S2, S4, S5, S8, S9
12	-4/7 V_{dc}	S1, S3, S6, S8, S9
13	-5/7 V_{dc}	S2, S3, S6, S8, S9
14	-6/7 V_{dc}	S1, S4, S6, S8, S9
15	- V_{dc}	S2, S4, S6, S8, S9

8) To obtain output voltage of V0 = 0, all switches are kept OFF to get 0 voltage from the power circuit and from bridge circuit switches S7 & S9 (or) S8 & S10 are turned ON to get zero output voltage level. Figure 2(h) shows the current flow path for this mode.

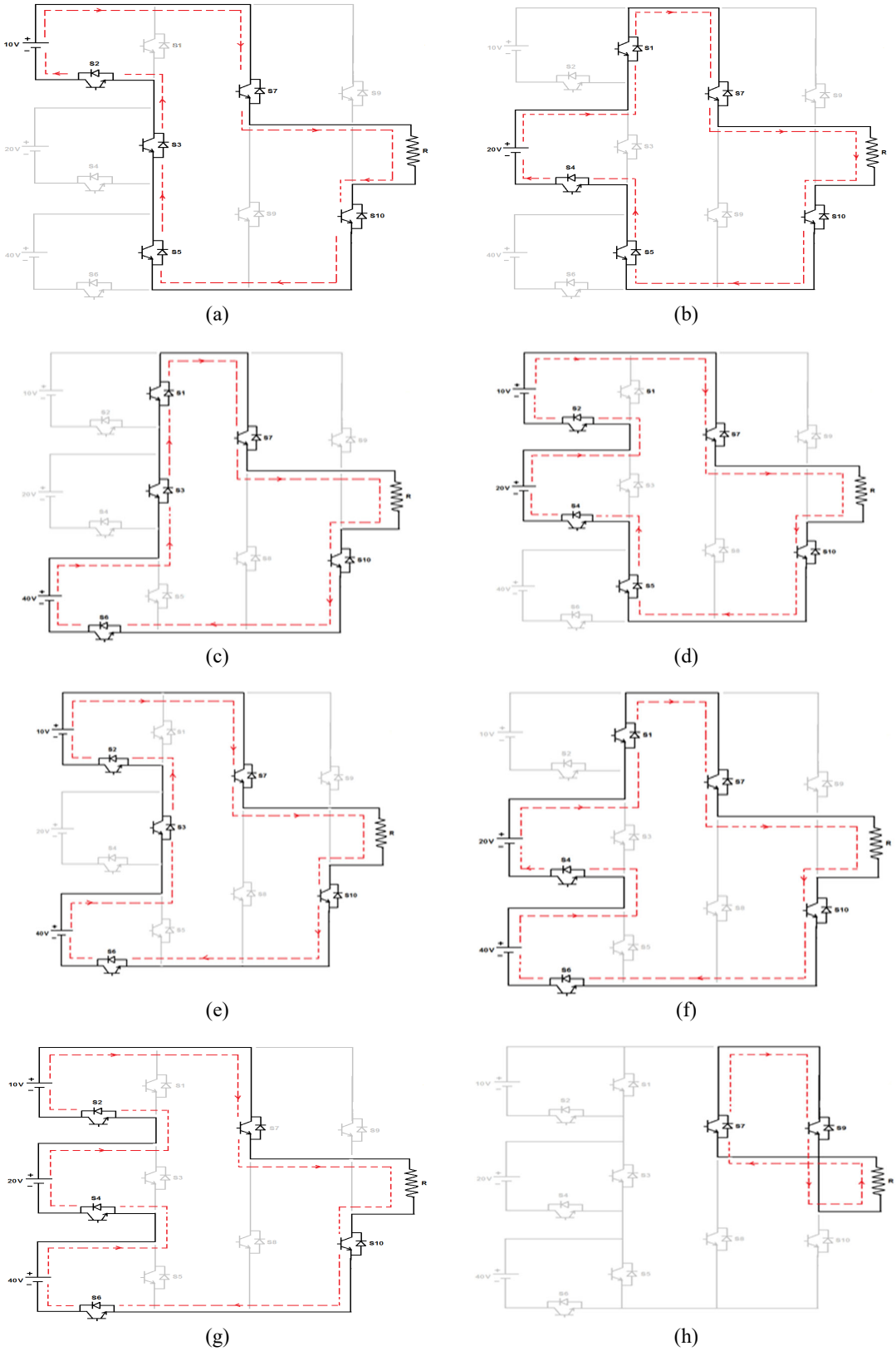


Figure 2. Modes of operation- positive and zero level, (a)+1/7 V_{dc} (b) +2/7 V_{dc} (c) +3/7 V_{dc} (d) +4/7 V_{dc} (e) +5/7 V_{dc} (f) +6/7 V_{dc} (g) V_{dc} (h) 0

Generally, voltage balancing problems arises due to non-uniform switching, non-ideal dc link capacitors, unequal commutation of semiconductor devices, unsymmetrical current and injection of current flow. It effects on performance of inverter degrades, increase of voltage stress, additional harmonic distortion and increase in load current magnitude. But this proposed system avoids above mention limitations, due to that voltage balancing not required.

2.3. Topology comparison

The proposed system compared with classic topologies like diode clamped, flying capacitor and cascaded H-bridge inverter. Among that proposed scheme requires minimum number of power switches and doesn't need of any passive elements. Table 2 shows equipments comparison of various topologies for 15 levels inverter.

Table 2. Equipments Comparison of Various Topologies for 15-Level Output Voltage

Features/Topologies	Proposed	Diode clamped	H-bridge	Flying capacitor
DC source	3	1	7	1
DC link capacitors	0	14	7	14
Power switches	10	128	28	128
Freewheeling (or) clamping diodes	0	14	0	0

3. MULTICARRIER SINUSOIDAL PULSE WIDTH MODULATION

To amalgamate the multilevel AC output voltage with different levels of dc input, the semiconductor power switches must switched to ON and OFF state in such that desired fundamentional is achieved with minimum harmonic distortion [21-23]. There are several approaches are available to select a PWM strategy for multilevel inverters like based on low/high frequency, number of switches used and voltage stress [24-27]. For classical multilevel topologies to get better performance mostly prepared space vector modulation the among various modulation techniques. But SVM is not possible when minimum number of switches used, because it cannot generate simultaneous switching pulses for multiple number of switches.

This proposed scheme implementated using Multicarrier Sinusoidal Pulse Width Modulation (MSPWM). A sinusoidal (reference) waveform is compared with numerous triangular (carrier) waveforms are scattered using phase disposition method. The peak to peak amplitude of triangular signal is Vtag, and peak to peak amplitude of sine signal is Vsin. Then the modulation index Mi is defined as,

$$M_i = \frac{V_{sin}}{3 * V_{tag}} \quad (1)$$

Then the output voltage of proposed system based on the applied input voltage and modulation index, which is defined as,

$$V_0 = M_1 * V_{dc} \quad (2)$$

Figure 3 shows the Multicarrier Sinusoidal Pulse Width Modulation with reference signal, carrier signal and gate pulses. Based on these comparison gate pulse generated for the power switches of proposed inverter, this is defined as,

(a) $V_{sin} < 0$ and $V_{sin} > V_{tag1}$ = S1 switched ON
(b) $V_{sin} > 0$ and $V_{sin} < V_{tag2}$ = S2 switched ON
(c) $V_{sin} > V_{tag4}$ = S4 switched ON and $V_{sin} < V_{tag}$ = S3 switched ON
(d) $V_{sin} > V_{tag5}$ = S5 switched ON and $V_{sin} < V_{tag4}$ = S6 switched ON
(e) $V_{sin} > V_{tag6}$ = S7 switched ON
(f) $V_{sin} > V_{tag3}$ = S8 switched ON

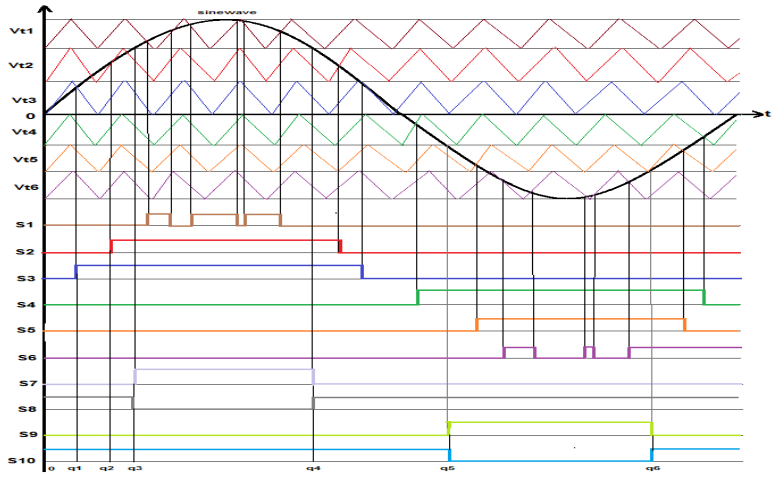


Figure 3. MSPWM - reference signal, carrier signal & gate pulses

4. SIMULATION RESULTS

The proposed 15 level inverter topology is simulated using matlab / simulink 2016a. The simulation results are obtained with switching frequency of 10 kHz and gate pulses are generated using multicarrier sinusoidal pulse width modulation with phase disposition method. Proposed system consists of three dc voltage sources are V1=10V, V2=20V & V3=40V. The simulation proposed system has the following merits,

(a) It does have diodes and capacitors, when number level increase, usage of diode will increase.
(b) Complexity of the controller is more, when number of level increase.
(c) Voltage stress & voltage balancing issue can be rectified based on the performance of the controller.

The proposed 15-level output voltage with 69.56 V, which is shown in Figure 4. In Figures 5 & 6 shows voltage across switch S8 & S9 respectively. Total harmonic distortion for output voltage and controlled current of proposed 15 levels scheme is 10.38% and 6.36% respectively, which is exposed in Figures 7(a) & 8(b).

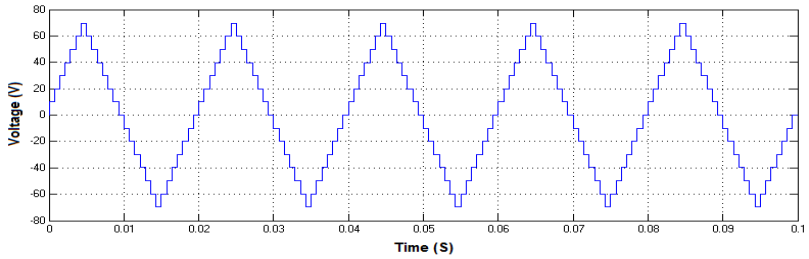


Figure 4. proposed 15 level output voltage waveform

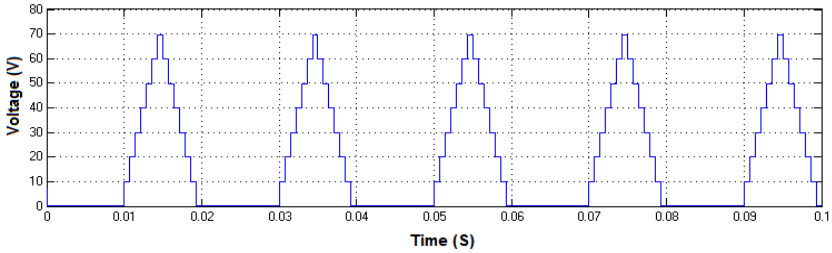


Figure 5. Voltage across switch S8

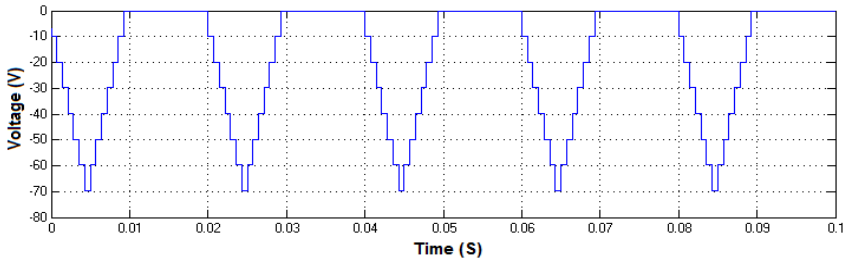
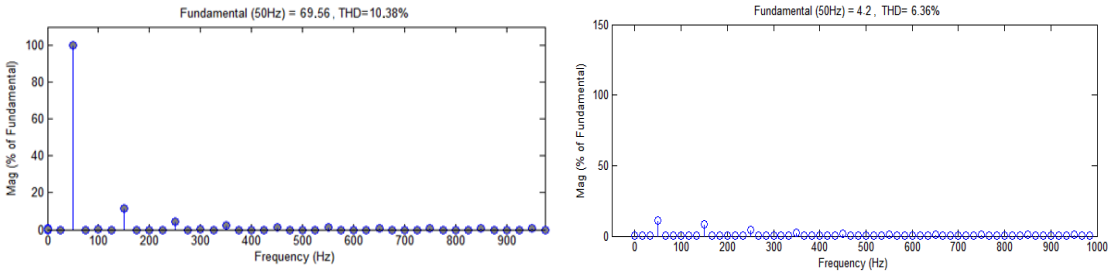


Figure 6. Voltage across switch S7



(a) (b)

Figure 7. THD analysis (a) Output voltage (b) Controlled current

Figure 8 shows proposed inverter output voltage with coupled inductor, which is used to smooth output voltage and current & also eliminates the usage transformer that can minimise cost of the system and leakage current problem. The modulation index will decide the output voltage level. When modulation index Mi is 0.6 with voltage of 49.2 V and Mi is 0.8 with voltage of 65.2 V and Mi is 0.99 with output voltage of 69.56 V, which is shown in Figures 9, 10 & 11 respectively. The output current of the proposed inverter without coupled inductor shown in Figure 12. The output current is controlled with help of coupled inductor with 4.2 A is exposed in Figure 13.

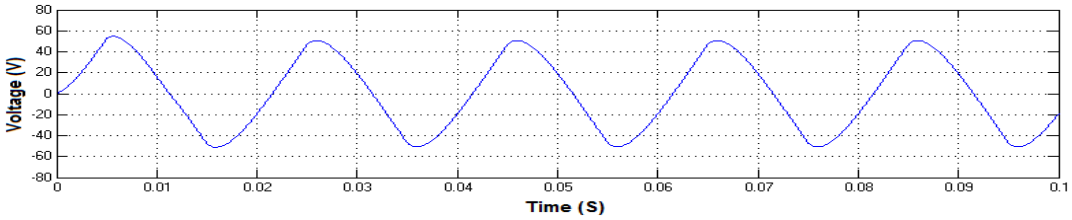


Figure 8. Inverter output voltage with coupled inductor

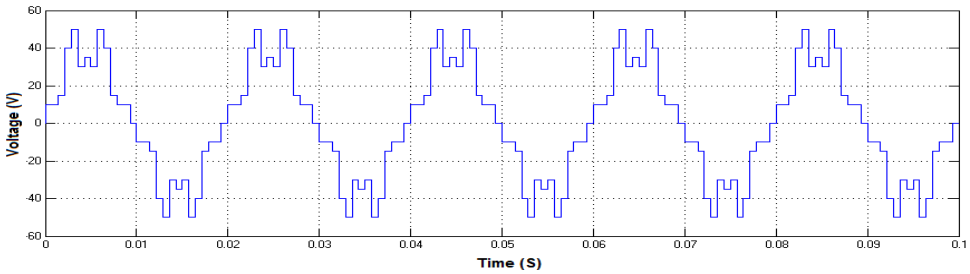


Figure 9. Output voltage with MI=0.7

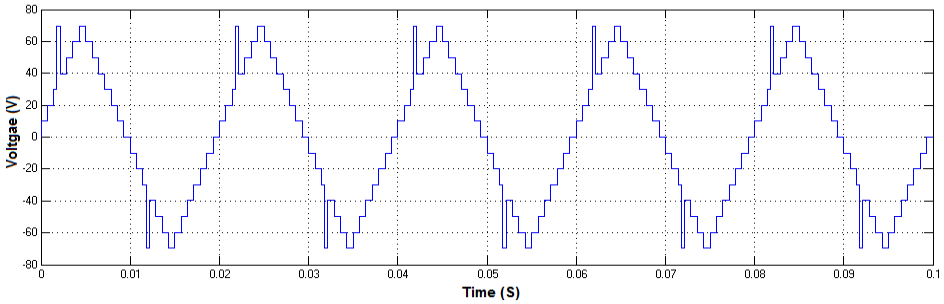


Figure 10. Output voltage with MI=0.8

In classical multilevel inverter topologies, number of switches connected in a leg will increase when the level increase. Due to increase in switches of a leg, this increases possibility for shoot through condition and complexity in switching pulse generation. But this proposed system doesn't have number of switches connected in series of a leg, which avoids the shoot through condition and easy to engender switching pulses.

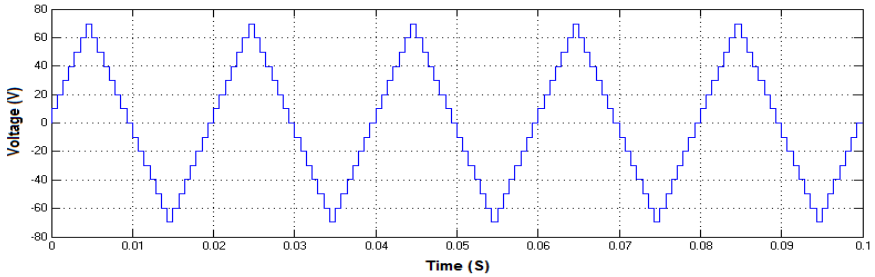


Figure 11. Output voltage with MI=0.99

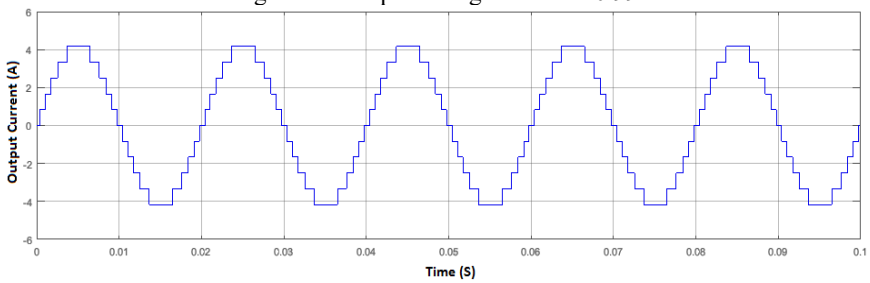


Figure 12. Output current without coupled inductor of 15 level inverter

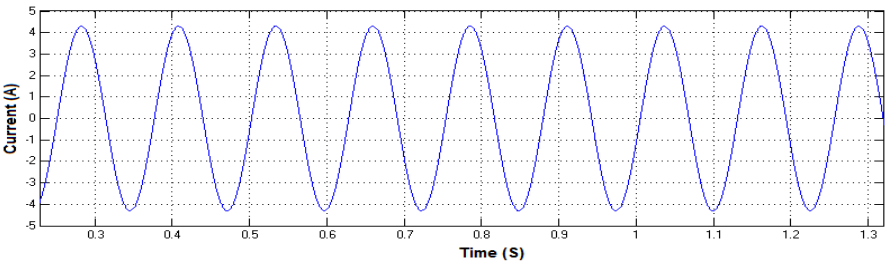


Figure 13. Controlled output current with coupled inductor of 15 level inverter

5. CONCLUSION

This paper established a novel 15 level dc-ac converter with reduced switches. Based on the SLR ratio the number of switches and level of inverter can be achieved. Proposed inverter power switches controlled by MSPWM method, and with help of coupled inductor which offer high consistency output voltage and low leakage current problem. At the same time, reducing of capacitor balancing, minimize the harmonic content and getaway from the shoot-through problem. The proposed 15-level inverter can accomplish higher efficiency, low system cost and higher reliability.

The proposed system generates 15 level output voltage with help of 10 power switches with Mi=0.99 and different level of output voltages are obtained with variation of Mi.

Accomplished better current control and voltage control of 15-level proposed inverter scheme with THD of 6.36% & 10.38% respectively.

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