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Three-phase five-level CHB inverter fed induction motor for renewable applications

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ABSTRACT

This paper presents the three-phase CHB inverter fed induction motor suitable for renewable energy source applications. Normally, all present existing multilevel inverters produce multilevel output, but the number of components required is more, bulk in size, more in cost. Which are more burdens to small capacity renewable sources. These challenges are eliminated in CHB inverter. This CHB mainly consisting of one DC source, one capacitor and eight switches in each phase. To generate a five-level output in phase to ground voltage, it is required to maintain the capacitor voltage (V2) at fifty percent of the DC source voltage (V1). This capacitor voltage is regulated by a sensor less voltage regulating technique. The sensor less voltage regulation works without any sensor devices. We can implement this technique with very less cost compared to other techniques. The sensor less voltage regulation is realized by level-shifted sinusoidal pulse width modulation. The simulation results show a very good dynamic performance. Controller maintains the capacitor voltage at fifty percent of the source voltage irrespective of main source voltage changes and load changes. Inverter generates a five-level wave at the output from line to ground and seven-level wave from line to line with fewer Harmonic. It is implemented in matlab/simulink and showing good dynamic performance.

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1. INTRODUCTION

Power demand is rapidly increasing day to day. The entire world searching for new ways to meet this demand by utilizing renewable energy sources. Because the renewable energy sources are pollution-free and eco-friendly. Consequently, an efficient interconnecting medium is required between renewable energy sources and load or grid. The best suitable power electronic device as a medium is multi-level inverters. So many multilevel inverter topologies have been proposed by researchers like NPC, FC and H-Bridge inverters. NPC and CHB are famous topologies [1-5]. NPC is the best topology for three-level configuration with a single DC bus for three-phase applications [6]. It has many drawbacks when increasing the number of levels more than three. Capacitor voltage balancing is the main drawback, unequal voltage distribution among the switches, unequal switching losses distribution among the semiconductor devices, a huge number of switches, capacitors and isolated DC sources are required are also drawbacks of NPC. All these challenges are eliminated in three phase five-level CHB inverter. CHB inverter requires eight switches, one capacitor, and only one DC source per phase [7, 8].

This paper presents the three-phase five-level Cascaded H-Bridge inverter fed three-phase induction motor. Each phase of this inverter control by sensor less voltage regulation. Sensor less voltage regulation is analyzed mathematically and control reference signals are modulated by level-shifted SPWM technique [9-16]. The system is tested in different load conditions using Matlab/smulink and compared with NPC topology.

2. FIVE LEVEL CHB

Five-level inverter is implemented by analyzing typical two-level, three-level, five-level and seven level waves THD results using FFT tool. It is as shown in Table 1. By Comparing two and three-level waveforms, thee level waveform reduces the THD by half naturally. The drop in the THD is similar when migrating from 3-level to 5-level. Such a ratio in THD value is small when going to the upper levels from 5 to 7. It happens because of the fact that five-level wave has been almost near to sine wave shape and THD also low, simultaneously increasing levels requires sensors and controlling devices, which rise in the size and cost. Because of the above merits in five-level inverter research leads in five-level inverters.

Table 1. No of voltage levels of a waveform and corresponding approximate THD value

No of voltage levels of waveform	Approximate THD value
2 level	110%
3 level	58%
5 level	30%
7 level	24%

Three-phase five-level Cascaded H-Bbridge inverter fed three-phase induction motor is shown in Figure 1 [17]. It accommodates eight switches, one capacitor and one DC source in each phase. If a DC source of V1 is connected at DC source point, the capacitor voltage V2 must be maintained at fifty percent of V1 by the controller [18, 19]. Hear sensor less voltage regulation is used to maintain the capacitor voltage at the required value. Table 2. shows the all possible switching states to obtain the five-level output [20-25]. It can be observed from Table 2. that the capacitor can be charged or discharged easily by using a switching pattern. During switching state 2 and 6 the capacitor is connected in series with source and load, capacitor charge increases. Similarly, during switching state 3 and 5 capacitors connected in series with a load, capacitor stored energy is supplied to load and capacitor charge reduces. Continuous alternative charging and discharging makes the capacitor voltage balance. These switching sequences are realized by level-shifted sinusoidal pulse width modulation integrated with sensor less voltage balancing [26].

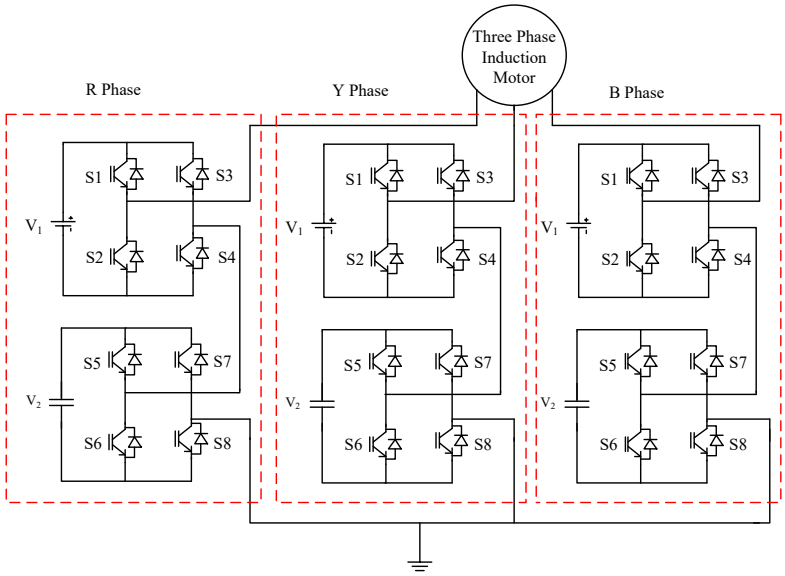


Figure 1. Three-phase cascaded H-Bridge inverter fed three phase induction motor

3. SENSOR-LESS VOLTAGE REGULATING TECHNIQUE

The DC source voltage (V_1) assumed as 2E volts. It is required to maintain the capacitor voltage (V_2) at E volts to produce five voltage levels in output. It can be observed from Table 2 that the capacitor can be charge or discharge in a positive half cycle, similarly it can be charge or discharge in the negative half cycle. The capacitor voltage can be maintained constant by maintaining constant charging time and discharging time, in such a way that it should be charge for the first half cycle and discharge for the remaining half cycle. Normally switching state 2 and 3 supplies E volts at output, but switching state 2 charges the capacitor and switching state 3 discharge the capacitor. Hence charging state 2 is used in a positive half cycle. Similarly, in negative half cycle switching state 5 and 6 produce the –E volts, but switching state 5 charges the capacitor and switching state 6 discharge the capacitor, hence charging state 6 is used in a negative half cycle. The charging and discharging are expressed in mathematical form in (1)

$$V_1 = V_2 + V_{out} \Rightarrow \begin{cases} 2E = V_2 + E \\ -2E = V_2 - E \end{cases} \Rightarrow |V_2| = E \quad (1)$$

Charged and discharged energy in the capacitor is depends on load only, not depends on output frequency or switching frequency. Similarly capacitor size also depends on the load. This self-regulating voltage strategy is mathematically proved with the energy storage relations of the capacitor. The output current and voltage waveforms of a five-level CHB inverter are shown in Figure 2.

Mathematical representation of output current and voltage waveforms at load is shown in (2) and (3)

$$V_l(t) = V_m Sin(\omega t) \quad (2)$$
$$i_l(t) = I_m Sin(\omega t - \theta) \quad (3)$$

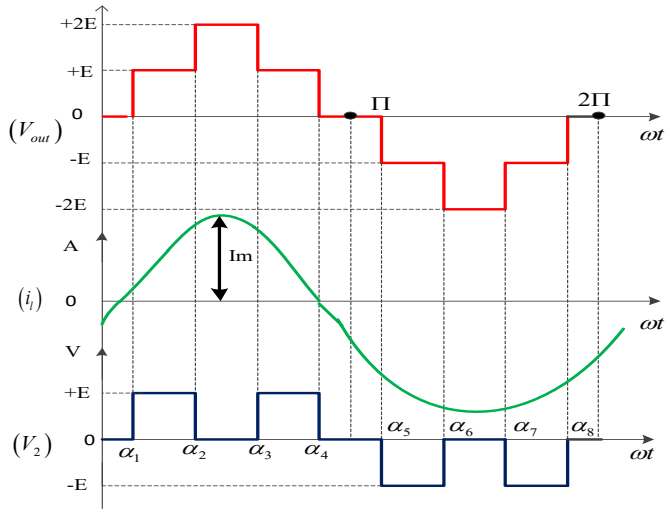


Figure 2. Typical output voltage and current of the five-level inverter

Where V_m and I_m are the maximum value of voltage and current respectively, similarly θ is the phase angle between voltage and current. Output current flowing through capacitor can be written as

$$I = \frac{dq}{dt}$$
$$dU = Vdq = VIdt \quad (4)$$
$$U = \int VIdt$$

Where I is the current flowing through the capacitor, V2 is the voltage across the capacitor, q is the charge on capacitor plates and U is energy stored in the capacitor. From (3) and (4) the charging energy of the capacitor can be written as follows by considering

$$U^{+}=\int_{0}^{\pi}V_{C}\,Sin(\omega t-\theta_{0})d(\omega t)U^{+}$$
$$=I_{m}\begin{bmatrix}\int_{0}^{\alpha_1}0\times Sin(\omega t-\theta_{0})d(\omega t)\\+\int_{\alpha_1}^{\alpha_2}E\times Sin(\omega t-\theta_{0})d(\omega t)\\+\int_{\alpha_2}^{\alpha_3}0\times Sin(\omega t-\theta_{0})d(\omega t)\\+\int_{\alpha_3}^{\alpha_4}E\times Sin(\omega t-\theta_{0})d(\omega t)\\+\int_{\alpha_4}^{\pi}0\times Sin(\omega t-\theta_{0})d(\omega t)\end{bmatrix}$$
$$=EI_{m}\begin{bmatrix}Cos(\alpha_1-\theta_0)-Cos(\alpha_2-\theta_0)\\+Cos(\alpha_3-\theta_0)-Cos(\alpha_4-\theta_0)\end{bmatrix} \quad (5)$$

In the same way, the discharging energy of the capacitor can be written as

$$U^{-}=\int_{\pi}^{2\pi}V_{C}I_{m}Sin(\omega t-\theta_{0})d(\omega t)$$
$$=I_{m}\int_{\pi}^{2\pi}V_{C}Sin(\omega t-\theta_{0})d(\omega t)$$
$$=EI_{m}Cos(\omega t-\theta_{0})\Big|_{\alpha_5}^{\alpha_6}+EI_{m}Cos(\omega t-\theta_{0})\Big|_{\alpha_7}^{\alpha_8}$$
$$=EI_{m}\begin{bmatrix}Cos(\alpha_6-\theta_0)-Cos(\alpha_5-\theta_0)\\+Cos(\alpha_8-\theta_0)-Cos(\alpha_7-\theta_0)\end{bmatrix} \quad (6)$$

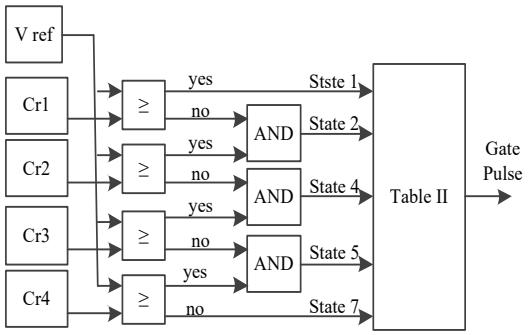
From equation (5) and (6), we can observe that the output voltage is symmetric about positive and negative half. Hence we can write an (7) as

$$\begin{cases}\alpha_5=\pi+\alpha_1\\ \alpha_6=\pi+\alpha_2\\ \alpha_7=\pi+\alpha_3\\ \alpha_8=\pi+\alpha_4\end{cases} \quad (7)$$

The energy stored in a positive half cycle and negative half-cycles are same, but has opposite in polarity

$$U^{+}=-U^{-} \quad (8)$$

From (8) the energy-charged or discharged by the capacitor is balanced and constant and also it keeps the capacitor output voltage constant irrespective of all conditions. Sensor less voltage control is integrated with level shifted multi carrier PWM modulation. Four carrier signals are used for five-level output, carrier signals and a reference sine wave are shown in Figure 3(a). The reference sine wave is modulated with four vertically shifted triangular signals. This modulation output is mixed with switching states shown in Table 2. Figure 3(b) shows the firing pulse generating algorithm. This algorithm initially fixes the capacitor voltage at the desired value and then produced five voltage levels at the output without any feedback sensor. Table 2 shows the switching positions in various states and capacitor charging/discharging conditions.



(a) (b)

Figure 3. (a) Four level-shifted carrier waves modulated with reference sine wave for Five-level PWM scheme, (b) The proposed sensor-less voltage regulating algorithm integrated into the switching technique

Table 2. Switching states, Capacitor charging/ discharging condition and output voltage of five levels CHB inverter

State	S1	S2	S3	S4	S5	S6	S7	S8	V output	V out value	Capacitor voltage status
1	1	0	0	1	1	0	1	0	V_1	*+2E*	No Effect
2	1	0	0	1	0	1	1	0	V_1- V_2	*+E*	Charging
3	1	0	1	0	1	0	0	1	+ V_2	*+E*	Discharging
4	1	0	1	0	0	1	0	1	0	*0*	No Effect
5	1	0	1	0	0	1	1	0	- V_2	*-E*	Discharging
6	0	1	1	0	1	0	0	1	V_2- V_1	*-E*	Charging
7	0	1	1	0	1	0	1	0	- V_1	*-2E*	No Effect

4. COMPARISON WITH NPC

Neutral Point Clamped (NPC) and Flying Capacitor inverters are more popular voltage source multilevel inverters. NPC is the most popular topology as in three-phase three-level inverter applications. NPC has been using since lost two decays for all types of applications in the industry. Because it is available with medium voltage and high power ratings and it is operated with only one DC link. But NPC has some disadvantages like complexity in capacitor voltage balance, more harmonics in output, unequal switching losses distributed over the semiconductor devices, limitations in switching frequency, unequal voltage rating switches are required in the design. While increasing voltage levels from three-phase three-level to three phase five-level, it requires more number of switches and isolated DC sources compared to three-phase five level CHB inverter. Because there is no effective method was proposed by researchers for three-phase five level NPC with a single DC link due to practical limitations in the ratio between the modulation index and the power factor. Three-phase CHB converter can generate seven levels in each phase and nine levels in line to line voltage with the same number of components used in three-phase five-level CHB inverter.

5. SIMULATION RESULTS AND DISCUSSION

Three-phase five-level CHB inverter operated by the designed switching pattern was simulated by using Matlab/Simulink. Capacitor voltage balancing and the symmetrical wave generated at the inverter output are analyzed to observe the effectiveness of proposed switching technique. Discrete demine is used in Matlab/Simulink with a sample time of one microseconds. All the parameters used in system are shown in Table 3. The simulation has been done with three-phase five-level CHB inverter connected to three-phase induction motor with capacitor initial voltage zero. Figure 5(a) shows the voltage across the capacitor in R phase. In this graph capacitor voltage is zero at starting and reaches the desired value in six cycles. Hear the source voltage is 440V, so the desired voltage is 220V. It reaches the 220V in 0.12 seconds. after 0.1sec capacitor voltage ripples are very less, which are in acceptable range as shown in Figure 5(a). Seven level waveform at line to line and five-level wave form at line to ground was generating after reached the capacitor value to the desired value. The inverter line to line and line to ground voltage is shown in Figure 4. three-phase load current shown in Figure 5(b). It has pure sine wave after reaching the capacitor voltage to the required value. It has high current at starting because of the induction motor type load. Load voltage FFT analysis is shown in Figure 6(b). it is analyzed for three cycles from 0.5 sec and the THD value is 20.23%.

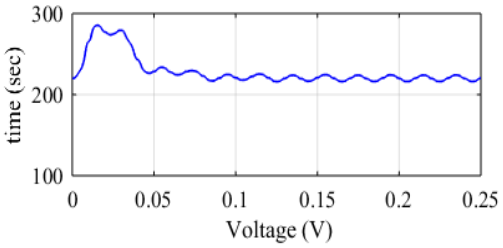
similarly, load current also analyzed in the same way and it showing a THD value of 1.87%. The speed of the motor is shown in Figure 6(a). It reaches to rated value in 0.3 seconds and a sudden load change applied at 0.5 seconds, it created small fluctuation in speed at 0.5 seconds. The overall system has given good dynamic performance under sudden load change condition, voltage change conditions and capacitor voltage balancing also good

Table 3. System parameters used in matlab

Parameter	Value
V_1	440 V
C	0.015F
Inverter fundamental frequency	50 Hz
Squirrel Cage Motor	460 V, 50Hz, 3730W
Carrier frequency	10 kHz
V_{Ref} peak to peak	3.5 V

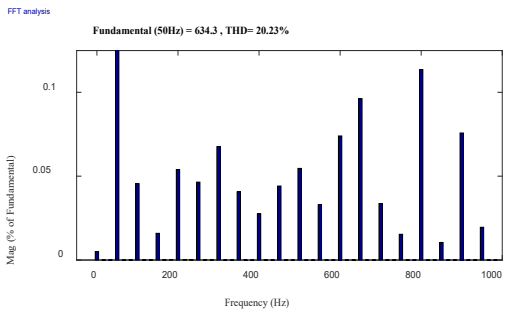
(a) (b)

Figure 4. (a) Three-phase line to line voltage output of inverter with seven levels (b) Phase to ground voltage output



(a) (b)

Figure 5. (a) Voltage across capacitor (b) Three-phase load current



(a) (b)

Figure 6. (a) Speed of the induction motor (PU), (b) THD spectrum of line voltage

6. CONCLUSION

In this paper, sensor less voltage control was proposed. It is applied to three-phase CHB inverter fed three-phase induction motor. This controller regulates the second source voltage at fifty percent of the first source voltage. However, five levels of voltage in each phase and seven levels of voltage from line to line have been generated in the output of the inverter. It is proved that the sensor less voltage regulator does not require any feedback sensor. Sensor less control is modulated into level-shifted sinusoidal pulse width modulation, which is very simple to implement in applications. This proposed system is best suitable for agricultural water pumping drive fed from a solar energy source. This system requires three voltage sources for three phases.

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