

An enhanced 17-level hybridized multilevel inverter with stair case modulation

Hemalatha Javvaji¹, Basavaraja Banakara²

¹ Department of Electrical and Electronics Engineering, PVP Siddhartha Institute of Technology, India

² Department of Electrical and Electronics Engineering, Davanagere University, India

Article Info

Article history:

Received Dec 11, 2019

Revised Apr 4, 2020

Accepted Jul 10, 2020

Keywords:

Cascaded H-bridge inverter

Multilevel

Stair case modulation technique

Total harmonic distortions

Voltage levels

ABSTRACT

This paper proposes a hybridized symmetric cascaded multilevel inverter for voltage levels ranging from 5 levels to 17 levels. The proposed Multi Level Inverter (MLI) topology is built using a modified H-bridge inverter that results in an increased output voltage levels with a smaller number of solid-state switches. This technique enhances the h-bridge configuration from three level to five level by means of a bi-directional switch at source. Gating pulses of hybridized symmetric MLI are generated through staircase modulation. The operation and performance of the proposed topology is tested for different output voltage levels, simulation results prove that the proposed technique results in less THD at all levels with lesser power consumption and are easily applicable for renewable energy applications.

This is an open access article under the [CC BY-SA](#) license.



Corresponding Author:

Hemalatha Javvaji,
Department of Electrical and Electronics Engineering,
PVP Siddhartha Institute of Technology,
Kanuru, Vijayawada, Andhra Pradesh, India.
Email: hemajavvaji@gmail.com

1. INTRODUCTION

Multilevel inverter topologies are emerged to be a versatile alternative in the area of high power and medium-voltage control. Multilevel inverters (MLI) comprise of quite a lot of input sources, capacitors, active switches, power diodes and drivers to generate the required output voltage using a suitable switching pattern [1] with an apt power quality. MLI has gain more attention because of their advantageous features like high output power quality, amplitude of fundamental component, efficiency, less harmonic distortion, switching losses, and low dv/dt. These features motivated to shift from the traditional two-level converter to multilevel converters. MLI's generates the stepped voltage waveform at the output by integrating dc source connected with its input terminals. With increasing the number of dc links at input higher and higher levels of voltages are obtained at output. Based on distinct topologies used in MLI design the dc power supplies at input can be isolated or inter-connected [2-6]. Because of high power outputs MLI's are mostly used in industrial applications [7]. Conventional structures such as Diode Clamped or Neutral Point Clamp (NPC) [4] and Flying Capacitor (FC) [8] used in the design of MLI's suffer from high number of diodes and capacitors in higher power applications. It is established in literature that cascaded MLI structure is compact reliable structure in deriving high voltage and power levels [9-13]. Cascaded MLI's are constructed by linking number of H-bridge inverters in series [14, 15] in symmetrical or asymmetrical structure. In the symmetric configuration, the magnitude of input DC sources are equal, in contrast, asymmetric MLI have different magnitude input DC sources due to which the number of output levels are more compared to symmetrical configuration with reduced Total Harmonic Distortion (THD) [16-22]. It is evident from the literature that

cascaded MLI supports high power levels with the use of low voltage rating components in inverters. Cascade MLI's are more reliable, fault tolerant and ease maintenance because of its modular structure [23]. MLI's are made fault tolerant through an appropriate control strategy that bypass the faulty cell without disturbing the load [24, 25]. Although Cascaded MLI's are simpler in construction and easy to control they use higher number of switching components and dc sources.

The advancements in MLI's also resulted in distinct modulation techniques. Modulation techniques are selected depending upon converter topology and its domain of application that has its own merits and demerits. Further high or low frequency switching based modulation technique is proposed [26] for MLI's with switching frequency up to 1 kHz for high power applications. One of the frequently adopted modulation techniques for MLI's is sinusoidal PWM widely used in two different forms, with the first being level shifted PWM which is widely used to generate high quality output wave form and other Phase shifted PWM techniques [14]. In second techniques, carriers are either triangular, saw-tooth or constant DC magnitude waveforms etc., and the reference waveforms are sinusoidal, sinusoidal injected with third harmonic and trapezoidal voltage waveforms. [27-32].

In this paper, a symmetric Hybridized MLI topology proposed to overcome some of the drawbacks of conventional cascaded MLI's. The proposed hybridized MLI topology adopts staircase modulation technique that generates more output voltage levels with less numbers of switches or active devices. Results obtained are validated by comparing with existing conventional cascaded H bridge MLI's.

Section II, discusses the proposed structure and possible states. A discussion on control method, losses and reliability is presented in section III. Simulation results and Comparative study are brought in section IV. Finally, the conclusion of this paper is given in section V.

2. PROPOSED TOPOLOGY

Figure 1 presents the topology of the novel hybridized H-bridge cascaded MLI. It comprises of five bidirectional active switches from voltage prospect (S_1, S_2, S_3, S_4 and S_A) and two symmetrical input dc voltage sources. Table 1 and Table 2 shows the output levels of generated voltage using the distinct switching patterns in the proposed topology. In Tables, green cell indicates conducting device (On position) and red cell indicates non conducting device (Off position). The proposed single-phase, 5-level cascade MLI, shown in Figure 1, is a hybridized 5-level inverter. Table 1, depicts the switching pattern for a five-level output voltage generated with two positive, two negative and one zero at the output. The 5-level hybrid inverter comprises a single-phase conventional H-bridge cell, and a bidirectional switch connected to the two dc sources at center tap.

In symmetrical configuration with 2 input dc sources, output level can be obtained as follows

$$P_{Level} = 4 * p + 1 \quad (1)$$

Where p is equal to the number of cells.

The number of switches is given as

$$\text{Number of Switches} = \frac{(P_{Level}-1)}{\text{Switches per cell}} * (\text{Switches per cell} + 1) \quad (2)$$

Similarly, a seventeen-level cascade MLI is obtained by using 4 hybridized H bridge cells. Figure 2, shows the proposed single-phase, 17-level cascaded MLI and its switching pattern are represented in Table 2.

Table 1. Switching States for 5 - level hybridized MLI

S. NO	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_A	V_0
1	Red	Green	Red	Red	Red	Red	Red	Red	Green	V_{dc}
2	Green	Green	Red	Red	Red	Green	Red	Red	Red	$2 V_{dc}$
3	Red	Red	Green	Red	Red	Red	Green	Red	Red	0
4	Red	Red	Red	Green	Red	Red	Red	Green	Red	$-V_{dc}$
5	Red	Red	Red	Red	Green	Red	Red	Red	Green	$-2 V_{dc}$

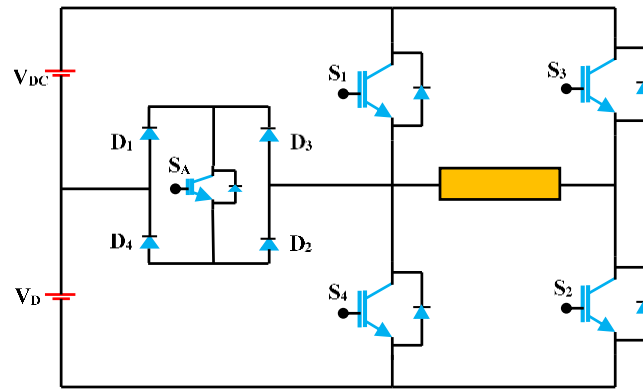


Figure 1. 5-Level hybridized H bridge MLI

Table 2. Switching states for a 17-level hybridised MLI

S. NO.	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂	S ₁₃	S ₁₄	S ₁₅	S ₁₆	S _A	S _B	S _C	S _D	V ₀
1	Off	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	V _{DC}
2	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	2V _{DC}
3	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	3V _{DC}
4	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	4V _{DC}
5	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	5V _{DC}
6	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	6V _{DC}
7	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	7V _{DC}
8	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	8V _{DC}
9	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	0
10	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-V _{DC}
11	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-2V _{DC}
12	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-3V _{DC}
13	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-4V _{DC}
14	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-5V _{DC}
15	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-6V _{DC}
16	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-7V _{DC}
17	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	On	-8V _{DC}

Off state of the Switch

On state of the Switch

Table 3. Comparison of solid-state components of conventional topologies with hybridized cascaded MLI for 17 -Level

Inverter Topology	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Hybridized H-Bridge
Main switches	$(P_{Level}-1)*2=32$	$(P_{Level}-1)*2=32$	$(P_{Level}-1)*2=32$	$\frac{(P_{Level}-1)}{Switches\ per\ cell} * (Switches\ per\ cell + 1) = 20$
Clamping diodes	$(P_{Level} - 1) * (P_{Level} - 2) = 240$	0	0	0
DC Bus	1	1	8	8
Bus Capacitors	$(P_{Level}-1)=16$	$(P_{Level}-1)=16$	$(P_{Level}-1)/2=8$	0
Balancing Capacitors	0	$\frac{(P_{Level}-1)*(P_{Level}-2)}{2} = 12$	0	0

Table 3. supports the developed topology as the main motto behind the developing present topology is to reduce the number of solid-state devices. The proposed topology uses only 4 H-bridge MLI's in generating 17-Level output which effectively reduced the solid-state devices by 37.5% in comparison to conventional cascaded H bridge MLI. As the number of components are reduced when compared with conventional topologies that also results in reduced switching losses and number of GATE drivers. It also has reduced circuit complexity with increased modularity and is more economic.

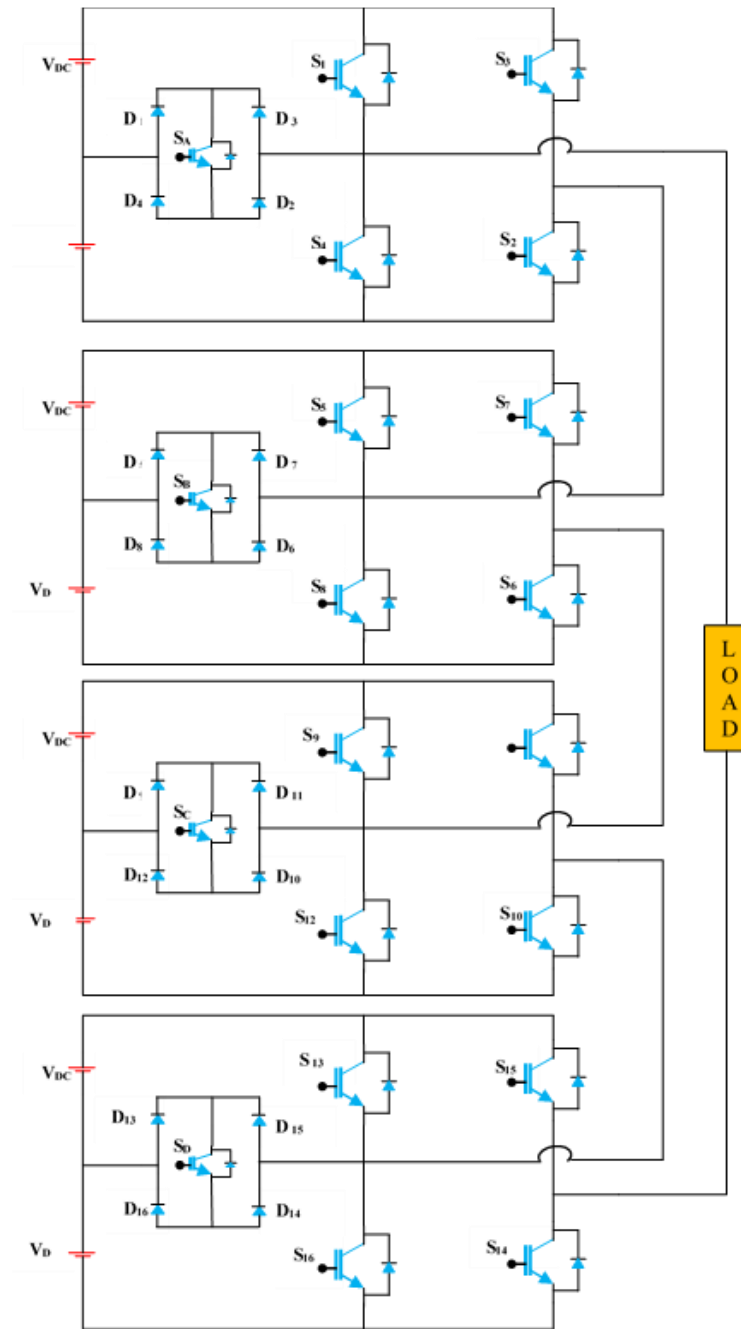


Figure 2. 17-Level hybridized cascaded MLI

3. CONTROL METHODS

In convention and Hybridized cascaded MLI topologies one of the prominent techniques used to achieve required switching pattern is multi carrier sinusoidal PWM. As the output levels increases it require high switching frequency resulting in more switching losses. The staircase PWM applied in the present work is a mixture of sinusoidal PWM and selective harmonic elimination. Stait case PWM is derived from a sinusoidal PWM by replacing the sine wave with a stair case. Number of steps in stair case are determined based on the specific harmonic cancellation. The desired output voltage level and quality is ibtained with a proper selection of frequency ratio and number of steps in the stair case. Whenever the value of modulating signal is more than the carrier signal pulses are generated. Compared with the carrier-based PWM technique, the staircase modulation features lower switching losses since the entire power semiconductor devices operate at the fundamental frequency. Staircase modulation is proven to a feasible solution in reducing the switching losses with a low frequency.

In digital implementation of stair case PWM the switching angles are determined in prior for all the 4 hybridized MLI's and are stored in a table. In this work a modulating wave has been separated in to 15 zones with each zone referring a switching pattern to obtain the voltage level in the output wave form. Figure 4. Shows the switching patterns of the power semiconductor modules of proposed topology and stepped-voltage waveform.

The staircase reference is compared with triangular carriers with different frequencies which generate the Boolean output. A logic operation is applied accordingly to get the switching pattern of the proposed MLI topology from generated Boolean output, which generates pulses for corresponding power modules is shown in Figure 3.

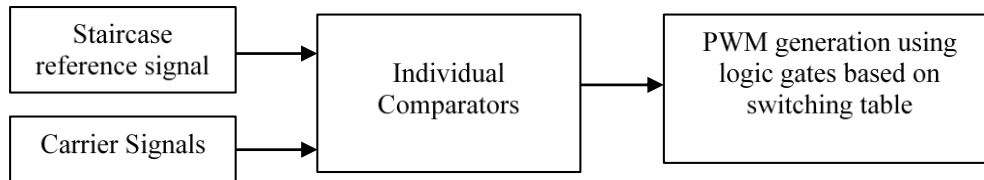


Figure 3. Block diagram to generate gate pulses

3.1. Calculation of switching frequency

Switching frequency for any level is predetermined using

$$f_{switch} = \text{fundamental frequency} * 2(2^p - 1) \quad (3)$$

3.2. Identification of step angle

$$\alpha_k = \sin^{-1} \frac{(k-1)+y}{z+y} \text{ for } k=1,2,\dots,z \quad (4)$$

Where k = number of step angles, z = Maximum number of steps and y = Coefficient for adjusting switching angle.

The modulation index can be obtained using

$$m_i = \frac{V_1}{z * \frac{4V_{dc}}{\pi}} \quad (5)$$

Where V_1 = Fundamental voltage V_{dc} = D.C Bus voltage.

3.3. Losses

In the operation of solid state components based circuits, conduction loss, switching loss, Off-state losses and gate losses are considered for the analysis. In general, the Off-state and Gate losses are negligible in comparison with the other two hence are neglected in the analysis.

3.3.1. Conduction losses

The conduction losses are generated in each device during ON state. In MLI's conduction losses also depends on conduction time of the device. Hence to consider the time conduction losses are multiplied by a correction factor P_{CON} . In general, the conduction loss in MLI's is given as

$$\text{Conduction loss} = V_{CE} \times I_C \times P_{CON} \quad (6)$$

Where V_{CE} is the collector-emitter voltage drop and I_C is the collector current during ON-state of the device and

$$P_{CON} = \frac{t_{L-i}}{T} \quad (7)$$

T is the total time period, and t_{L-i} is the total ON state time of the device in p^{th} level.

3.3.2. Switching loss

The switching loss in the IGBT are in general given as

$$P_{SW} = F_{SW} \times (E_{SW(on)} + E_{SW(off)}) \quad (8)$$

Switching loss also depends on the switching time. In the design of MLI's calculation of switching time depends on switching frequency which becomes complex with higher frequencies. Switching loss with switching time are given as

$$P_{SW} = F_{SW} \times (E_{SW(on)} + E_{SW(off)}) \times D_{SW} \quad (9)$$

Where D_{sw} is factor accounted for switching time $D_{SW} = \frac{T_{SW}}{T}$

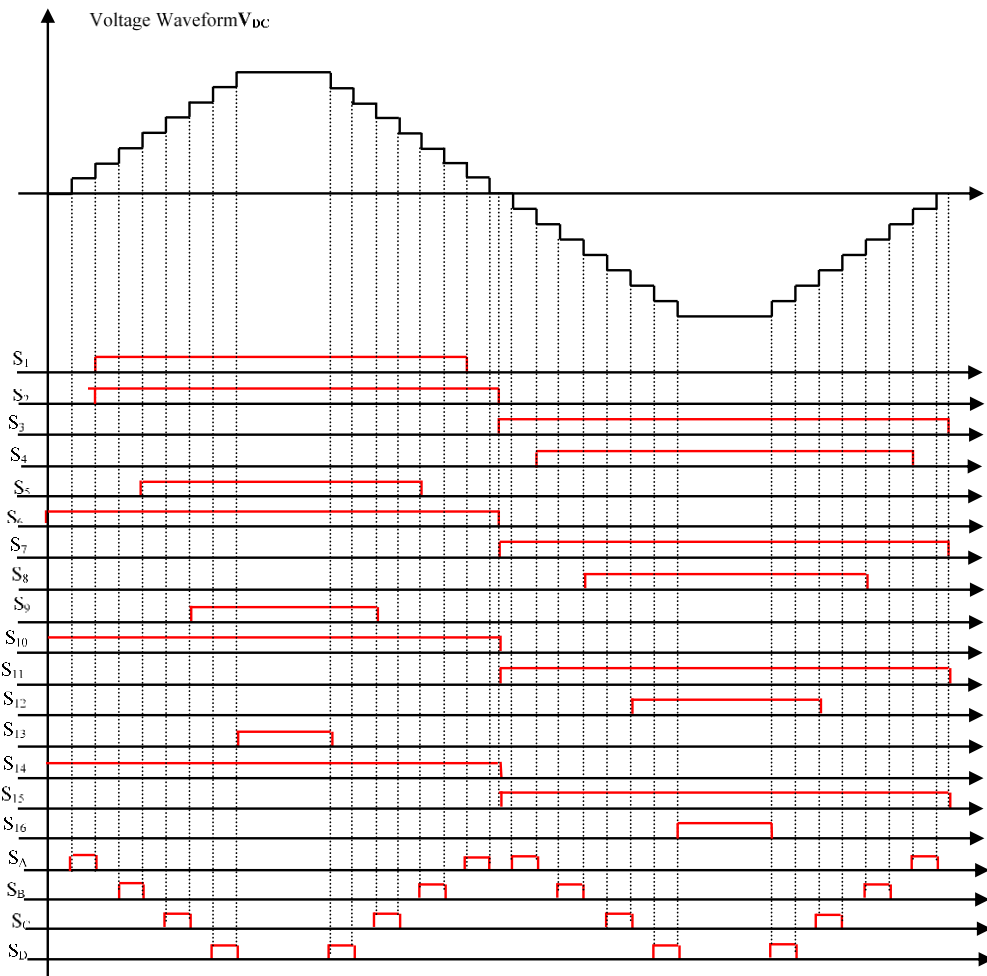


Figure 4. Switching Patterns of Hybridized MLI

4. SIMULATION AND RESULTS

In order to support the proposed cascaded MLI topology, simulations studies are carried in MATLAB SIMULINK environment with the constructed Simulink model. With the switching schemes described in Section 3, 5-level and 17-level MLI's are considered for the analysis. In a 17 Level hybridized MLI stair case PWM switching patterns T1-T4 are generated with switching frequency of 100Hz, 300Hz, 700Hz and 1500Hz against a Stair case reference wave at fundamental frequency of 50 Hz, as depicted in Figure 5 and Figure 6.

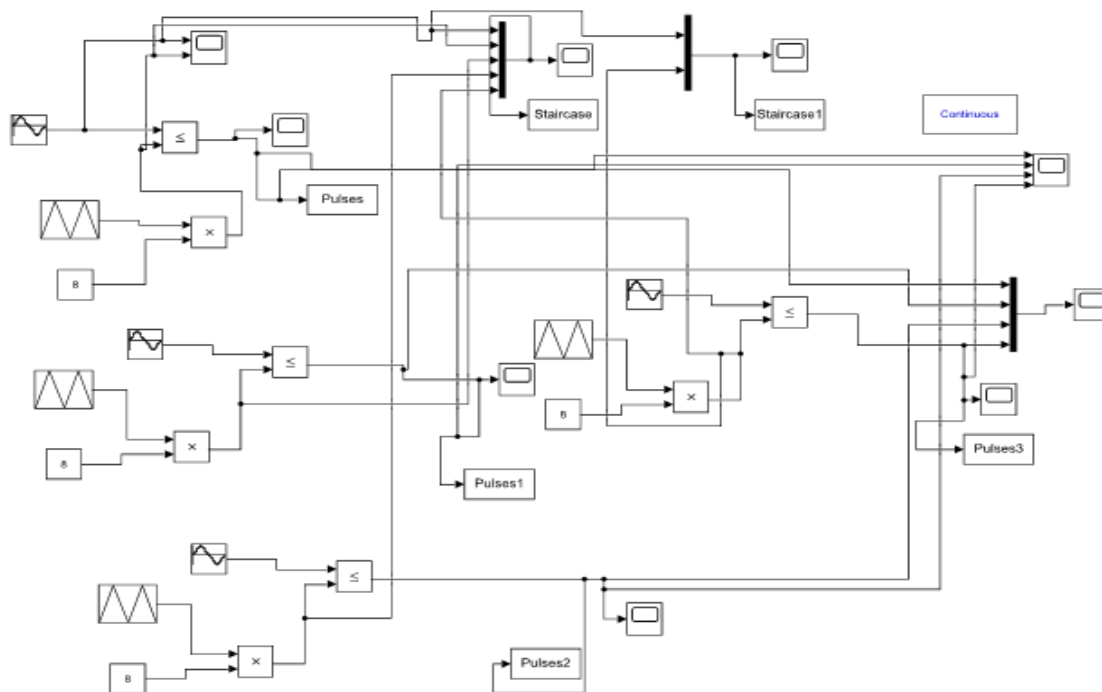
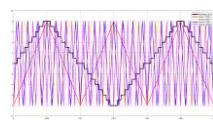
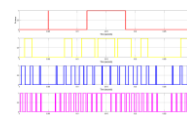


Figure 5. Simulink model of pulse generation using staircase modulation



(a)



(b)

Figure 6. Stair case modulation for the proposed 17-level hybridized MLI
(a) staircase modulation and corresponding carrier (b) generated pulses

4.1. Calculation of switching frequency

Switching frequency for any level is predetermined using

$$f_{switch} = \text{fundamental frequency} * 2(2^p - 1)$$

Table 4 shows the switching frequency adopted in this paper for different output levels of the hybridized cascaded MLI.

Table 4 Switching frequencies for output levels

Output Level	Switching frequency
5-Level	100Hz
9-Level	300Hz
13-Level	700Hz
17-Level	1500Hz

4.2. Identification of Step angle

$$\alpha_k = \sin^{-1} \frac{(k-1)+y}{z+y} \text{ for } k=1,2,\dots,z$$

where k = number of step angles, z = Maximum number of steps and y = Coefficient for adjusting switching angle

For a hybridized 17 level MLI the value of $z = 8$ and $y = 1$ are considered. The obtained step angles are given by $\alpha_1 = 6.38^\circ$; $\alpha_2 = 12.84^\circ$; $\alpha_3 = 19.47^\circ$; $\alpha_4 = 26.39^\circ$; $\alpha_5 = 33.74^\circ$; $\alpha_6 = 41.81^\circ$; $\alpha_7 = 51.05^\circ$; $\alpha_8 = 62.74^\circ$ and are shown in Figure 4.

The modulation index can be obtained using

$$m_i = \frac{V_1}{z * \frac{4V_{dc}}{\pi}}$$

Where V_1 = Fundamental volatge V_{dc} =D.C Bus voltage.

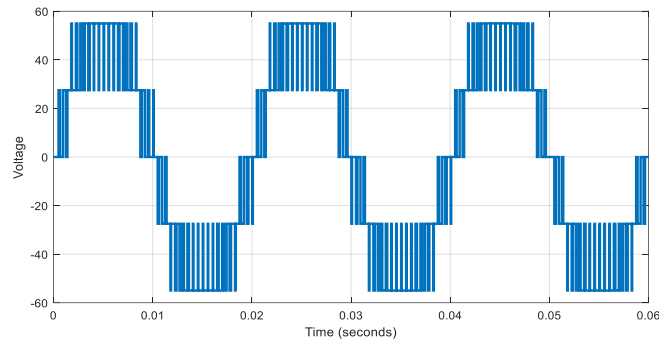


Figure 7. 5– level output voltage across one symmetrical hybridized MLI

Figure 7. shows the 5–level output voltage across one symmetrical hybridized MLI. Figure 8. shows the simulated waveforms of output voltage and load current with a R load for the 17-level inverter by selecting modulation index as 0.9 and a input source voltage $V_s = 55V$ for each cell. It is observed from Figure. 8 that generated output voltage wave from is much closure to sinusoidal from than the convention CHB MLI's.

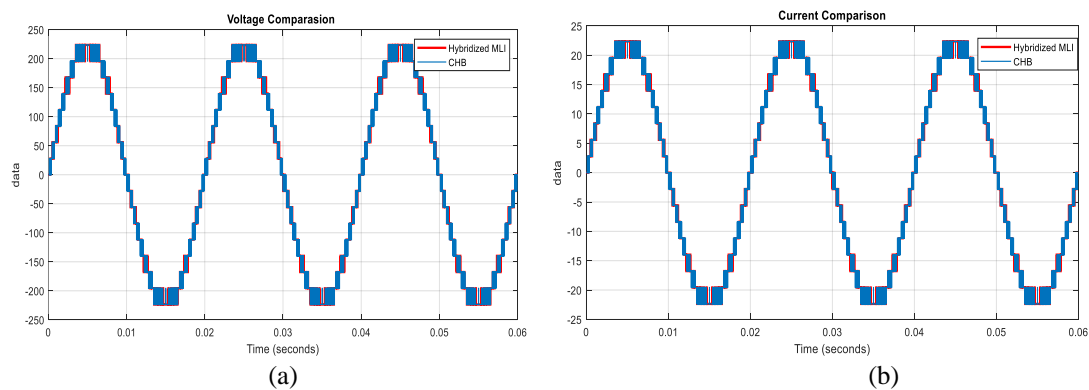


Figure 8. 17–Level output voltage and current waveform of hybridized MLI and CHB MLI
(a) comparison of generated output voltage (b) comparison of output current

The steady state testing has been performed with resistive load (unity power factor load) with 220 V peak to peak output voltages. The obtained output current is about 20A, peak to peak. The RMS value of the output voltage and current obtained are 155.56V and current 14.14A respectively.

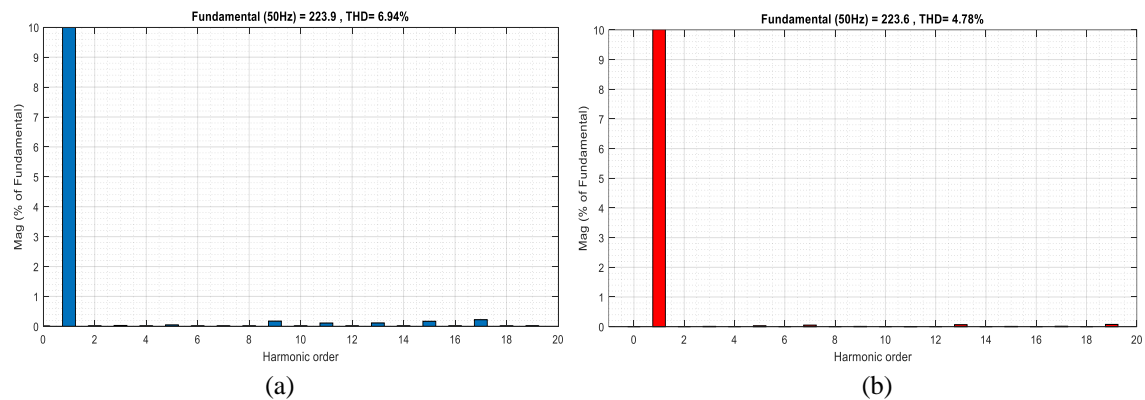


Figure 9. FFT spectrum of hybridized MLI and CHB MLI

Figure 9 shows the THD spectrum of the proposed hybridized multilevel inverter. From the Figure 9 (a) total THD is reduced than that of Figure 9 (b) due to the variation in the number of solid state switches in generating the same output levels.

Table 5 shows the comparison between proposed hybridized MLI and cascaded H bridge MLI. The percentage level of THD are low with the proposed topology for distinct level of voltage generation. From the table it is also evident that the proposed topology results in an improved output voltage in comparison to cascaded H Bridge MLI. Comparison between both the topologies are presented in Figure 10.

Table 5. Comparison of output voltage and THD for different levels

Level	Symmetric Hybridized MLI	Cascaded Hybridized MLI
5-Level		
Fundamental output voltage (Max)	218.7	215.4
THD	27.07%	29.65%
9-Level		
Fundamental output voltage (Max)	221.6	219.9
THD	12.94%	14.11%
13-Level		
Fundamental output voltage (Max)	220.1	219.2
THD	8.06%	9.45%
17-Level		
Fundamental output voltage (Max)	223.6	223.9
THD	4.78%	6.94%

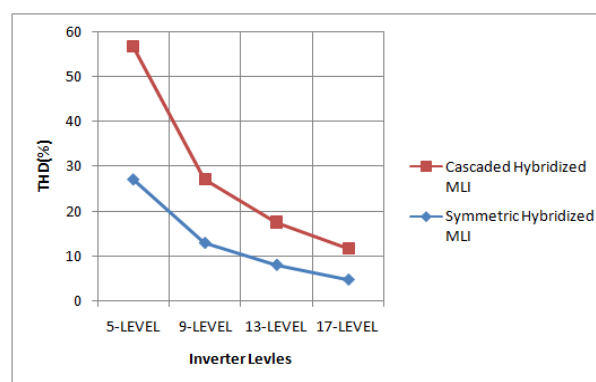


Figure 10. THD Comparison of symmetrical hybridized and cascaded hybridized MLI

5. CONCLUSION

A Hybridized MLI with stair case modulation scheme was proposed in this paper. It generates closure sinusoidal voltage at the output with a smaller number of solid-state switches. Two kinds of MLI's generating different output levels are tested by simulation. As the output levels increases the proposed topology considerably reduces switching devices when compared to the CHB MLI. Considerable advantages of the proposed topology are 1) As the number of levels are increased it generates output waveform closer to sinusoidal. 2) Few switching devices compared with the conventional MLI 3) Low THD 4) Low switching devices loss as device conduction time is reduced. Based on the above merits, the proposed Hybridised MLI with stair case modulation shows a better performance in comparison to convention MLI's

REFERENCES

- [1] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.
- [2] L. G. Franquelo, J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Trans. Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28-39, June, 2008.
- [3] A. Nami. "A New Multilevel Converter Configuration for High-Power High-Quality Application," *PhD Thesis*, Queensland University of Technology, 2010.
- [4] Thiagarajan V, Somasundaram P, "A New Seven Level Symmetrical Inverter with Reduced Switch Count," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, no. 2, pp. 921-925, Jun 2018.
- [5] I. López, S. Ceballos, J. Pou, J. Zaragoza, J. Andreu, I. Kortabarria and V. G. Agelidis, "Modulation strategy for multiphase Neutral-Point Clamped converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 928-941, March, 2015.
- [6] Motaparthi Nagaraju, Malligunta Kiran Kumar, "Analysis of series/parallel multilevel inverter with symmetrical and asymmetrical configurations," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, no. 1, pp. 300-306, Mar 2019.
- [7] V. Dargahi, A. K. Sadigh, M. Abarzadeh, S. Eskandari and K. Corzine, "A new family of modular multilevel converter based on modified flying capacitor multicell converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 138-147, January, 2015.
- [8] Y. Lei *et al.*, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570-8581, Nov. 2017.
- [9] Hema Latha Javvaji, Basavaraja Banakara, "Simulation & analysis of different parameters of various levels of cascaded H bridge multilevel inverter," *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (Prime Asia)*, 2013; 62-67.
- [10] E. Babaei, S. Laali, and S. Alilu, "Cascaded multilevel inverter with series connection of novel H-bridge basic units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6664-6671, Dec. 2014.
- [11] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3109-3118, Nov. 2011.
- [12] S. Kakar, S. M. Ayob, N. M. Nordin, M. S. Arif, A. Jusoh, N. D. Muhamad "A novel single-phase PWM asymmetrical multilevel inverter with number of semiconductor switches reduction," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, no. 3, pp. 1133-1140, Sep 2019.
- [13] B. P. Reddy, M. R. A. M. Sahoo, and S. Keerthipat, "A fault tolerant multilevel inverter for improving the performance of pole-phase modulated nine-phase induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1107-1116, July. 2017.
- [14] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2197-2206, August, 2010.
- [15] Lipika Nanda, A Dasgupta, U. K. Rout, "A comparative Analysis of Symmetrical and Asymmetrical Cascaded M ultilevel Inverter Having Reduced Number of Switches and DC Sources", *International Journal of Power Electronics and Drive System (IJPEDS)*, Vol. 8, No. 4, December 2017, pp. 1595-1602
- [16] C. I. Odeh, D. B. Nnadi, and E. S. Obe, "Three-phase, five-level multilevelinverter topology," *Electr. Power Compon. Syst.*, vol. 40, no. 4, pp. 1522-1532, 2012.
- [17] V. Sonti, S. Jain, and S. Bhattacharya, "Analysis of the modulation strategy for the minimization of the leakage current in the PV grid-connected cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1156-1169, Feb. 2017.
- [18] S. Sabyasachi, V. B. Borghate, R. R. Karasani, S. K. Maddugari, and H. M. Suryawanshi, "A fundamental frequency hybrid control technique based three phase cascaded multilevel inverter topology," *IEEE Access*, vol. 5, pp. 26912-26921, July. 2017.
- [19] Ibrahim Haruna Shanono, Nor Rul Hasma Abdullah, Aisha Muhammad, "9-Level Voltage Source Inverter Controlled Using Selective Harmonic Elimination", *International Journal of Power Electronics and Drives System (IJPEDS)*, Vol. 9, No. 3, September 2018, pp. 1251-1262
- [20] P. L. Kamani and A. M. Mulla, "Middle-level SHE pulse-amplitude modulation for cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2828-2833, August. 2017.
- [21] L. Wang, Q. H. Wu, and W. Tang, "Novel cascaded switched-diode multilevel inverter for renewable energy integration," *IEEE Trans. Energy Convers.*, vol. 32, no.4, pp. 1574-1582, Dec. 2017.

- [22] S. R. Raman, K. W. E. Cheng, and Y. Yuanmao, "Multi-input switched capacitor multilevel inverter for high-frequency ac power distribution," *IEEE Trans. Power Electron.*, vol. 33, no.7, pp. 5937-5984, August. 2017.
- [23] C. I. Odeh and D. B. N. Nnadi, "Single-phase, 17-level hybridized cascaded multi-level inverter," *Electr. Power Compon. Syst.*, vol. 41, no. 2, pp. 182-196, 2013.
- [24] M. F. M. Elias, N. A. Rahim, H. W. Ping, and M. N. Uddin, "Asymmetrical cascaded multilevel inverter based on transistor-clamped H-bridge power cell," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4281-4288, Nov./Dec. 2014.
- [25] Youssef Babkrani, Ahmed Naddami, Mohamed Hilal, "A smart cascaded H-bridge multilevel inverter with An optimized modulation techniques increasing the quality and reducing harmonics," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, no. 4, pp. 1852-1862, Dec 2019.
- [26] Y. Suresh and A. K. Panda, "Investigation on hybrid cascaded multilevel inverter with reduced dc sources," *Renew. Sustain. Energy Rev.*, vol. 26, pp. 49-59, Oct. 2013.
- [27] J. Dixon and L. Moran, "High-level multistep inverter optimization using a minimum number of power transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 330-337, Mar. 2006.
- [28] S.-J. Park, F.-S. Kang, M. H. Lee, and C.-U. Kim, "A new single phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 831-843, May 2003.
- [29] S. J. de Mesquita, F. L. M. Antunes, and S. Daher, "A high resolution output voltage multilevel inverter topology with few cascade-connected cells," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, pp. 289-296, Mar. 2014.
- [30] C. I. Odeh and D. B. N. Nnadi, "Single-phase 9-level hybridised cascaded multilevel inverter," *IET Power Electron.*, vol. 6, no. 3, pp. 468-477, 2013.
- [31] F.-S. Kang, S.-J. Park, S. E. Cho, C.-U. Kim, and T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906-915, Dec. 2005.
- [32] H. M. Basri1 and S. Mekhile, "Digital predictive current control of multilevel four-leg voltage-source inverter under balanced and unbalanced load conditions," *IET Electr. Power Appl.*, vol. 11, no. 8, pp. 1499-1508, 2017.

BIOGRAPHIES OF AUTHORS



Mrs. Hema Latha Javvaji received AMIETE degree from IETE, NewDelhi, M.Tech., from Madan Mohan Malviya Engineering College, Gorakhpur in 2001 and 2004 respectively. She is currently working towards the Ph. D degree at Acharya Nagarjuna University, under the guidance of Dr. B. Basavaraja. Presently she is working as Sr. Assistant Professor at PVP Siddhartha Institute of Technology, Vijayawada, Andhra Pradesh, India. Her research interests include power electronics, multilevel converters, modulation techniques and microcontrollers and DSP processors.
email: hemajavvaji@gmail.com



Dr. Basavaraja Banakara ME, MBA (HR), Ph.D (NITW), Senior Member EEE, LMISTE, SMIACSIT, MIAENG, Fellow IEI Executive Committee Member for ISTE Andhra Pradesh Section. He was born in 1970. He obtained his B.E (EEE) degree from Gulbarga University and M.E from Karnataka University, India and he is completed his Doctoral program from National Institute of Technology, Warangal, India. He worked as a Lecturer in VEC Bellary, Associate Professor at SSJ Engineering College Mahaboobnagar, Professor at SR Engineering College Ananthasagar, Waranagal, Principal at Padmasri Dr.BV Raju Institute of Technology, Narasapur, AP, India, Professor & Director for Academic Registration at KL University, Guntur, AP, India, Professor & Vice-Principal at GITAM University Hyderabad, AP, India, Professor and TPO at UBDTU, Davanagere .& Presently he is working as a Regestrar Davanagere University, Karnataka, India. His areas of interest include power electronics and drives, Power Quality, Micro-grids, High voltage Engineering and EMTP applications.
e-mail: banakara45@ubtec.org