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A dual-switch cubic SEPIC converter with extra high voltage gain

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ABSTRACT

To provide a high votage conversion ratio, conventional non-isolated DC-DC boost topologies, which have reduced voltage boost capability, have to operate with extremely high duty cycle ratio, higher than 0.9. This paper proposes a DC-DC converter which is mainly based on the narrow range of duty cycle ratio to achieve extra high voltage conversion gain at relatively reduced voltage stress on semiconductors. In addition, it does include any magnetic coupling structure. The structure of the proposed converter combines the new hybrid SEPIC converter and voltage multiplier cells. From the steady-state analysis, this converter has wide conversion ratio and cubic dependence with respect to the duty ratio and then, can increase the output voltage several times more than the conventional and quadratic converters at the same duty cycle ratio. However, the proposed dual-switch cubic SEPIC converter must withstand higher voltage stress on output switches. To overcome this drawback, an extension of the proposed converter is also introduced and discussed. The superiority of the proposed converter is mainly based on its cubic dependence on the duty cycle ratio that allows it to achieve extra high voltage gain at reduced voltage stress on semiconductors. Simulation results are shown and they corroborate the feasibility, practicality and validity of the concepts of the proposed converter.

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1. INTRODUCTION

Numerous applications for high step-up DC-DC converters have been reported so far, such as renewable energy systems (photovoltaic, wind, fuel cells, automotive industry, industrial applications, computer, uninterruptible power systems, telecommunications. The development of new power electronics circuits, in order to satisfy all these needs, is a topic of great interest, where the trends are wide conversion gains, high power density, improved efficiency and low cost [1], [2]. Typically, the 48 V DC of the battery bank has to be boosted to a 380 V in order to be connected to the DC bus in the information and telecommunication industry and the high intensity discharge (HID) lamps for automobile head lamp require at their start-up the increase of voltage from the battery's 12 V to more than 100 V, at 35 W power [3], [4].

The output voltage of fuel cells is very low. Then, a step-up DC-DC converter must follow a fuel cell stack in order to realize a useful power supply [5]. The photovoltaic arrays are sources with low output voltage. Moreover, the output voltage can be affected either by the weather or the partial shading. Series connections of photovoltaic cells or arrays are not actually a practical solution to obtain wide voltage. Thus, for grid connected applications, DC-DC converter needs to boost that low output voltage to high voltage [6], [7]. The interconnection of low voltage energy sources onto the higher voltage is difficult task. The conventional basic converters to achieve such a wide voltage gain, would lead to operate with extremely high duty ratio, higher than 0.9 (D>0.9). An extreme duty cycle impairs the efficiency and seriously affects the dynamic behaviour of the converter by imposing obstacle for transient response [8]. However, a very fast comparator, which is expensive, is required into the control loop in order to produce an extreme duty cycle. The extreme duty ratio may even cause malfunctions at high switching frequency due to the very short conduction time of the diode in step-up converters [8]. Also, they force fruitfully short off-times or low switching frequencies, which produce a severe diode reverse-recovery current and then, will increase the electromagnetic interferences (EMI) level. Low switching frequency causes higher ripple current and increases magnetic components [9]. Moreover, the voltage conversion gain is limited by the effect of power switch, rectifier diodes, parasitic resistances of inductor and capacitor, and saturation effects of the inductors and capacitors [8].

Several technologies and topologies of DC-DC converters to provide wide voltage gain are reported in the literature. The extreme high duty ratio operation could be avoided and the high step-up voltage achieved by using either isolated or non-isolated DC-DC converters. The isolated converters can provide high voltage gain by adjusting the turn's ratio of the high frequency transformer or the coupled inductors. However, they suffer high voltage spike, high circulating current and high voltage stress on output semiconductors caused by the leakage inductor [10]-[13]. The non-isolated converters can provide high voltage gain, either by increasing the turn's ratio of the coupled inductors or by the permutations and combinations of the various voltage booting techniques [14]. Many non-isolated and isolated step-up DC-DC converters have been reported in the literature [1], [14]-[16]. A classification of non-isolated with high gain DC-DC converters operating in CCM has been presented in [1]. In [1], step-up topologies with wide conversion ratios have been sorted into five types, namely: (1) cascaded boost converters, (2) coupled-inductor based boost converters, (3) switched capacitor based boost converters, (4) interleaved boost converters, and (5) three-state switching cell (3-SSC) based converters.

To achieve a high step-up voltage gain using non-isolated topologies without any magnetic coupling, the voltage boosting techniques have been used [14] has presented a categorization of voltage boosting techniques. They have been classified into five types, namely: (a) switched capacitor (charge pump), (b) voltage multiplier, (c) switched inductor and voltage lift, (d) magnetic coupling, and (e) multi-stage/-level structures. This categorization gives a view on how most of high step-up converters are constructed. Thus, in the purpose to enlarge the voltage gain and ameliorate the converter performance and efficiency, a number of converter arrangements have been derived and reported in the literature [14]-[16]. Basic boost DC-DC converters combined with voltage multiplier cells have been proposed to get families of converters possessing higher voltage gain in [17], [18]. In [19]-[21], basic DC-DC boost converters and switched capacitor/switched inductor structures have been combined to improve the voltage conversion gain. [22]-[24] have used the voltage lift technique with classical boost converters to achieve wide voltage ratios. The authors in [25]-[31] have substituted for inductors in the classical boost converter with voltage multiplier cells and obtained quadratic voltage conversion gains.

This paper proposes a dual-switch cubic SEPIC converter exhibiting an extra high voltage gain and moderate voltage stress on semiconductor switches. It consists of a voltage multiplier cell (VMC) and the hybrid SEPIC DC-DC converter in [19]. The proposed converter is a non-isolated converter without any magnetic coupling having a cubic dependence on the duty cycle D. The proposed converter has a higher voltage gain compared to the conventional and quadratic boost converters. The proposed converter has the following merits:

- Cubic dependence on the duty ratio allowing it to provide wide output-to-input conversion range at moderate duty cycle without any magnetic coupling,
- Relatively reduced voltage stress on active and passive switches except the output switches S_2 and D_o for $0.5<D<1$,
- The input and output terminals share a common ground.

This paper is organized as following: section 2 presents the structure and the operating principle of the proposed converter, section 3 details the steady-state analysis of the proposed converter, section 4 provides the efficiency analysis with parasitic parameters considered, the comparison with some quadratic converters is done in section 5, section 6 discusses the extension of the proposed converter so that the voltage stress on the output switches drops, section 7 presents the simulation results and section 8 concludes the paper.

2. PROPOSED CONVERTER AND OPERATING PRINCIPLE

The dual-switch cubic SEPIC converter is derived from the new hybrid SEPIC converter, despicted in Figure 1, by inserting in cascade between the input inductor and the main switch, a voltage multiplier cell as shown in Figure 2(a). The additional components allow the proposed converter to operate differently from the hybrid SEPIC Converter. The steady-state waveform under continuous conduction mode (CCM) and discontinuous inductor current mode (DICM) Operations is depicted in Figure 3 and, the corresponding modes are shown in Figure 2. To analyse the steady-state characteristics of the proposed converter, some conditions are assumed as follows: i) All components are ideal, ii) All capacitors are sufficiently large, and the voltages across the capacitors can be treated as constant.

For ease the analysis, the proposed converter is assumed to be lossless, so $P_{in}=P_{out}$ is held. Hence, the ESRs of inductors and capacitors and losses of the semiconductor's devices such as switches and diodes are not considered.

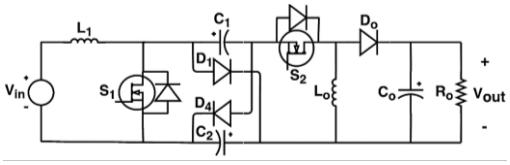

Figure 1. New hybrid SEPIC converter

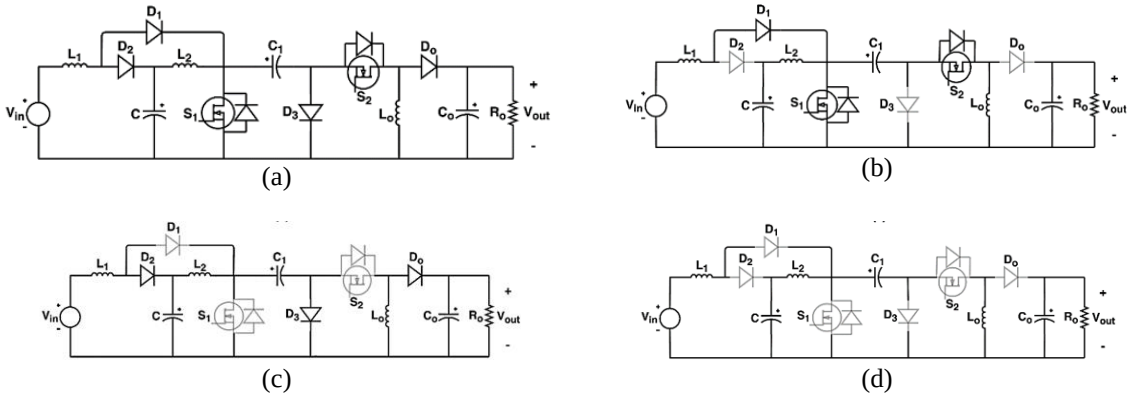

Figure 2. Dual-switch cubic SEPIC converter modes, (a) converter; (b) switches on; (c) switches off; (d) switches off in DICM

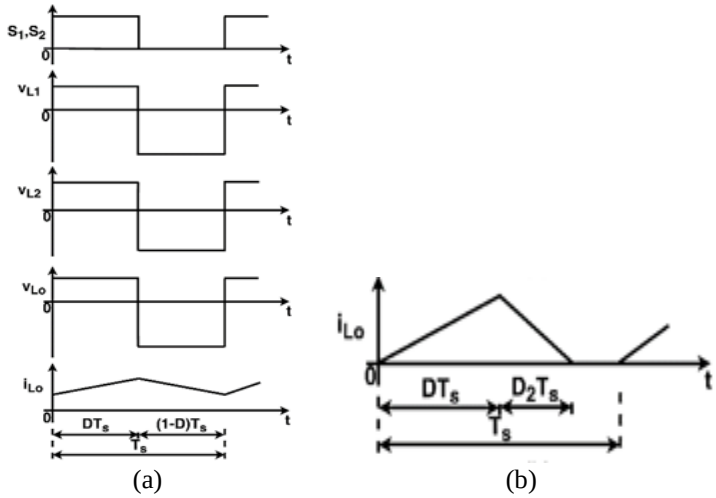

Figure 3. Key waveforms of the dual-switch cubic SEPIC converter; (a) CCM; (b) DICM

2.1. CCM operation

In CCM, the dual-switch cubic SEPIC converter goes through two topological modes, defined as modes 1 and 2, as shown in Figure 2(b) and (c) in each switching period.

Mode 1: At $t = t_0 = 0$, both power switches S_1 and S_2 are turned on, and diode D_1 is turned on, while diodes D_2, D_3, and the output diode Do are reverse biased, as shown in Figure 2(b). The currents through inductors L_1 and L_2 and, output inductor L_o increase linearly. The energy stored in the capacitor C is released to the inductor L_2, and the energy stored in the capacitors C_1 is released to the output inductor L_o, while the output capacitor C_o is supplied the load. Some of the main equations among the components in this mode are given as (1),

$$\begin{cases} v_{L_1} = v_{in} \\ v_{L_2} = v_C \\ v_{L_o} = v_{C_1} \end{cases} \quad (1)$$

And (2)

$$\begin{cases} i_C = -i_{L_2} \\ i_{C_1} = -i_{L_o} \\ i_{C_o} = -v_{out}/R_o \end{cases} \quad (2)$$

Mode 2: At $t = t_1 = DT_s$, both power switches S_1 and S_2 are turned off, and diode D_1 is reverse biased, while diodes D_2, D_3, and the output diode Do are forward biased, as shown in Figure 2(c). The currents through inductors L_1 and L_2 decrease linearly. The energy stored in the output inductor Lo is released to the output capacitor C_o and the load, while the energy stored in L_1 and L_2 with the source energy V_{in} are released to charge the capacitors C and C_1. Thus, the voltages across L_1, L_2 and L_o, the currents through C, C_1 and C_o are given as (3),

$$\begin{cases} v_{L_1} = v_{in} - v_C \\ v_{L_2} = v_C - v_{C_1} \\ v_{L_o} = -v_{out} \end{cases} \quad (3)$$

and (4)

$$\begin{cases} i_C = i_{L_1} - i_{L_2} \\ i_{C_1} = i_{L_2} \\ i_{C_o} = i_{L_o} - v_{out}/R_o \end{cases} \quad (4)$$

2.2. DICM operation

In DICM, the operating modes can be divided into three modes defined as modes 1, 2, and 3.

Mode 1. The operating principle is the same as that for mode 1 of the CCM operation.

Mode 2. The operating principle is the same as that for mode 2 of the CCM operation.

Mode 3. At $t = t_2 = (D + D_2)T_s$, both power switches S_1 and S_2 are still turned off, and diode D_1 is still reverse biased, while diodes D_2, D_3, and the output diode Do are turned off, as shown in Figure 2(d). The energies stored in inductors L_1, L_2 and L_o are zero. Thus, only the energy stored in C_o is discharged to the load.

3. STEADY-STATE PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

By using the volt-second balance principle on inductors and ampere-second balance principle on capacitors, the following equations are derived as (5),

$$\begin{cases} DV_{in} + (V_{in} - V_C)(1 - D) = 0 \\ DV_C + (V_C - V_{C_1})(1 - D) = 0 \\ DV_{C_1} - V_{out}(1 - D) = 0 \end{cases} \quad (5)$$

and (6)

$$\begin{cases} -DI_{L_2} + (I_{L_1} - I_{L_2})(1 - D) = 0 \\ -DI_{L_o} + I_{L_2}(1 - D) = 0 \\ -DI_{out} + (I_{L_o} - I_{out})(1 - D) = 0 \end{cases} \quad (6)$$

3.1. Ideal voltage conversion ratio in CCM

By solving (5), the output voltage and the voltages of the capacitors can be derived as,

$$V_C = \frac{1}{1-D} V_{in} \tag{7}$$

$$V_{C_1} = \frac{1}{(1-D)^2} V_{in} \tag{8}$$

$$V_{out} = \frac{D}{(1-D)^3} V_{in} \tag{9}$$

Hence, from (9), the ideal voltage conversion gain is given by (10);

$$M_{CCM} = \frac{V_{out}}{V_{in}} = \frac{D}{(1-D)^3} \tag{10}$$

According to (10), the ideal voltage gain of the proposed converter is a cubic function of the duty cycle D. So, this converter can provide wide voltage conversion ratio range. Moreover, the proposed converter can operate either in step-up mode or in step-down mode. If the duty cycle D>0.317, the voltage gain is greater than 1, it operates in step-up mode. Otherwise, it operates in step-down mode.

3.2. Ideal voltage conversion ratio in DICM

By solving equations from volt-second balance principle on each inductor, we derive the voltages of capacitors and the ideal output voltage as (11),

$$\begin{cases} V_C = \frac{D+D_2}{D_2} V_{in} \\ V_{C_1} = \left(\frac{D+D_2}{D_2}\right)^2 V_{in} \\ V_{out} = \frac{D}{D_2}\left(\frac{D+D_2}{D_2}\right)^2 V_{in} \end{cases} \tag{11}$$

From (11), M_{DICM} is derived as (12)

$$M_{DICM} = \frac{V_{out}}{V_{in}} = \frac{D}{D_2}\left(\frac{D+D_2}{D_2}\right)^2 \tag{12}$$

From Figure 3(b), the average value of the output diode current I_{D_o} is given by;

$$I_{D_o} = \frac{1}{2} I_{D_{max}} D_2 = \frac{1}{2} \frac{V_{C_1}}{L_o} D T_s D_2 = \frac{V_{in} T_s}{2L_o} \frac{D}{D_2} (D + D_2)^2 \tag{13}$$

I_{D_o} is equal to the average load current I_o. Thus,

$$\frac{V_{in} T_s}{2L_o} \frac{D}{D_2} (D + D_2)^2 = \frac{V_o}{R_o} \tag{14}$$

By substituting (12) into (14), we get;

$$D_2 = \sqrt{\frac{2L_o}{R_o T_s}} \tag{15}$$

Then, the normalized inductor time constant is defined as (16);

$$k_L = \frac{2L_o}{R_o T_s} \tag{16}$$

By substituting (15) into (12), the voltage gain is given by (17);

$$M_{DICM} = \frac{V_o}{V_{in}} = \frac{2D}{\sqrt{k_L}}\left(1 + \frac{D}{\sqrt{k_L}}\right)^2 \tag{17}$$

3.3. Boundary operating condition between CCM and DICM

In boundary conduction mode (BCM), the voltage gain of the CCM operation is equal to the voltage gain of the DICM operation. From (11) and (20), the boundary normalized inductor time constant k_{LB} can be derived as (18);

$$k_{LB} = (1 - D)^2 \tag{18}$$

The Dual-Switch Cubic SEPIC converter will operate in CCM if k_L is larger than k_{LB}. It will operate in DICM if D_2<(1-D), that is, k_L<$(1-D)^2$.

3.4. Voltage stresses on power switches and diodes

The voltage stress on the semiconductor components is calculated during their turn-off state. The normalized voltage stresses on S_1, S_2, D_1, D_2, D_3 and D_o are derived as (19) and (20),

$$\begin{cases} V_{S_1} = \frac{1-D}{D} \\ V_{S_2} = 1 \end{cases} \tag{19}$$

$$\begin{cases} V_{D_1} = 1 - D \\ V_{D_2} = \frac{(1-D)^2}{D} \\ V_{D_3} = \frac{1-D}{D} \\ V_{D_o} = \frac{1}{D} \end{cases} \tag{20}$$

The normalized voltage stresses on the active and passive switches of the Dual-Switch Cubic SEPIC converter are plotted in Figure 4. Since the proposed converter can achieve high voltage gain when the duty cycle ratio lies in the range 0.5<D<1, the voltage stresses on semiconductor switches, except for output passive switch D_o, are less or equal to the output voltage as shown in Figure 4.

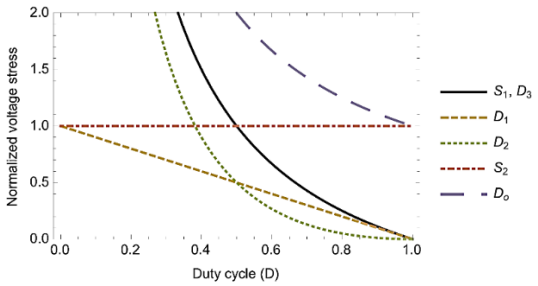

Figure 1. Normalized voltage stresses as a function of duty cycle D

3.4. Current stresses on power switches and diodes

From the charge balance (6), the average currents of the inductors L_1, L_2 and L_o, namely, I_{L_1}, I_{L_2} and I_{L_o} can be calculated as (21), (22), (23),

$$I_{L_1} = \frac{D}{(1-D)^3} I_o \tag{21}$$

$$I_{L_2} = \frac{D}{(1-D)^2} I_o \tag{22}$$

$$I_{L_o} = \frac{1}{1-D} I_o \tag{23}$$

The normalized DC current stresses of the two power switches (S_1 and S_2) and the four diodes (D_1, D_2, D_3 and D_o can be derived as (24) and (25),

$$\begin{cases} I_{S_1} = \frac{D}{(1-D)^3} \\ I_{S_2} = \frac{D}{1-D} \end{cases} \quad (24)$$

$$\begin{cases} I_{D_1} = \frac{D^2}{(1-D)^3} \\ I_{D_2} = \frac{D}{(1-D)^2} \\ I_{D_3} = \frac{D}{1-D} \\ I_{D_o} = 1 \end{cases} \quad (25)$$

3.1. Currents of the inductors

The peak-to-peak current ripples of the inductor currents i_{L_1}, i_{L_2} and i_{L_o} can be given as (26), (27), and (28),

$$\Delta i_{L_1} = \frac{DV_{in}}{L_1 f_s} \quad (26)$$

$$\Delta i_{L_2} = \frac{DV_{in}}{(1-D)L_2 f_s} \quad (27)$$

$$\Delta i_{L_o} = \frac{DV_{in}}{(1-D)^2 L_o f_s} \quad (28)$$

where f_s is the switching frequency.

3.2. Voltages of the capacitors

The peak voltage ripples of the capacitor voltages v_C, v_{C_1} and v_{C_0} can be deduced as (29), (30), and (31),

$$\Delta v_C = \frac{D^2 I_o}{(1-D)^2 C f_s} \quad (29)$$

$$\Delta v_{C_1} = \frac{DI_o}{(1-D)C_1 f_s} \quad (30)$$

$$\Delta v_{C_o} = \frac{R_o(1-D)I_o}{8L_o C_o f_s^2} \quad (31)$$

4. EFFICIENCY ANALYSIS CONSIDERING THE PARASITIC PARAMETERS

The theoretical analysis above is based on ideal components, i.e. without parasitic parameters. However, the design of converter must consider inductor and capacitor copper losses due to the ESRs of inductors and capacitors, respectively, power loss in the active switches and power loss in the passive switches. In order to facilitate calculations, the voltage and current ripples of inductors and capacitors are neglected.

4.1. Power losses of inductors

The loss in the inductors consists of the copper loss and the core loss. The inductor copper loss is caused by ESRs r_{L_1}, r_{L_2} and r_{L_o} of inductors L_1, L_2 and L_o, respectively, and can be deduced by,

$$P_{cu} = r_{L_1} I_{L_{1(rms)}}^2 + r_{L_2} I_{L_{2(rms)}}^2 + r_{L_o} I_{L_{o(rms)}}^2 \quad (32)$$

hence,

$$P_{cu} = \left[\frac{D^2 r_{L_1}}{(1-D)^6 R_o} + \frac{D^2 r_{L_2}}{(1-D)^4 R_o} + \frac{r_{L_o}}{(1-D)^2 R_o} \right] P_{out} \quad (33)$$

From [30], the core loss in the magnetic circuit of inductors is deduced by,

$$P_{core} = P_{fe_1} + P_{fe_2} + P_{fe_o} = a_1 B_1^b f_1^c l_{m_1} A_{c_1} + a_2 B_2^b f_2^c l_{m_2} A_{c_2} + a_o B_o^b f_o^c l_{m_o} A_{c_o} \quad (34)$$

where a, b and c are obtained from the datasheets; B is the half of the AC flux; f is the frequency; A_c is the area of the core; and l_m is the mean length of the core. Thus, the overall power losses of inductors are obtained by,

$$P_L = P_{cu} + P_{core} \tag{35}$$

4.2. Power losses of capacitors

The capacitor copper loss is caused by ESRs r_C, r_{C_1} and r_{C_o} of capacitors C, C_1 and C_o, respectively. The rms of currents i_C, i_{C_1} and i_{C_o} are calculated as (36),

$$P_C = r_C I_{C_{(rms)}}^2 + r_{C_1} I_{C_{1(rms)}}^2 + r_{C_o} I_{C_{o(rms)}}^2 \tag{36}$$

the rms values of currents through the capacitors are:

$$\begin{cases} I_{C_{rms}} = \frac{D^{3/2}}{(1-D)^{5/2}} I_{out} \\ I_{C_{1(rms)}} = \frac{D^{1/2}}{(1-D)^{3/2}} I_{out} \\ I_{C_{o(rms)}} = \frac{D^{1/2}}{(1-D)^{1/2}} I_{out} \end{cases} \tag{37}$$

thus, the power loss in the capacitors are calculated by (38)

$$P_C = \left[\frac{D^3 r_C}{(1-D)^5 R_o} + \frac{D r_{C_1}}{(1-D)^3 R_o} + \frac{D r_{C_o}}{(1-D) R_o}\right] P_{out} \tag{38}$$

4.3. Power losses of power switches

The power loss in the power switches is divided into two parts: the conduction loss and the switching loss. The conduction loss occurs during the ON-state caused by the ON-resistances r_{ON_1} and r_{ON_2} of the power switches S_1 and S_2, respectively, and can be calculated as (39),

$$P_{S_{cond}} = r_{ON_1} I_{S_{1(rms)}}^2 + r_{ON_2} I_{S_{2(rms)}}^2 \tag{39}$$

The rms values of currents flowing through the power switches are given by

$$\begin{cases} I_{S_{1(rms)}} = \frac{D^{1/2}}{(1-D)^3} I_{out} \\ I_{S_{2(rms)}} = \frac{D^{1/2}}{1-D} I_{out} \end{cases} \tag{40}$$

So, the conduction loss can be evaluated by

$$P_{S_{cond}} = \left[\frac{D r_{ON_1}}{(1-D)^6 R_o} + \frac{D r_{ON_2}}{(1-D)^2 R_o}\right] P_{out} \tag{41}$$

The switching loss occurs during the ON-OFF transitions of power switches and can be calculated as (42),

$$P_{S_{switching}} = \frac{1}{2} f_s C_{S_1} V_{S_1}^2 + \frac{1}{2} f_s C_{S_2} V_{S_2}^2 \tag{42}$$

So, the overall power loss in the active power switches is (43)

$$P_S = P_{S_{cond}} + P_{S_{switching}} \tag{43}$$

4.4. Power losses of diodes

The power loss in the diodes is caused by the forward resistances r_{D_1}, r_{D_2}, r_{D_3} and r_{D_o}, then by the threshold voltages V_{F_1}, V_{F_2}, V_{F_3} and V_{F_o} of diodes D_1, D_2, D_3 and D_o, respectively. The rms value of currents through the diodes are given by

$$\begin{cases} I_{D_{1(rms)}} = \frac{D^{3/2}}{(1-D)^3} I_{out} \\ I_{D_{2(rms)}} = \frac{D}{(1-D)^{5/2}} I_{out} \\ I_{D_{3(rms)}} = \frac{D}{(1-D)^{3/2}} I_{out} \\ I_{D_{o(rms)}} = \frac{1}{(1-D)^{1/2}} I_{out} \end{cases} \quad (44)$$

The power loss due to the forward resistance of the diodes is expressed as (45)

$$P_{cu} = r_{D_1} I^2_{D_{1(rms)}} + r_{D_2} I^2_{D_{2(rms)}} + r_{D_3} I^2_{D_{3(rms)}} + r_{D_o} I^2_{D_{o(rms)}} \quad (45)$$

The power loss due to the threshold voltage of the diodes is expressed as (46)

$$P_{av} = V_{F_1} I_{D_1} + V_{F_2} I_{D_2} + V_{F_3} I_{D_3} + V_{F_o} I_{D_o} \quad (46)$$

Hence, the overall power loss in the diodes gives

$$P_D = P_{cu} + P_{av} \quad (47)$$

4.5. Efficiency

The relatively accurate estimation of the efficiency η can be calculated as (48)

$$\eta = \frac{P_o}{P_o + \Sigma P_{loss}} \times 100 = \frac{P_o}{P_o + P_L + P_C + P_S + P_D} \times 100 \quad (48)$$

5. COMPARISON WITH SOME QUADRATIC CONVERTERS

The comparison, in order to verify some key steady-state features of the dual-switch cubic SEPIC converter with some quadratic converters in the literature, namely, the number of components, voltage gains and voltage stresses of the switches and diodes is presented in Table 1. From the Table 1, the proposed converter utilises the same number and the higher number of components, respectively, with the converter in [29] and the converters in [19], [31]. However, it has the widest voltage conversion gain for 0.5<D<1 with the same input voltage, as shown in Figure 5. Compared to the the converters in [29] and [31], the proposed converter has the lower voltage stresses on their switches and diodes for the duty cycle lies in the range 0.5<D<1, except the output diode D_o.

Table 1. Comparison between the proposed converter and some existing converters

Topology	Converter in [31]	Converter in [19]	Converter in [29]	Proposed Converter
Switches	2	2	1	2
Diodes	2	3	5	4
Inductors	2	2	3	3
Capacitors	2	3	3	3
Ideal Voltage Conversion Gain M_{CCM}	$\left(\frac{D}{1-D}\right)^2$	$\frac{2D}{(1-D)^2}$	$\left(\frac{D}{1-D}\right)^2$	$\frac{D}{(1-D)^3}$
Normalized Voltage Stresses of the Switches	$S_1 : \frac{1-D}{D^2}$ $S_2 : \frac{1}{D}$	$S_1 : \frac{1-D}{2D}$ $S_2 : \frac{1+D}{2D}$	$S : \frac{1}{D^2}$	$S_1 : \frac{1-D}{D}$ $S_2 : 1$
Normalized Voltage Stresses of the Diodes	$D_1 : \frac{1-D}{D^2}$ $D_0 : \frac{1}{D}$	$D_1 : \frac{1-D}{2D}$ $D_2 : \frac{1+D}{2D}$ $D_0 : \frac{1}{D}$	$D_1 : \frac{1-D}{D^2}$ $D_2 : \frac{1}{D}$ $D_3 : \frac{1}{D^2}$ $D_4 : \frac{1-D}{D^2}$ $D_0 : \frac{1}{D}$	$D_1 : 1-D$ $D_2 : \frac{(1-D)^2}{D}$ $D_3 : \frac{1-D}{D}$ $D_0 : \frac{1}{D}$

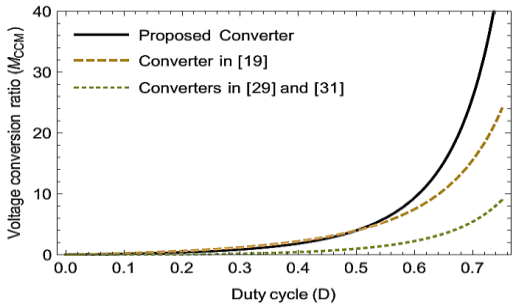

Figure 5. Ideal voltage gain M as a function of duty cycle D

6. EXTENSION OF THE DUAL-SWITCH CUBIC SEPIC CONVERTER

The extension of the dual-switch cubic SEPIC converter improves the voltage gain and reduces the voltage stresses across the output switches. It is obtained by adding a voltage multiplier rectifier which consists of diode and capacitor at its output as shown in Figure 6. It shall be noted that the voltage gain can further be improved by inserting additional voltage multiplier cells. The voltage gain of the extension of the dual-switch cubic SEPIC converter can be easily derived as

$$M = \frac{V_o}{V_{in}} = \frac{1}{(1-D)^3} \tag{49}$$

The normalized voltage stresses on output switches S_2 and D_o of the extended proposed converter are derived as

$$\begin{cases} V_{S_2} = 1 - D \\ V_{D_o} = V_{D_4} = 1 \end{cases} \tag{50}$$

One notice that the normalized voltage stresses on output switches are at most equal to V_o.
The merits of the proposed extension are:

– High voltage conversion gain
– Reduce voltage stress on output switches (S_2, D_4 and D_o)

The inconvenient, if we can consider it as such, is the increase in number of the component elements, namely, diode D_4 and capacitor C_3 as illustrated in Figure 6(a).

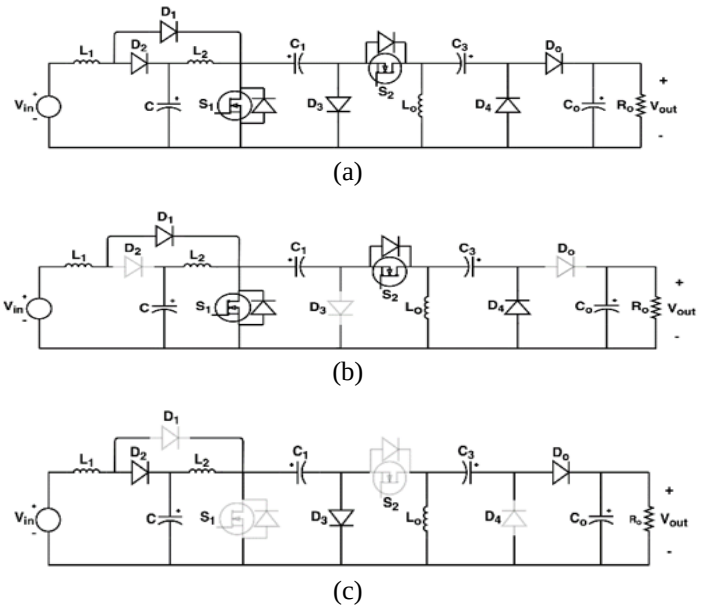

Figure 6. Extension of the dual-switch cubic SEPIC converter; (a) converter; (b) switches on; (c) switches off

7. SIMULATION RESULTS

The proposed converter in Figure 2(a) has been simulated using MATLAB/Simulink to validate the theoretical results that were obtained in Section 2. The proposed converter is simulated for the following specifications: $V_{in} = 20\,V$, $V_{out} = 400\,V$, $P_{out} = 280\,W$ and $f_s = 40\,kHz$. The nominal voltage conversion ratio and the duty ratio from (11) are: $M_{CCM} = 20$ and $D = 0.676$, respectively. The values of the passive components have been selected based on (26), (27), (28), (29), (30) and (31), then calculated for $\Delta v/V = 1\%$ and $\Delta i/I = 1\%$. The simulations have been done using the following values: $L_1 = 250\,\mu H$, $L_2 = 2.5\,mH$, $L_o = 15\,mH$, $C = 150\,\mu F$, $C_1 = 22\,\mu F$, $C_o = 2.2\,\mu F$ and $R_o = 570\,\Omega$. Figure 7 and Figure 11 present the simulated output voltage and current waveforms with average voltage of 400 V and 0.7 A respectively, for an input voltage of 20 V which is in accordance with the specifications. Figure 8, Figure 9, and Figure 10 show the simulated inductor current waveforms i_{L_1}, $i_{L_2}$and i_{L_o}, which show that the converter works in CCM. Moreover, the average currents i_{L_1}, $i_{L_2}$and i_{L_o} are 14 A, 4.5A and 2.2 A respectively, which are in accordance with the obtained values from the analytical (21), (22) and (23). These results were expected from the analysis, and show the feasibility of the proposed converter.

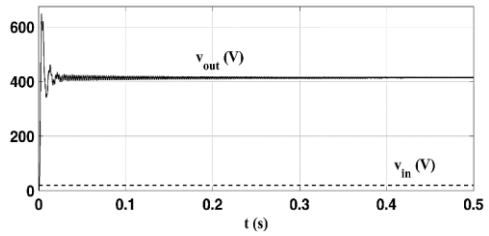

Figure 7. Input and Output voltage waveforms of the proposed converter in Figure 2(a)

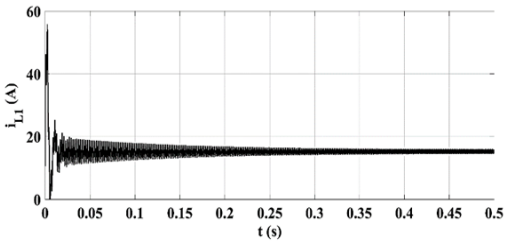

Figure 8. Input current waveform of the proposed converter in Figure 2(a)

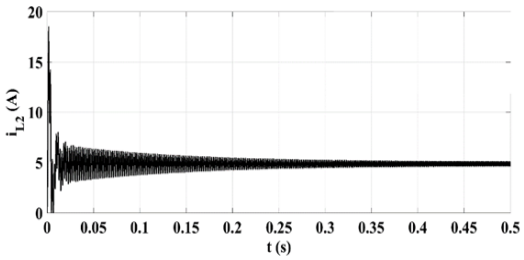

Figure 9. Inductor current waveform through L2 of the proposed converter in Figure 2(a)

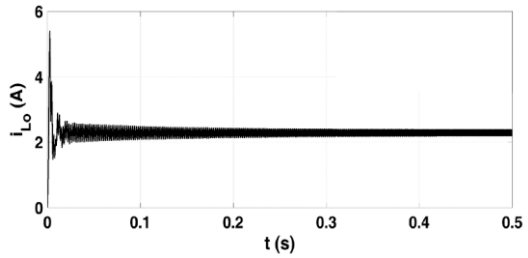

Figure 10. Inductor current waveform through Lo of the proposed converter in Figure 2(a)

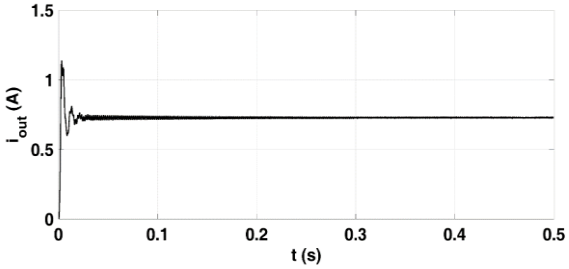

Figure 11. Output current of the proposed converter in Figure 2(a)

8. CONCLUSION

This paper proposes a dual-switch cubic SEPIC converter and performs the steady-state analysis. In order to improve the voltage stress on output semiconductors, an extension of the proposed converter is presented and steady-state analysis done. The detail comparative analysis of this configuration is done with

respect to their voltage gains, voltage stresses on the switches and diodes, and numbers of components. The characteristics of the converter are as following: a) The proposed converter has a cubic dependence with respect to the duty ratio that allows them to provide extra high voltage conversion gain which is an operable solution for high voltage applications, and also helpful to reduce the current stress through the switches. b) The voltage multiplier cells are important to obtain the voltage gain that the system required, also, to reduce the voltage stress on semiconductors switches. Then, the efficiency is improved. c) The voltage stresses on the switches and the diodes of the proposed converter are relatively low compared to some quadratic converters. In order to validate the theoretical analysis, MATLAB simulation has been achieved and the simulation results have been provided. These results support the theoretical analysis and speak the feasibility of the proposed converter.

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