❒   1660

Reduction of single DC bus capacitance in photovoltaic cascaded multilevel converter

Turki Kahawish Hassan
Department of Electrical Engineering, College of Engineering, University of Mustansiriyah, Iraq

Article Info	**ABSTRACT**

This paper presented single DC bus single phase seven level cascaded H-bridge (CHB) inverter for multi-panel photovoltaic grid-connected applications. A single DC bus supplying flyback converters to produce DC link voltages for CHB cells is suggested. A balanced operation of CHB inverter cells is obtained irrespective to power unbalance occurred by individual maximum power point tracking boost converter of photovoltaic (PV) panels due to the non-uniform irradiation and partial shading. A DC bus voltage control system with addition of estimated DC bus ripple voltage to the reference is proposed to eliminate the second order harmonic contained in the feedback voltage of DC bus enabling to design high bandwidth of DC voltage control loop. This produces fast dynamic response, low total harmonic distortion (THD) of grid current and smaller DC bus capacitance. Mathematical modeling of bus voltage control system is presented. PSIM simulation program is used and the simulation results are obtained to validate the proposed control system.

Corresponding Author:

Turki K. Hassan,
Department of Electrical Engineering, College of Engineering
Mustansiriyah University, Iraq
Email: thassan2013@yahoo.com

1. INTRODUCTION

The cascaded H-bridge multilevel inverter topology is one of commonly used converters in photovoltaic (PV) systems because of its modularity, simpler layout, higher efficiency and power quality with no clamping diodes or voltage balancing capacitors [1]. A major drawback of CHB inverter is the inherent unbalanced power among each cell causing unbalanced output power from different phases of inverter when the PV panels or strings that are connected to CHB cells suffer from non-uniform irradiation and partial shading. Many authors studied the control of this type of PV systems in the cases of single-phase converters when unbalanced power from cells supplied by PV panels are to be considered [2], [3] and unbalanced phases power for three-phase systems [4-12].

A controlled exchange of reactive power is proposed in [13] to inject balanced power to the grid so that the converter can work with unbalanced power generation within the clusters of each phase. The problem of power balancing is not completely solved especially under operation at rated conditions since balancing mechanisms are introduced in the modulation stage which could cause over modulation [10].

The per-phase and per-cell unbalanced powers are eliminated by collecting the total generated PV power in a single DC bus [14-16].

In single phase applications a large capacitor is connected across the DC bus to minimize the double frequency ripple and fluctuations in DC bus voltage [15]. The double frequency ripple is naturally produced in the single phase grid-connected converters, such ripple distorts the reference for output current in control

loop. The DC bus voltage fluctuations are due to random changes in the input power of PV system. The life time of large DC bus electrolytic capacitor is typically between 1000-7000 hours at 105°C operating temperature, therefore the life span of PV converters is limited. Many researchers have proposed various methods to reduce the size of the required DC bus capacitor of single phase inverters. In [17], band stop filter is used in DC bus voltage control loop to reduce harmonics of inverter current supplied to grid resulting smaller required DC bus capacitor. In [18], bi-directional converter with load of small capacitor is used to control ripple power. An auxiliary circuit is used in [19, 20] for ripple energy control in order to reduce the energy storage capacitance. The relationships between the oscillations due to single-phase switching and the DC link energy storage capacitor for PV grid-connected inverter are investigated in [21] without any suggestion to reduce it. A digital FIR filter that gives a notch to remove second order harmonic is proposed in [22] resulting a design of inverters with small DC bus capacitance. All above methods allow for longer life span capacitors, such as film capacitors, to be used, but with extra active devices, passive components or band stop filters. This increases the system complexity and cost.

The aim of this paper is to present single DC bus single phase seven level inverter with three PV panels and small DC bus capacitance. An individual P&O maximum power point tracking boost converter is applied for each PV panel. An intermediate isolated flyback DC-DC converter stages are applied between single DC bus and CHB inverter cells to produce DC link voltage for each cell and decouple the PV system from grid-tie inverter. This arrangement produces balanced operation of CHB cells. To reduce the DC bus capacitance without extra components or filters, the ripple voltage of DC bus is estimated and added to reference voltage to eliminate the second order harmonic from error signal that is applied to proportional-integral DC bus voltage controller. This gives grid current amplitude with very small ripple and smaller required DC bus capacitance. Using small DC bus capacitance increases the life time of converter, reducing the cost and design the DC bus voltage controller to produce fast dynamic response control system.

The paper is organized as follows: the structure of seven level cascaded H-bridge inverter with single DC bus is presented in section 2. The control scheme is demonstrated in section 3. Analysis and modeling of the DC bus voltage control loop is explained in section 4. The results of proposed photovoltaic system is shown in section 5. And finally, conclusion is presented in Section 6.

2. STRUCTURE OF SEVEN LEVEL CASCADED H-BRIDGE INVERTER WITH SINGLE DC BUS

The PV multi-panel single DC bus single phase cascaded H-Bridge (CHB) seven level inverter is shown in Figure 1. Each PV panel is connected to non-isolated boost DC-DC converter in order to raise the PV voltage and to perform maximum power point tracking (MPPT). The output of each boost converter is connected to single DC bus. For seven level inverter, there are three H-bridge cells, each one is fed from isolated DC source. For this purpose a flyback DC-DC converters are connected between the single DC bus and individual DC links of CHB cells of seven level inverter. The advantages of this structure is equally distributed output power between the cells of CHB.

3. CONTROL SCHEME

The control of each boost converter to perform a perturb and observe (P&O) maximum power point tracking (MPPT) [23] is shown in Figure 2. The PV panel voltage (V_{pvk}) and current (i_{pvk}) are sensed and used to perform the MPPT and generation the reference voltage ($V_{pv,ref}$) which is compared with (V_{pvk}). A proportional-integral controller is used to give the required duty cycle for pulse width modulation to obtain control pulses for boost converter transistor.

Figure 3 shows the closed loop control of output DC voltage of each one of three flyback converters (V_{dck}). The DC link voltage of each H-bridge cell is regulated to fixed value. The duty cycle of flyback transistor is varied through the pulse width modulation depending on the output of proportional-integral (PI) controller.

In this paper, the ripple voltage (v_{ripple}) of DC bus is estimated and added to the reference voltage ($V_{bus,ref}$) to cancel the ripple voltage contained in the feedback voltage (V_{bus}) enabling to design high bandwidth of DC voltage control loop so a faster dynamic response of DC bus voltage can be achieved. Smaller capacitor can be used in the common DC bus.

The derivation to determine the ripple voltage of DC bus as follows:
The input power that appears in the common bus is

$$P_{dc} = P_{pv} + C_{bus}V_{bus}\frac{dv_{ripple}}{dt} \tag{1}$$

Where P_{pv}, V_{bus} and C_{bus} are total power of all photovoltaic panels, steady state average voltage of single DC bus and DC bus capacitance respectively.

The output power at ac side (assuming unity power factor) can be written as

$$P_{ac} = V_g^\wedge \sin(\boldsymbol{\omega} t) \cdot I_g^\wedge \sin(\omega t) = \frac{V_g^\wedge I_g^\wedge}{2} - \frac{V_g^\wedge I_g^\wedge}{2} \cos(2\omega t) \tag{2}$$

Where $V_g^\wedge$ and $I_g^\wedge$ are the amplitudes of grid voltage and current respectively.

For lossless converter, the DC components of P_{dc} and P_{ac} which are P_{pv} and $\frac{V_g^\wedge I_g^\wedge}{2}$ respectively are equal and $P_{dc} = P_{ac}$ .Then

$$C_{bus} V_{bus} \frac{dv_{ripple}}{dt} = -\frac{V_g^\wedge I_g^\wedge}{2} \cos(2\omega t) \tag{3}$$

Integration and arrangement of equation (3) gives

$$v_{ripple} = -\frac{V_g^\wedge I_g^\wedge}{4\omega C_{bus} V_{bus}} \sin(2\omega t) = -\frac{P_{pv}}{2\omega C_{bus} V_{bus,ref}} \sin(2\omega t) \tag{4}$$

Where $V_{bus,\ ref}$ and V_{bus} are equal at steady state, ω is the grid frequency in rad/s and P_{pv} is the sum of individual photovoltaic power of three PV panels obtained by P&O maximum power point tracker. Phase locked loop (PLL) synchronized with grid is used to obtain unity sinusoidal signal with double frequency ($\sin(2\omega t)$). As shown in equation (4) $\sin(2\omega t)$ and P_{pv} are multiplied and divided by a constant ($2\omega C_{bus} V_{bus,ref}$) to estimate the ripple of DC bus voltage (v_{ripple}).

The amplitude of reference current ($I_{g,\ ref}$) produced by DC bus voltage PI controller is multiplied by v_{PLL} which is unity sinusoidal signal ($\sin(\omega t)$) obtained from PLL and synchronized with grid to give sinusoidal reference of grid current (i_{ref}). The grid current (i_g) is measured and subtracted from reference then the error signal is applied to proportional resonant controller (PR) that is used instead of a proportional integral controller in order to eliminate the frequencies other than 50Hz from the current [24]. A phase-shifted modulation scheme (PS-PWM) is used to get low total harmonic distortion and balanced power distribution among CHB cells [25]. The control scheme of cascaded H-bridge multilevel inverter is shown in Figure 3.
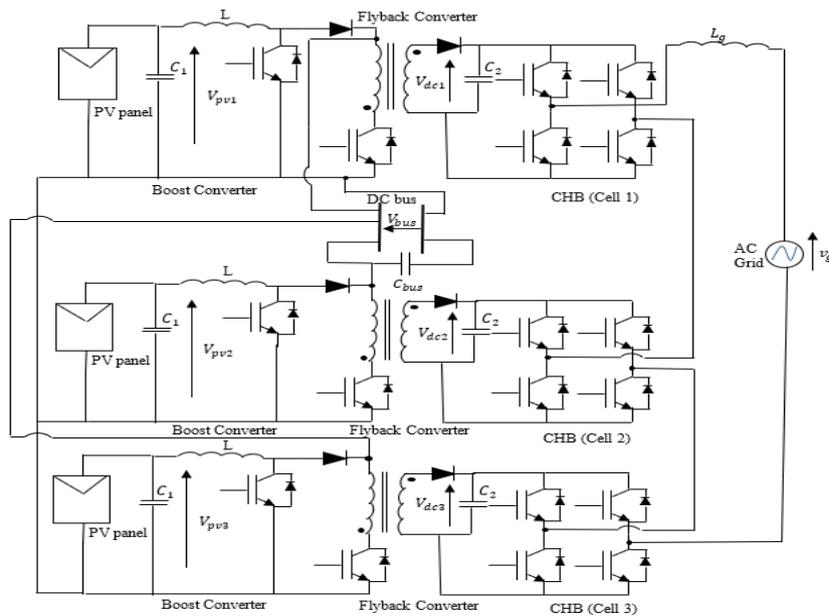
Figure 1. PV mult-panel single DC bus single phase seven level CHB inverter
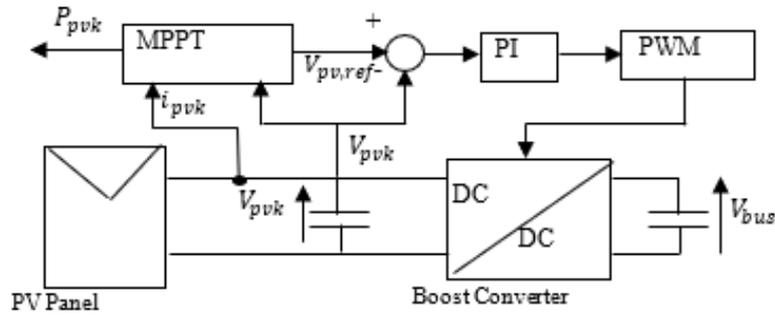
Figure 2. Boost converter with MPPT control scheme
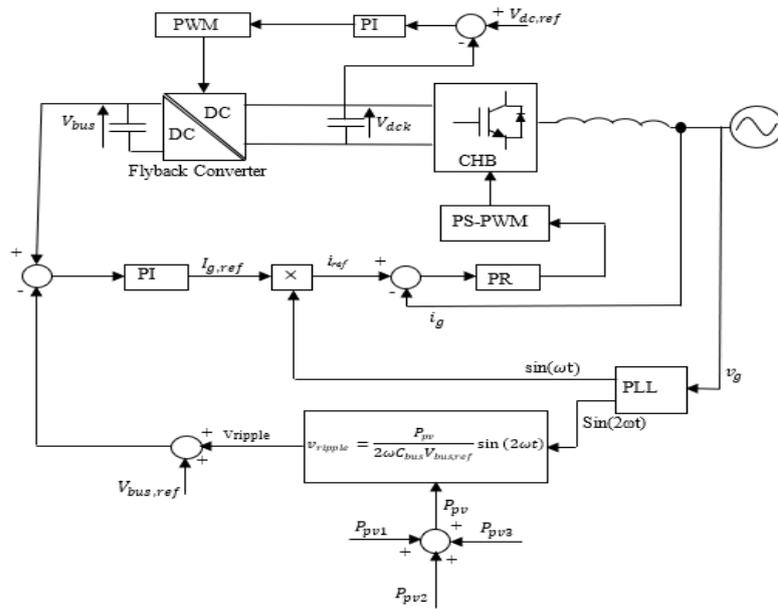
Figure 3. Flyback converter and cascaded H-bridge inverter control scheme

4. ANALYSIS AND MODELING OF THE DC BUS VOLTAGE CONTROL LOOP

The analysis of control loop of single DC bus voltage based on assumption that the current loop is fast and its transient is neglected compared to the single DC bus voltage control. Figure 4 shows the block diagram of the single DC bus voltage control. The simplified model can be obtained using the following assumptions:

− The effect of single DC bus voltage ripple on voltage controller is ignored by addition of the estimated ripple voltage (v_{ripple}) to reference voltage (the ripple voltage is eliminated from input of controller).

− The output of voltage controller ($I_{g,ref}$) is multiplied by v_{pLL} which is $\sin\omega t$ to obtain $i_{ref}=I_{g,ref}\sin\omega t$. The current loop is assumed ideal and fast, therefore $i_g=i_{ref}$, where i_g is the grid current.

− The converter output power is $v_g i_g = \frac{\hat{V_g}\hat{I_g}}{2}(1 - cos2(\omega t))$. By assuming the double frequency component of power has no effect on dynamic of single bus voltage control in terms of average signals [22], then the output power is approximated to active term which is $\frac{\hat{V_g}I_{g,ref}}{2}$.

− Any imbalance between photovoltaic power P_{pv} and output power is supplied from single DC bus capacitor C_{bus} and given by the following equation:

$$C_{bus}\frac{dV_{bus}}{dt} V_{bus,ref} = P_{pv} - \frac{\hat{V_g}I_{g,ref}}{2} \qquad (5)$$

Applying Laplace transform, V_{bus} can be obtained as

$$V_{bus} = \frac{1}{s C_{bus} V_{bus,ref}} (P_{pv} - \frac{\hat{V_g} I_{g,ref}}{2}) \tag{6}$$

From the simplified model of bus voltage control system shown in Figure 5, the characteristic equation of the control system is

$$1 + \frac{1}{s}(k_p + \frac{k_i}{s})(\frac{\hat{V_g}}{2 C_{bus} V_{bus,ref}}) = 0 \tag{7}$$

In (7) can be written as

$$s^2 + \frac{k_p \hat{V_g} s}{2 C_{bus} V_{bus,ref}} + \frac{k_i \hat{V_g}}{2 C_{bus} V_{bus,ref}} \tag{8}$$

After comparison with standard second-order characteristic equation which is

$$s^2 + 2\varsigma\omega_n s + \omega_n^2 = 0 \tag{9}$$

The following relations are obtained,

$$2\varsigma\omega_n = \frac{k_p \hat{V_g}}{2 C_{bus} V_{bus,ref}} \tag{10}$$

$$\omega_n^2 = \frac{k_i \hat{V_g}}{2 C_{bus} V_{bus,ref}} \tag{11}$$

Where ς and ω_n are the damping factor and undamped natural frequency respectively. The stability condition requires that $k_p > 0$ and $k_i > 0$. The proportional gain (k_p) and integral gain (k_i) of PI controller can be tuned to minimize bus voltage fluctuation and grid current harmonics.

The total photovoltaic power (P_{pv}) to the common bus voltage is given by

$$G(s) = \frac{V_{bus}(s)}{P_{pv}(s)} = \frac{s}{C_{bus} V_{bus,ref} s^2 + 2\varsigma\omega_n s + \omega_n^2} \tag{12}$$

The time response of bus voltage to a step change of photovoltaic power (P_{pv}) is

$$V_{bus}(t) = \frac{P_{pv}}{C_{bus} V_{bus,ref} \omega_n \sqrt{1-\varsigma^2}} e^{-\varsigma\omega_n t} \sin\{(\omega_n \sqrt{1-\varsigma^2}) t\} \tag{13}$$

The bus voltage peak fluctuation (overshoot) can be obtained by solving $\dot{V}_{bus}(t) = 0$. The normalized peak fluctuation is [17]

$$V_p = \frac{V_{bus,max} - V_{bus,ref}}{V_{bus,ref}} = \frac{P_{pv}}{C_{bus}(V_{bus,ref})^2 \omega_n} e^{\frac{-\varsigma \cos^{-1}\varsigma}{\sqrt{1-\varsigma^2}}} \cong \frac{P_{pv}}{C_{bus}(V_{bus,ref})^2 \omega_n} e^{-\varsigma} \tag{14}$$

According to (14), the bus control bandwidth (characterized by ω_n) must be higher value in order to achieve lower voltage fluctuations. The voltage fluctuations become larger with smaller capacitor (C_{bus}) unless the bandwidth increased accordingly.

The double frequency ripple that is existed in the single DC bus voltage is a result of oscillating component of the output ac power which has a magnitude of $\frac{\hat{V_g} \hat{I_g}}{2}$. The ac pulsating power passes through the $\frac{1}{s}$ block, then through $\frac{1}{C_{bus} V_{bus,ref}}$ unit to create the bus voltage ripple which its magnitude is given by

$$v_{bus,ripple} = \frac{P_{pv}}{2\omega C_{bus} V_{bus,ref}} \tag{15}$$
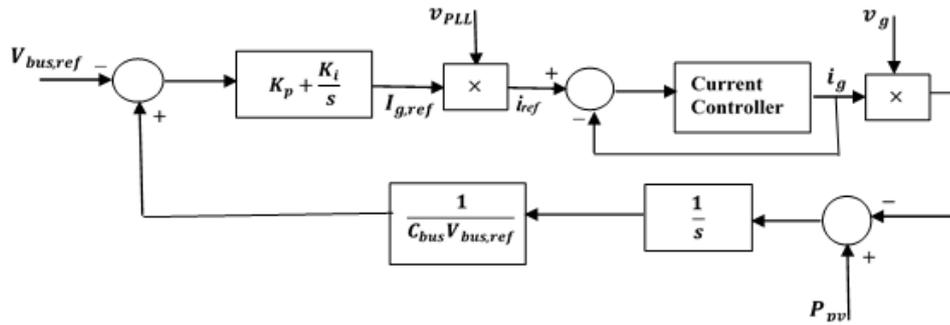
Figure 4 DC bus voltage control model
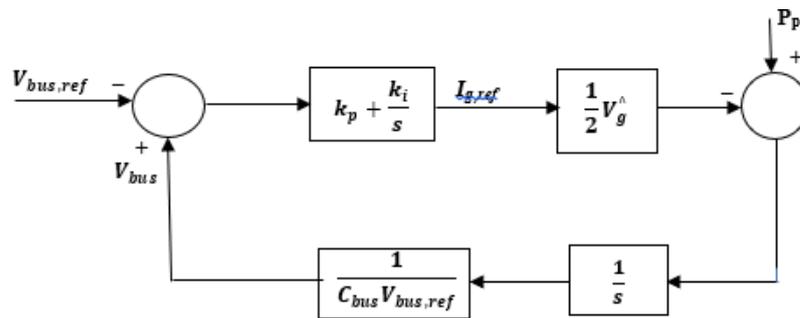
Figure 5. DC bus voltage simplified control model

5.   RESULTS

The proposed single-phase single-bus multi-panel photovoltaic conversion system is simulated using PSIM program. The system is consisted of three photovoltaic panels, each one gives maximum power of 120 W with current and voltage of 7.5 A and 16 V respectively at maximum power point for radiation intensity of 1000 W/m² and temperature of 25 °C. The boost converter for each PV panel is suggested to obtain maximum power point using P&O method. The output of each boost converter is connected to single DC bus with regulated voltage of 100V. Three flyback converters with isolation transformers of 1:1turns ratio are used to obtain DC link voltage of 120 V for each cascaded H-bridge cell of seven level inverter. The output of inverter is connected to grid of 220 V, 50 Hz through smoothing reactor (L_g) of 3mH.

The complete system dynamic performance is shown in Figure 6 for change of total photovoltaic power from zero to 184 W for time period between zero and 0.4 s, then a step change of total photovoltaic power from 184 W to 352 W for time period between 0.4 s and 0.8 s as shown in Figure 6 (a) when sun radiation intensity is changed from 500 W/m² to 1000 W/m² at t=0.4 s, where t is the time. For this simulation, the values of parameters of DC bus voltage controller and bus capacitance are k_p=.02, k_i=2.0, and C_{bus}=500 µF respectively. Figure 6 (b) shows the ripple voltage that is calculated using '(4). The frequency of ripple voltage equals to 100 Hz and its amplitude equals to 5 V and increased to 10 V at t=0.4 s when the photovoltaic power increased from 184 W to 352 W.

Figure 6 (c) shows the DC bus voltage reference plus ripple voltage and DC bus voltage which are approximately equal at steady state therefore the double frequency ripple voltage is cancelled from error signal that is applied to the controller of DC bus voltage resulting no second order harmonic found in the output of controller $I_{g,ref}$. Elimination of second order harmonic leading to the reference current of inner current loop to be sinusoidal with fundamental frequency. A rise in DC bus voltage which is approximately of 25 V is noticed at t=0.4 s when the photovoltaic power is increased from 184 W to 352 W. This increment in DC bus voltage is approximately matched with previous analysis (14). The DC bus voltage is returned to its original average value of 100 V after a time of 0.04 s from the instant of input power jump. Initially the bus voltage is started from zero and increased to value higher than reference with an overshoot slightly higher than overshoot that happens when the power is increased to 352 W at 0.4 s, this is due to charging of storage capacitors of conversion system resulting delay in voltage control loop response.

Figure 6 (d) shows the DC link voltages (V_{dc1},V_{dc2} ,V_{dc3}) for CHB cells. These voltages have average value of 120 V with small ripple and fast response. The single DC bus voltage swell is not

propagated to any of these voltages. This is due to variation of duty ratio of flyback converters to regulate the DC link voltages to a constant reference value of 120 V by action of proportional-integral controller for each flyback converter.

The inverter output voltage is shown in Figure 6 (e). The seven voltage levels can be observed verifying the used PS-PWM technique. Figure 6 (f) shows the output of DC bus voltage controller that represents the amplitude of reference current with small ripple due to the proposed method of estimated ripple voltage addition to DC bus voltage reference. Figure 6 (g) shows the grid voltage and grid current with very low total harmonic distortion (THD of grid current=3.9% at P_{PV}=352 W). The grid current is in phase with grid voltage (power factor=0.998).

(a)

(b)

(c)

(d)

(e)

(f)

(g)
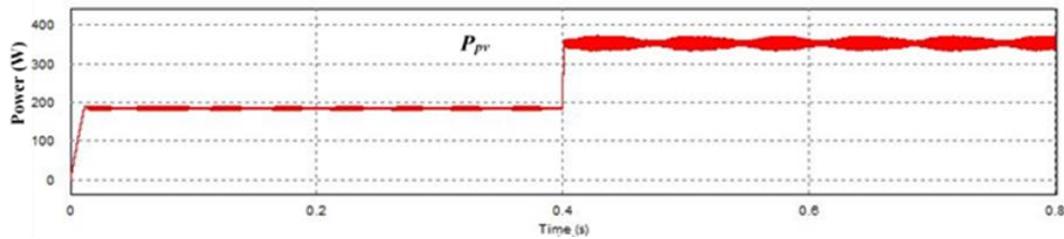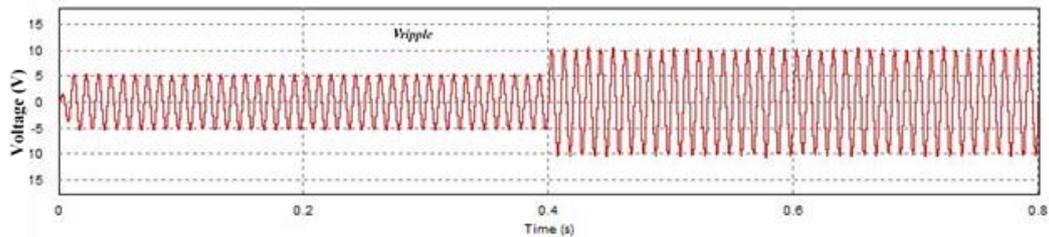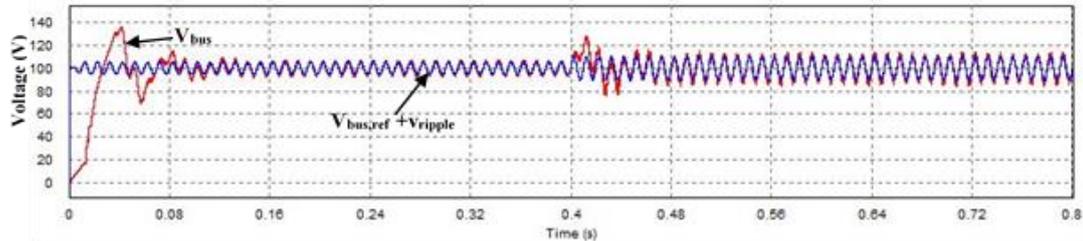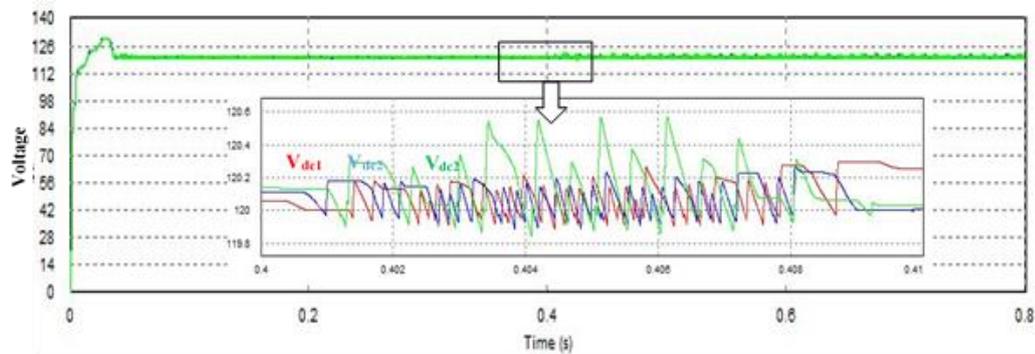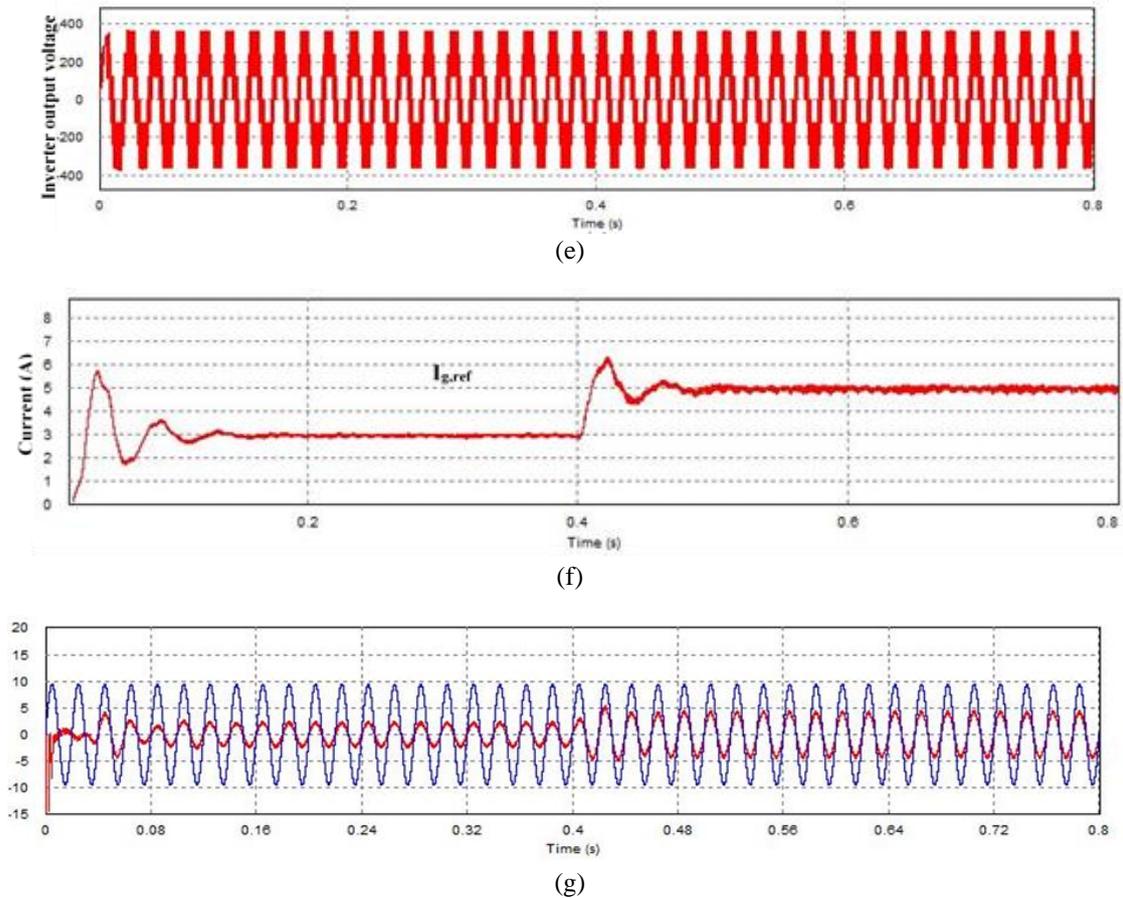
Figure 6. Step change in photovoltaic power results with Cbus=500 µF, Kp=0.02 ,ki=2.0,
(a) Photovoltaic power at input, (b) Estimated ripple voltage, (c) DC bus voltage and reference plus ripple
voltage, (d) DC link voltage for each cell of CHB, (e) Inverter output voltage, (f) Scaled amplitude of
reference current (multiplied by 2), (g) Scaled grid voltage(divided by 33) and scaled grid current
(multiplied by 2).

Figure 7 shows the dynamic performance of complete system with same conditions and parameters applied in Figure 6 but without addition of ripple voltage to the DC bus voltage reference. The DC bus voltage and reference are shown in Figure 7 (a). An overshoot of 26 V is noticed in the DC bus voltage at t=0.4 s when the input PV power is increased from 184 W to 352 W, and peak-to-peak second order harmonic ripple equals to 20 V at Ppv=352 W. The average value of DC bus voltage at steady state is matched the reference of 100 V. No significant difference with Figure 6 (c) is noticed. Figure 7 (b) shows the reference current amplitude (Ig, ref) contaminated with second order harmonic that is not cancelled from error signal (the input of DC bus voltage controller).

Figure 7 (c) shows the grid current with higher THD (6.7% at Ppv=352 W), in phase with grid voltage. Comparing with Figure 6 (g), a higher THD for grid current is due to presence of second order harmonic in DC bus voltage control loop.

(a)

(b)

(c)
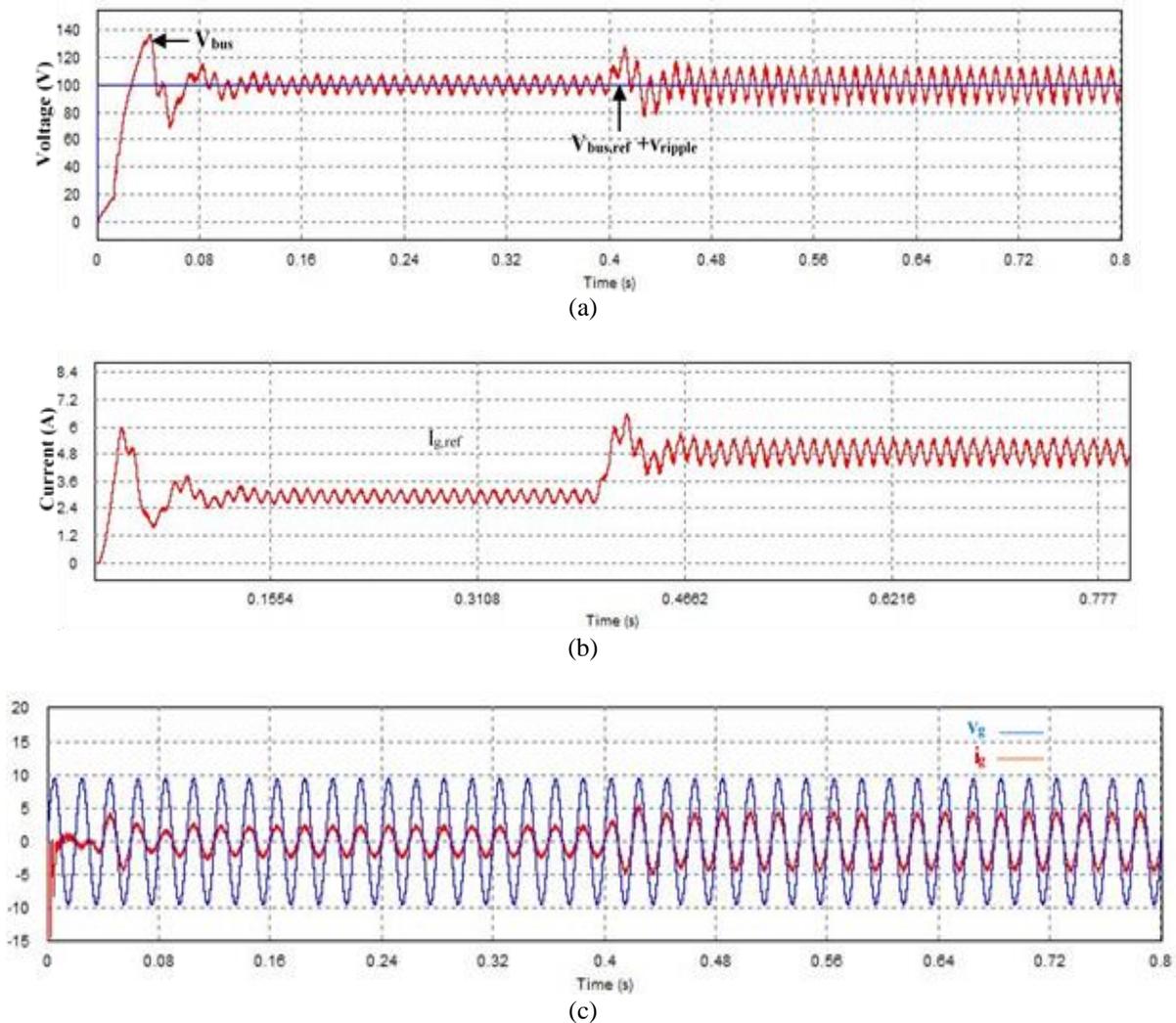
Figure 7. Step change in photovoltaic power results with Cbus=500 µF, Kp=0.02, ki=2.0 and no ripple voltage estimation, (a) DC bus voltage and reference voltage, (b) Scaled amplitude of reference current (multiplied by 2), (c) Scaled grid voltage (divided by 33) and scaled grid current (multiplied by 2)

The main goal of this paper is to inject current into the grid with low THD using small DC bus capacitance. From comparison between Table 1 and 2, a lower DC bus capacitance can be used to give THD for grid current less than 5% with the addition of estimated ripple voltage to reference voltage and Ppv=352 W, kp=.02 and ki=2.0. For example, with Cbus=250 µF, THD of grid current equals to 4.67% compared with 12.09% for the same DC bus capacitance and Ppv when no addition of ripple voltage to the reference voltage.

Table 3 shows the values of undamped natural frequency (ωn) in rad/s, damping factor (η) and overshoot percentage (Vp) obtained using equations 11, 10, and 14 respectively. The natural frequency and damping factor are increased with reduced DC bus capacitance resulting faster dynamic response for step rise in photovoltaic power. The values of overshoot percentage in the table for step rise of photovoltaic power from 184W to 352W are increased when the DC bus capacitance value is reduced but this overshoot does not appear in the DC link voltage for each cell of CHB inverter therefore the design of the converter system with small DC bus capacitance gives acceptable results.

Figure 8 shows the DC bus voltage, grid current and DC link voltages responses with Cbus=250 µF and step rise of Ppv from 184 W to 352 W at t=0.4 s. The average bus voltage peak fluctuation around average reference equals to 32 V which is approximately agree with analytical value in table 3. Grid current THD value was 4.67% as mentioned in table 1. The average value of DC link voltage for each CHB cell was 120 V with very small ripple and no transmission of DC bus voltage jump or ripple to these voltages.

Table 1. THD for grid current with ripple voltage estimation using different values of DC bus capacitance	
C_{bus} (µF)	THD% of grid current (i_g)
100	13.77
150	8.56
200	5.59
250	4.67
300	4.32
350	3.98
500	3.9
1000	3.72

Table 2. THD for grid current without ripple voltage estimation using different values of DC bus capacitance	
C_{bus} (µF)	THD% of grid current (i_g)
100	28.99
150	20.86
200	15.16
250	12.09
300	10.25
350	8.93
500	6.7
1000	4.58

Table 3. Analytical results for ω_n, η and V_p for different values of DC bus capacitance

C_{bus}(µF)	ω_n(rad/s)	η	V_p%
100	176.35	0.8817	37.91
150	143.99	0.7199	34.99
200	124.69	0.6234	32.83
250	111.53	0.5576	31.11
300	101.81	0.509	29.7
350	94.26	0.4713	28.5
500	78.86	0.3943	25.76
1000	55.767	0.2788	20.66
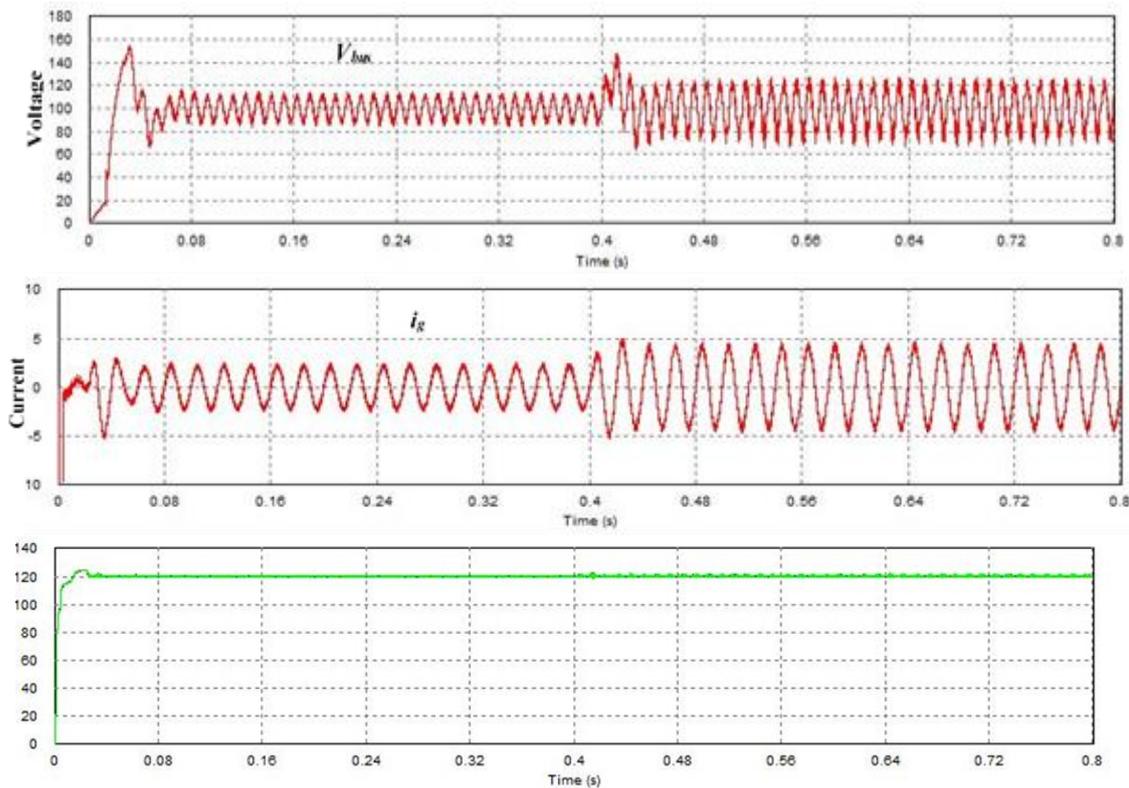
Figure 8. DC bus voltage, scaled grid current (multiplied by 2) and DC link voltages with C_{bus}=250 µF and P_{pv} step rise from 184 W to 352 W

Figure 9 shows the DC bus voltage and grid current responses with bus capacitance of 300 µF and step rise of P_{pv} from 184 W to 352 W. The bus voltage fluctuation approximately matched the analytical value which was 31 V. Grid current THD value was 4.32% as mentioned in Table 1.

Figure 10 shows the DC bus voltage and grid current responses with bus capacitance of 350 µF and step rise of P_{pv} from 184 W to 352 W. The bus voltage fluctuation approximately matched the analytical value which was 28 V. Grid current THD value was 3.98% as mentioned in Table 1.

The practical capacitors have maximum tolerance of ±10%. If the ideal value of capacitance for example 250 µF is used to calculate the ripple voltage that is added to reference DC bus voltage and the actual capacitor of 250+10% is connected across the DC bus to test the performance of proposed system as shown in Figure 11. The DC bus voltage and reference plus ripple voltage are matched and the grid current is sinusoidal with THD of 4.9% and in phase with grid voltage
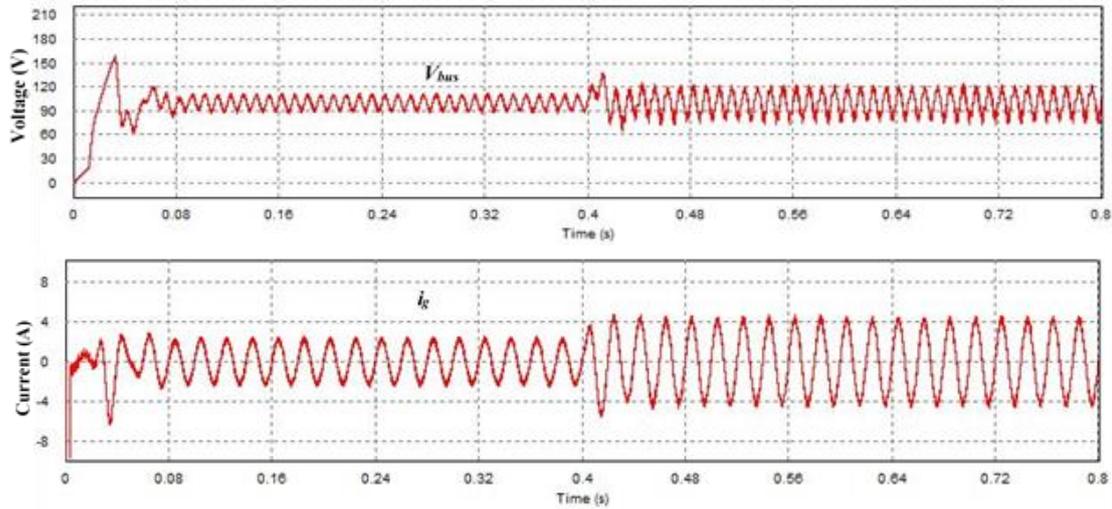
Figure 9. DC bus voltage and scaled grid current (multiplied by 2) with C_{bus}=300 µF and step rise of P_{pv} from 184 W to 352 W
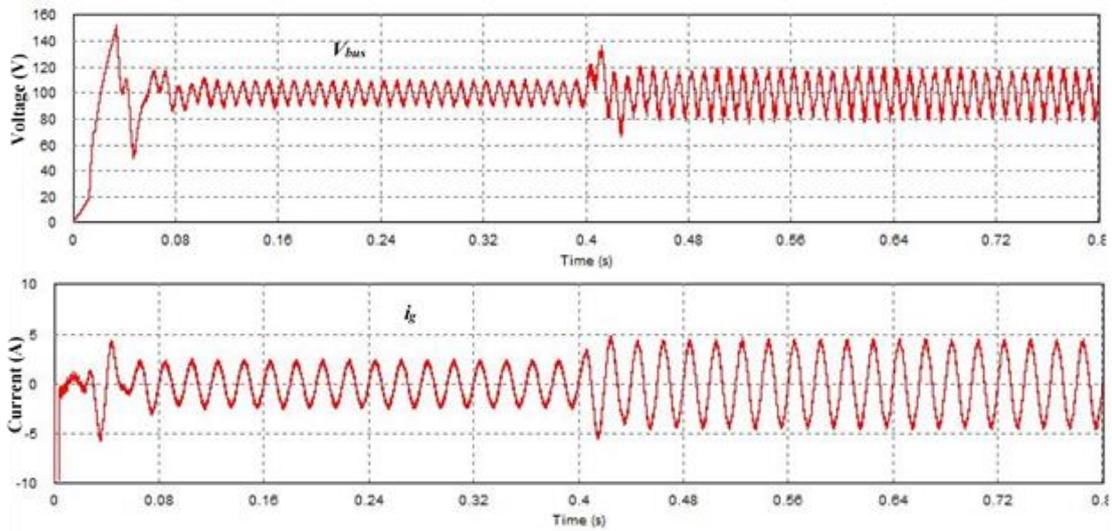
Figure 10. DC bus voltage and scaled grid current (multiplied by 2) with C_{bus}=350 µF and step rise of P_{pv} from 184 W to 325 W
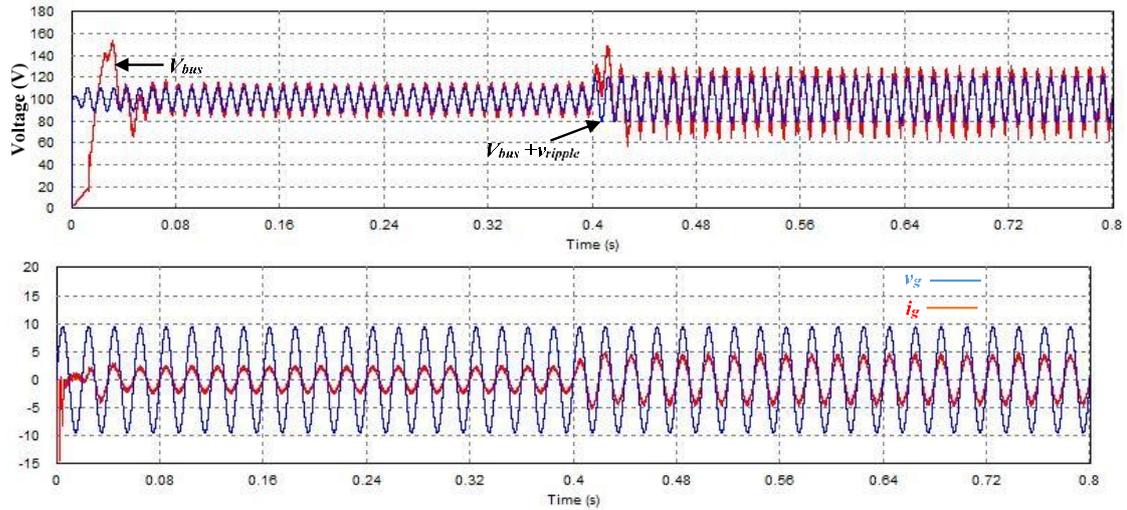
Figure 11. DC bus voltage and reference plus ripple voltage, scaled grid voltage (divided by 33) and scaled grid current (multiplied by 2) with C_{bus}=250 µF+10% and step rise of P_{pv} from 184 W to 352 W at t=0.4 s

Figure 12 shows the performance of proposed system for the actual capacitor of 250 µF-10% (225 µF) that is connected across the DC bus and using the ideal capacitor value (250 µF) to calculate the ripple voltage. The DC bus voltage and reference plus ripple voltage are matched and the grid current is sinusoidal and in phase with grid voltage. Grid current THD value was 5.2%. A variation of ±10% of practical capacitor around the ideal value of 250 µF gives small increment on THD of grid current due to small difference between the estimated ripple voltage that is added to the reference and the actual ripple voltage contained in DC bus voltage.
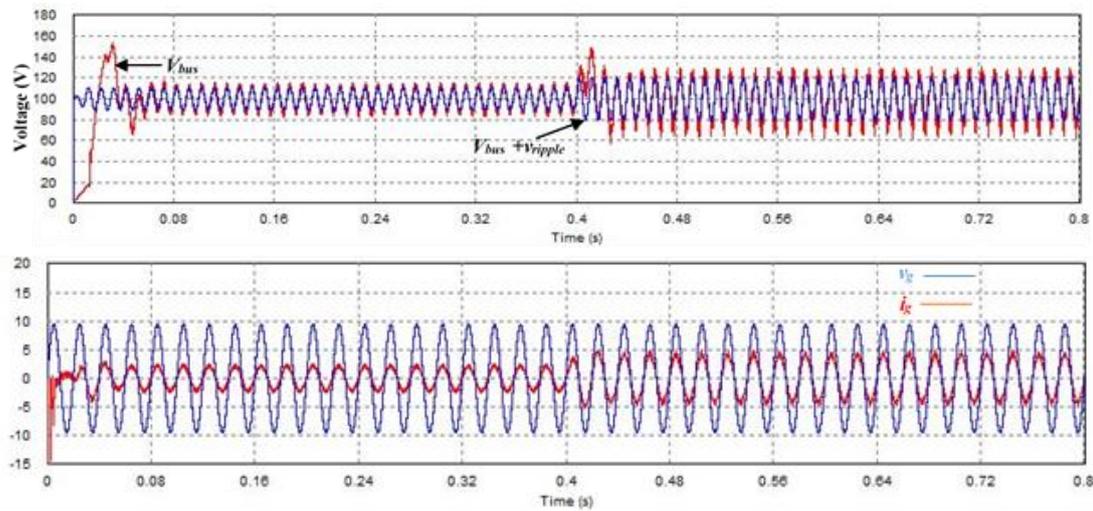
Figure 12. DC bus voltage and reference plus ripple voltage, Scaled grid voltage (divided by 33), and scaled grid current (multiplied by 2) with C_{bus}=250 µF-10% and step rise of P_{pv} from 184 W to 352 W at t=0.4 s

Figure 13 shows the dynamic behavior of the system for reference voltage step from 100 V to 140 V with C_{bus}=500 µF, k_p=0.02, k_i=2.0 and P_{pv}=352 W. Initially the DC bus voltage has an overshoot of approximately 40 V,then matched the reference at time of 0.06 s. The DC bus voltage follows the reference step at t=0.4 s with small overshoot as shown in Figure 13 (a). The rise of DC bus voltage to 140 V (average value) is not appeared in DC link voltage for each CHB which is regulated to average value of 120 V with small ripple as shown in Figure 13 (b), this is due fast dynamic response of flyback converter. Figure 13 (c) shows the amplitude of grid current and Figure 13 (d) shows the grid voltage and sinusoidal grid current. The

grid current is decreased at the instant of reference rise since the photovoltaic energy is used to charge the bus capacitance to new reference value then the current rises during overshoot period. The grid current is returned to its original value after the coincidence of bus voltage and reference plus ripple voltage.

Finally, the proposed photovoltaic power conversion system is tested to verify the equally distributed output power among CHB cells irrespective to unequal input photovoltaic applied from PV panels. Let the photovoltaic power supplied from first PV panel is P_{pv1}=61.5 W, the photovoltaic power supplied from second PV panel is P_{pv2}=9.5 W and the photovoltaic power supplied from third PV panel is P_{pv3}=117 W. The total input photovoltaic power is P_{pv}=188 W applied to single DC bus. The output power (P_o) applied to grid is P_o=172 W distributed with the value of 57.3W for each CHB cell of seven level inverters.

(a)

(b)

(c)

(d)
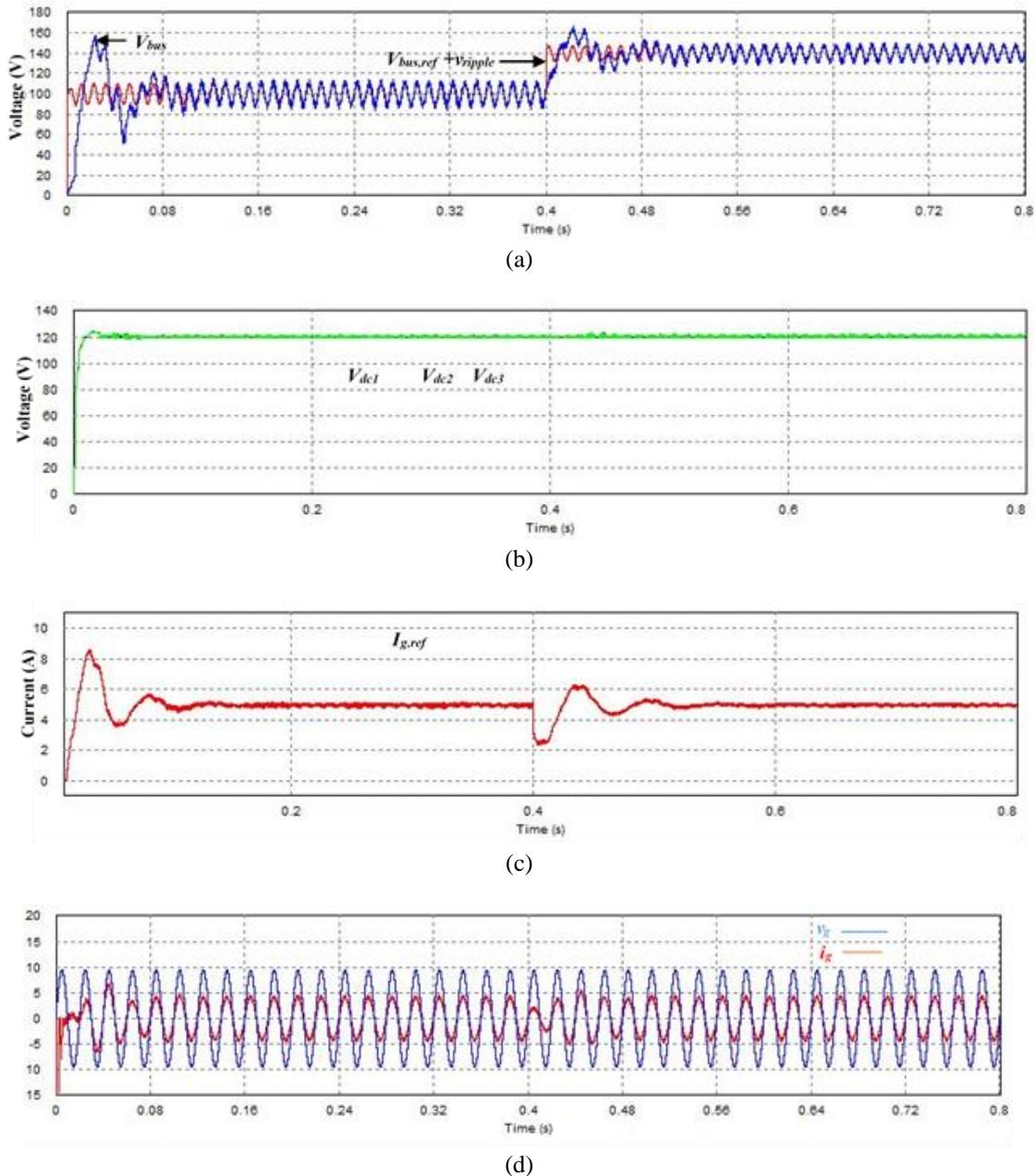
Figure 13. Step change of DC bus voltage reference results with C_{bus}=500 µF and P_{pv}=352 W, (a) reference plus ripple voltage and DC bus voltage, (b)DC link voltage for each CHB cell, (c) Scaled amplitude of grid current reference (multiplied by 2), (d) Scalled grid current (multiplied by 2) and scaled grid voltage (divided by 33).

6.   CONCLUSIONS

In this paper, single DC bus single phase seven level cascaded H-bridge multilevel inverter with three PV panels is proposed. Three non-isolated boost converters are used, one for each PV panel to extract maximum power. The output of each boost converter is connected to common DC bus. Three flyback DC-DC converters are used to obtain DC link voltages for CHB cells. The DC link voltages are regulated to constant value and stable against variation of single DC bus voltage due to PV power jump. The DC bus voltage control loop is simplified, analyzed and designed. No band-stop filter is used to attenuate second order harmonic in the feedback DC voltage or used it in control loop. This simplifies the analysis, design and implementation.

The ripple voltage is estimated and added to reference voltage to eliminate the second order harmonic in DC voltage control loop, therefore using small DC bus capacitance is sufficient to give grid current with low THD. The DC voltage control can be designed with larger bandwidth making the response is faster to reject any disturbance. The simulation results show that the bus capacitance (C_{bus}) can be reduced to a value of 250 µF and the THD of grid current is still less than 5% (4.67%) when the ripple voltage is added to the reference and the THD is increased to 12.09% with no addition of ripple voltage to the reference.

Grid voltage, grid frequency, nominal power, DC bus voltage, DC bus capacitance, and THD of grid current values, and the need for stop band filter are shown in Table 4 to compare the results and confirm the proposed method. Highly reduction in DC bus capacitance is noticed when the estimated voltage ripple is added to the DC bus reference voltage compared to the value used in [15]. THD of grid current was 3.87 % with DC bus capacitance of 500 µF and 3.06 % when DC bus capacitance was 11000 µF in [15]. No need to band stop filter in the proposed method. Without ripple voltage estimation, THD of grid current was 10.21%.

The output power is equally distributed between CHB cells due to using single DC bus. This work can be extended to single or three phase multistring PV single DC bus multilevel inverter (each multistring is consisted of PV panels connected in series) and implemented using long life film capacitors instate of short life electrolytic capacitors.

Table 4. Comparison of results

	[15]	With ripple voltage estimation	Without ripple voltage estimation
Grid voltage	40 V	40 V	40 V
Grid frequency	50 Hz	50 Hz	50 Hz
Nominal power	225 VA	225 VA	225 VA
DC bus voltage	48 V	48 V	48 V
DC bus capacitance	11000 µF	500 µF	500 µF
Grid current THD	3.06 %	3.87 %	10.21 %
Band stop filter	Yes	No	No

REFERENCES

[1]   S. Kouro, *et al.*, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," *IEEE Industrial Electronics Magazine*, vol.9, no.1, pp. 47-61, 2015.

[2]   E. Villanneva, *et al.*, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol.56, no.11, pp. 4399-4406, 2009.

[3]   M. Coppola, et al., "An fpga-based advanced control strategy of a grid-tied pv CHB inverter," *IEEE Transactions on Power Electronics*, vol. 31, no.1, pp. 806-816, 2016.

[4]   B. Xiao, et al., "Modular cascaded H-bridge multilevel inverter with distributed MPPT for grid-connected applications," *IEEE Transactions on Industry Applications*, vol. 51, no.2, pp. 1722-1731, Mar. 2015.

[5]   B. Xiao, et al., "Control of three-phase cascaded voltage source inverter for grid-connected photovoltaic systems," *in IEEE Proc. Applied Power Electronics Conference and Exposition (APEC)*, pp. 291-296, 2013.

[6]   Y. Zhou, et al., "A high-performance photovoltaic module-integrated converter (MIC) based on cascaded quasi-z-source inverters (qzsi) using eGaN FFTs," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2727-2738, 2013.

[7]   C. D. Townsend, et al., "Cascaded H-bridge multilevel PV topology for alleviation of per-phase power imbalances and reduction of second harmonic voltage ripple*," IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5574-5586, 2016.

[8]   M. Miranbeigi, et al., "Hybrid modulation technique for grid-connected cascaded photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 99, no. 12, pp. 7843-7853, 2016.

[9]   L. Maharjan, et al., "Active-power control of individual converter cells for a bridge energy storage system based on a multilevel cascade PWM converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1099-1107, 2012.

[10]   Y. Yu, et al., "Power balance of cascaded H-bridge multilevel converters for large scale photovoltaic integration," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1108-1120, 2016.

[11] Y. Yu, et al., "Power balance optimization of cascaded H-bridge multilevel converters for large –scale photovoltaic integration," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1108-1120, 2016.

[12] S. Essakiappan, et al., "Multilevel medium frequency link inverter for utility scale photovoltaic integration," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3674-3684, 2015.

[13] Rahul Sharma, et al., "Enhanced active power balancing capability of grid connected solar PV fed cascaded H-bridge converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7. no.4, pp. 2281-2291, 2019.

[14] S. Kouro, et al., "Single DC-link cascaded h-bridge multilevel multistring photovoltaic energy conversion system with inherent balanced operation," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 4998–5005, 2012.

[15] C. D. Fuentes, et al., "Experimental validation of a single DC bus cascaded H-bridge multilevel inverter for multistring photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 930-934, 2017.

[16] K. Wang, et al., "Cascaded multilevel converter topology for large-scale photovoltaic system with balanced operation," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 7694-7705, 2019.

[17] S. A. Khajehoddin, et al., "DC-bus design and control for a single-phase grid-connected renewable converter with a small energy storage component," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, 2013.

[18] Baoming Ge, et al., "Direct instantaneous ripple power predictive control for active ripple decoupling of single-phase Inverter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3165-3175, 2018.

[19] P. T. Krein, et al., "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, 2012.

[20] R. Wang, et al., "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1430-1443, 2011.

[21] Gurhan Ertasgin, et al., "Analysis of DC link energy storage for single-phase grid-connected PV inverters," *Electronics*, pp. 1-19, 2019.

[22] Y. Levron, et al., "Bus voltage control with zero distortion and high bandwidth for single phase solar inverters", *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 258-269, 2016.

[23] N. Femia, et al., "Predictive & adaptive MPPT perturb and observe method," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 43, no. 3, pp. 934-950, 2007.

[24] D. N. Zmood, et al., "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 814-822, 2003.

[25] J. Chavarria, et al., "Energy balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMS," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 1, pp. 98-111, 2013.