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ZVS based on dead-time analysis of three port half bridge converters

Phuong Vu, Manh Linh Nguyen, Viet Phuong Pham
School of Electrical Engineering, Hanoi University of Science and Technology, Vietnam

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ABSTRACT

In this research, the zero-voltage switching (ZVS) of the GaN FETs-based high frequency three-port half-bridge converter (TPHBC), which is capable of interfacing a renewable energy source, an energy storage and a load is discussed. To achieve ZVS, which plays a key role in power loss reduction of the high switching frequency converters, not only the parasitic elements but also the dead-time between two switches in one converter arm must be taken into account. This research gives a detail analysis about the influence of the dead-time on the ZVS condition. Based on the analysis, a minimum dead-time which guarantees not only the ZVS but also the safe operation of the converter is obtained. Simulations in various load condition of the TPHBC are carried out to verify the validity and effectiveness of the proposed method.

Corresponding Author:

Manh Linh Nguyen,
School of Electrical Engineering, Hanoi University of Science and Technology,
No.1, Dai Co Viet Road, Hai Ba Trung, Hanoi, Vietnam,
Email: linh.nguyenmanh@hust.edu.vn

1. INTRODUCTION

Renewable energy has attracted great attention recently as an alternate solution to the fossil energy which may soon be depleted in near future. Due to the inherent intermittence of renewable energy source such as solar, wind, tide, etc., the energy storages such as battery, super capacitor are indispensable in the renewable energy power systems, especially in the stand-alone systems [1]. These energy storages function as an energy buffer to smoothly supply the loads. Conventionally, several converters are employed to interface the energy source, storage and load simultaneously. The advantages of this solution is simple in hardware and control design since these converters function independently. However, multiple converters may result in large volume and high power losses [5].

To deal with the aforementioned problems of the conventional solution, three port converters (TPCs) which capable of interfacing renewable energy source, storage and load simultaneously has been developed [8], as PV-fed LED lighting systems, etc. Comparative studies on TPCs shows that this configuration offers many advantages over the conventional solution such as higher efficiency, lower cost and compact packing design. These remarkable merits allow the TPCs to be employed in many applications such as hybrid electric vehicles, hybrid energy storage systems, PV systems with battery backup. To handle the power flow in TPCs, various topologies where half bridge or full bridge converters along with magnetic coupling via high frequency transformer have been studied. The most flexible topology where bidirectional power flow can easily be achieved is based on the dual active bridge (DAB) converter [11]. In this configuration, the power flow can be controlled by phase shift and/or duty cycle of the converter bridges. Since the energy can be transferred bidirectionally, this topology is a promising solution to many applications

such as: fuel-cell electric vehicles where regenerative energy can be collected from the motor, or in renewable energy systems with backup battery.

How to minimize the total power loss, which is composed of conduction losses, static losses and switching losses, has always been a major issue in high switching frequency converters. Since the conduction losses and static losses are almost constant due to the hardware design, the switching losses play a key role in the total efficiency of the system. One of the most effective solution to reduce the switching losses in converters until now is zero voltage switching (ZVS) where the switch voltage is brought to zero before the gate voltage is applied [18]. Conventionally, the analysis of ZVS condition is carried out based on the parasitic elements and the load condition while the influence of the dead-time between two switches in one converters arm is neglected [18].

In this research, the ZVS condition of a three-port half-bridge converter with secondary side synchronous rectifier (TPHBC-SR) is analyzed. This configuration suits well small power stand-alone PV applications with a backup battery such as led lighting. The main contribution of this research is the theoretical analysis of the influence of the dead-time on the ZVS condition. This analysis allows the dead-time can be appropriately chosen to guarantee the ZVS while the safe operation of the converters arm is still fulfilled. The proposed method is verified by both numerical simulations and experiments.

2. THREE PORT HALF BRIDGE CONVERTERS

2.1. Operating mode analysis of the TPHBC-SR

The topology of the TPHBC-SR is shown in Figure 1 in which the primary side of the converter can be operated in either half bridge, buck or forward-flyback mode. The flexibility of this topology allows the power flow to be controlled in multiple directions which fulfills the requirement of stand-alone PV systems with battery backup as illustrated in Figure 2. The battery can be can be charged when the primary side operates in buck mode. In half-bridge mode, the load can be feed from either the PV or both the PV and the battery. And in the case of no-irradiation, the converter can be operated in forward-flyback mode to transfer the energy from the backup battery to the load.

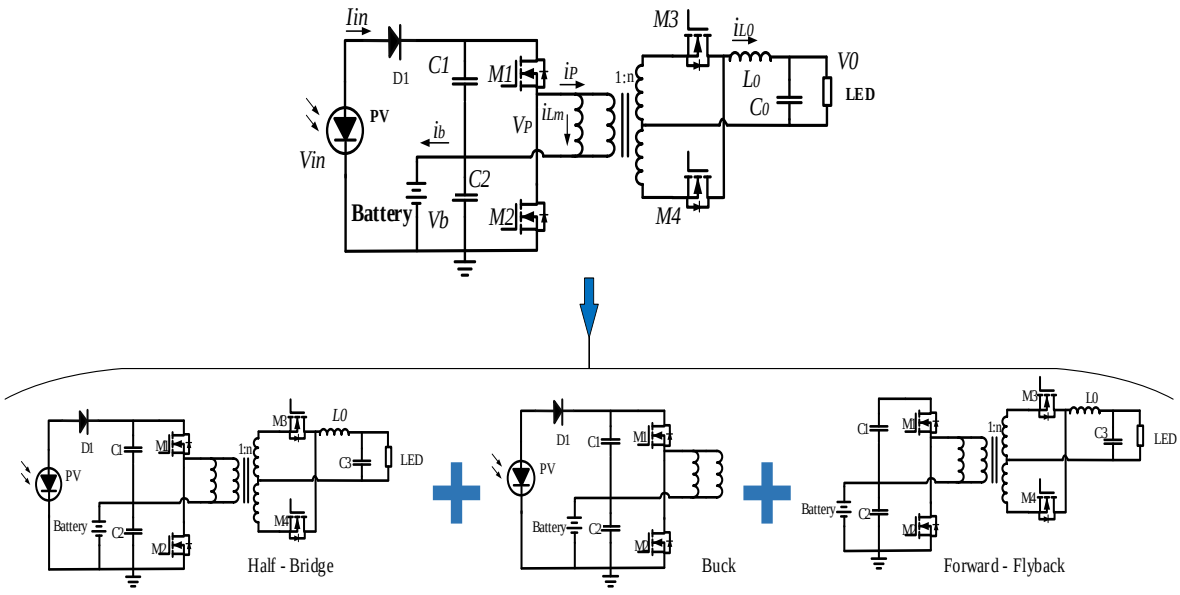


Figure 1. The operation modes of the TPHBC [14]

For simplicity, assume that the capacitor C_0, C_1, C_2 are sufficient large such that the voltage across the capacitor are constant in steady-state operation. By neglecting the power loss of the converter, the following relation holds:

$$p_{in} = p_b + p_o \quad (1)$$

where Pin, Pb and Po are the power of the PV, the backup battery and the load, respectively.

The operating mode of the converter can be explained based on the above relation as follows:

- In DO mode where $p_{in} > p_o$, both the load and the battery receive energy from the PV.
- In DI mode where $0 < p_{in} < p_o$, the load receives energy not only from the PV source but also from the backup battery.
- In SISO mode where $p_{in} = 0$ corresponding to no-irradiation situation, the backup battery becomes the main energy source of the system.

2.2. ZVS analysis.

As mentioned above, the ZVS play a key role in power loss reduction of switching power supply. This section first gives an analysis to show the relation between parasitic elements and ZVS condition of the TPHBC-SR. Then, the influence of the dead-time between two switches of the inverter arm on the ZVS condition, which have never been stated in the literature, is analyzed. Based on this result, the dead-time can be appropriately selected to fulfill not only the safe operation of the inverter arm but also the ZVS condition. In TPHBC-SR, the two switches M3 and M4 on the secondary sides operate with ZVS naturally due to the synchronous rectification configuration with body diodes while M1 cannot achieve ZVS. Hence, the ZVS condition of switch M2 is considered in this research.

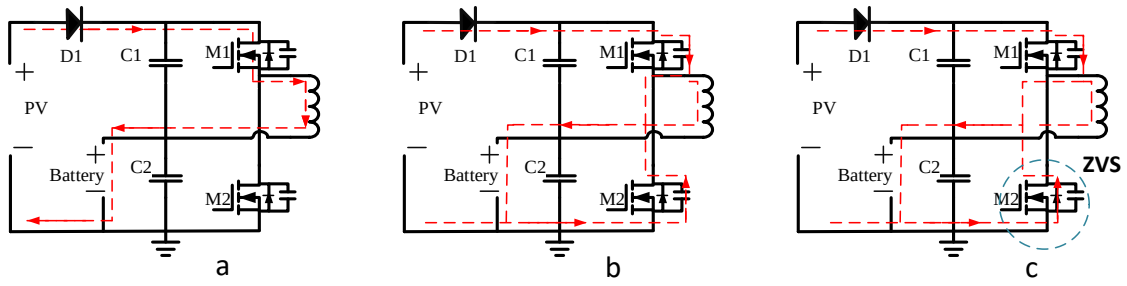


Figure 2. ZVS of switch M_2

Figure 2 show the switching states of M2. As can be realized, M2 can only achieve ZVS if and only if its parasitic capacitor C_{DS} is fully discharged whilst the corresponding capacitor of M1 is fully charged. Which means M2 is turned on when its drop voltage V_{DS} is zero while the remaining switch M1 had already been turned off. In that case, the energy stored in the transformer leakage inductance must satisfy the following relation:

$$\begin{cases} \frac{1}{2} L_k (I_{Lm} + nI_{L0})^2 > C_{DS} V_b^2 \\ I_{Lm} + nI_{L0} > 0 \end{cases} \quad (2)$$

In which, L_k is the leakage inductance, C_{DS} is the parasitic capacitor of the switch, I_{L0} is the current of the secondary inductor. As given in [14], I_{Lm} is the current of the main coil of the transformer computed by:

$$I_{Lm} = \frac{I_b - (D_1 - D_2) n I_o}{D_1 + D_2} \quad (3)$$

During transient state, the voltage across M2 oscillates at its natural resonant frequency and can be represented by:

$$V_{DS} = V_m \sin(2\pi f_r t + \Phi) \quad (4)$$

In (4), Φ is the phase angle, the amplitude V_m is dependence of the primary side current I_p and the resonant frequency f_r is computed by:

$$f_r = \frac{1}{2\pi\sqrt{2 C_{DS} L_k}} \quad (5)$$

Suppose that $I_{pMin} = I_{Lm} + nI_{L0}$ is the minimal value of the primary current I_p such that the ZVS condition (2) is satisfactory. The voltage across M2 during off-to-on state with different values of the primary current I_p is shown in Figure 3. As can be seen, in the case of $I_p < I_{pMin}$, the amplitude V_m is small and does not decrease to zero following that the ZVS cannot be achieved. In contrast, the ZVS condition is always fulfilled as $I_p > I_{pMin}$. By taking Figure 3 in consideration, it can be seen that the amplitude of the oscillation voltage V_m is equal to the battery voltage V_b in the case $I_p = I_{pMin}$, which means

$$\frac{1}{2}L_k I_{pB}^2 = C_{DS}V_b^2 \quad (6)$$

To properly chose the dead-time, define t_z as the necessary time for the voltage across M2 to decrease from V_b to zero. Then, the ZVS condition can be reached if and only if the dead-time $t_d > t_z$. It is obviously seen in Figure 3 that:

$$t_z = \frac{1}{4f_r} \quad (7)$$

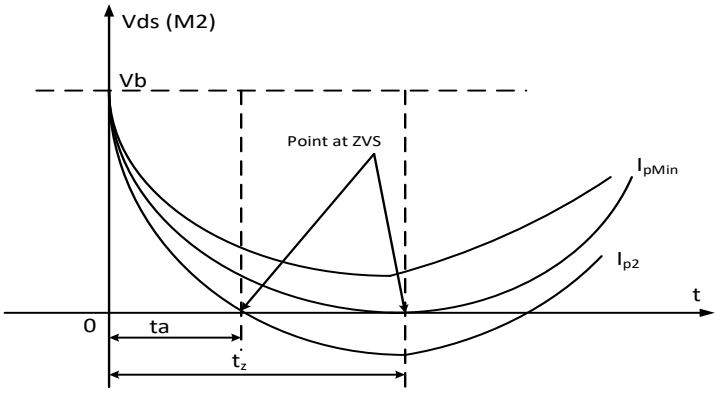


Figure 3. The relation between oscillation V_{ds} of M_2 and primary side current

Based on (5) and (7), it can be derived that

$$t_z = \pi\sqrt{\frac{C_{DS}L_k}{2}} \quad (7)$$

So, the minimal dead-time t_d which guarantees not only the safe operation but also the ZVS is:

$$t_{dMin} = t_z = \pi\sqrt{\frac{C_{DS}L_k}{2}} \quad (8)$$

3. NUMERICAL SIMULATION.

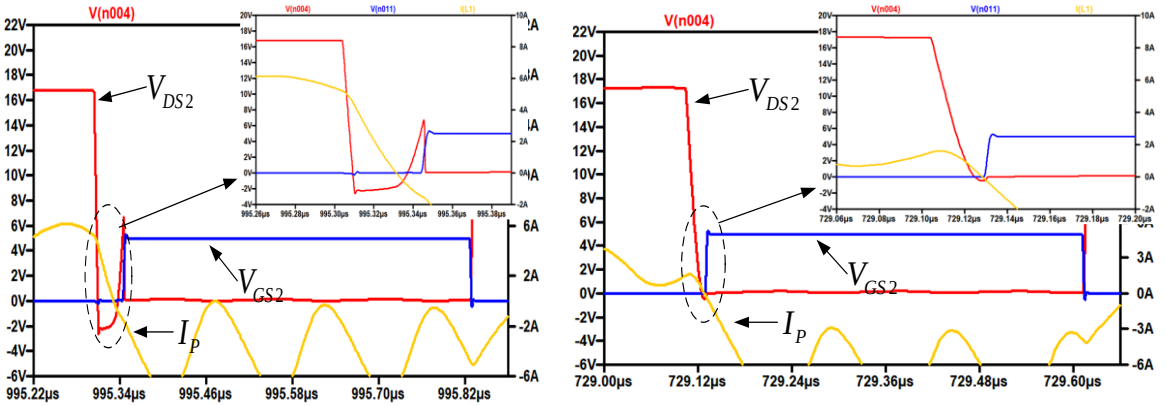
To show the validity of the proposed method, numerical simulations using eGAN FETs are carried out by LTSPICE software, parameters of eGAN FETs are available in [25]. The parameters of the TPHBC-SR used in simulation are provided in Table 1.

As discussed in previous section, (2) must be satisfied to achieve ZVS. However, the proper value of t_d should be carefully considered. For example, if t_d is too large, e.g., $t_d > 2t_z$, the ZVS may not be achieved due to the rising of oscillation voltage V_{DS} as shown in Figure 4a. In contrast, appropriate value of t_d results in ZVS with low dv/dt of V_{DS} as shown in Figure 4b. The nature ZVS of M_3 and M_4 are also shown in Figure 5. In conclusion, the appropriate dead-time should be:

$$\pi\sqrt{\frac{C_{DS}L_k}{2}} < t_d < 2\pi\sqrt{\frac{C_{DS}L_k}{2}} \quad (9)$$

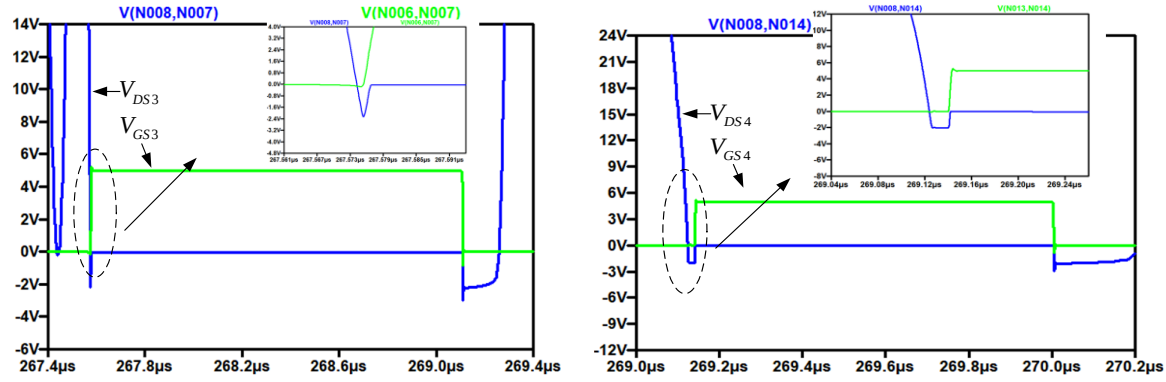
Table 1. Simulation parameter

	Parameter	Values
Input voltage	V_{in}	18.5V
Battery	V_b	12V
Output capacitor	C_o	2.5uF
Output inductor	L_o	30uH
Output power	P_o	30W
Transformer	*Coilcraft PL300-104L*	Plannar
Switching freq	f_s	500Khz



(a) (b)

Figure 4. Switching state of M_2 with different values of dead-time t_d, (a). Switching state with large dead-time (40ns), (b) Switching state with appropriate dead-time (20ns)



(a) (b)

Figure 5. Nature ZVS of M_3 and M_4 switch, (a) ZVS of M_3, (b) ZVS of M_4

4. EXPERIMENT RESULTS.

In this section, a prototype TPHBC-SR is built based on GaN FETs. The schematic of the high frequency driver for the switches is shown in Figure 6. The parameters of the experimental system are same as simulation section.

Since the switching frequency is high, i.e., 500kHz in this case, the printed board circuit (PCB) design plays a very important role in suppressing the ringing loop which may cause serious problem such as electromagnetic interference (EMI) noise or over voltage [21]. In TPHBC-SR design, there are two important ringing loops, i.e., Driver-GaN loop and power ringing loop including input capacitors and switches. The main reason of the ringing loop is the existence of parasitic inductor and capacitor along the circuit routes. Therefore, minimizing the loop in PCB design is crucial in minimizing the parasitic elements. The PCB design with minimized loop is shown in Figure 7, in details.

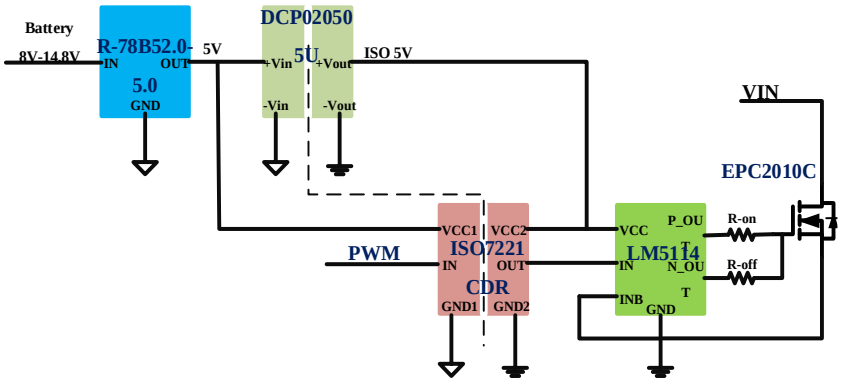
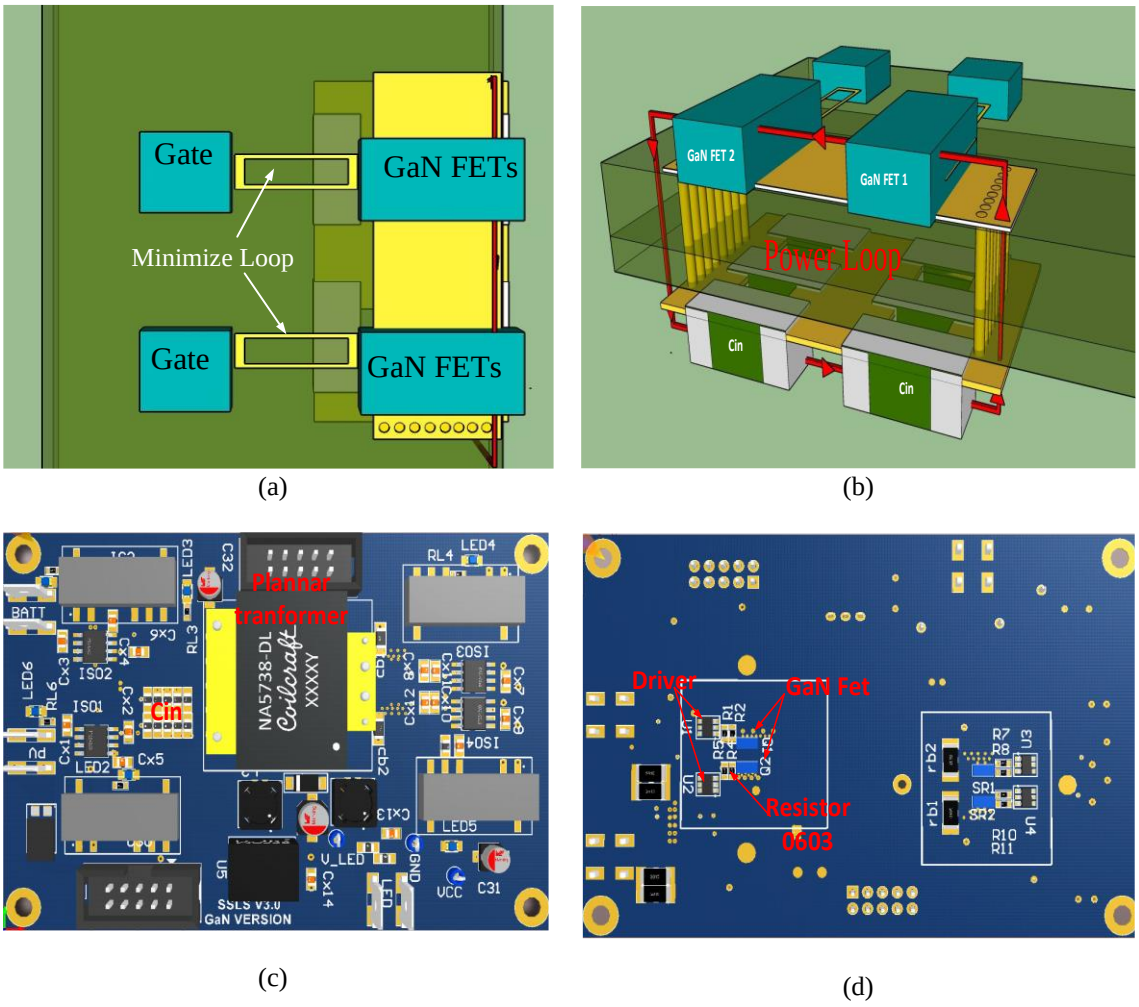


Figure 6. GaN FETs driver schematic



(a) (b)

(c) (d)

Figure 7. PCB design of TPHBC-SR with minimized ringing loop (a) Minimized Driver-GaN loop, (b) Minimized ringing power loop, (c) Top layer, (d) Bottom layer

The experimental results with prototype TPHBC-SR are shown in Figure 8. The switching state of switch M_3 is shown in Figure 8(b) while the switching states of M_2 with various load conditions are shown in Figure 8(c) and Figure 8(d), respectively. It can be observed that both M_2 and M_3 achieve ZVS. In advanced, with appropriate dead-time which is adjusted based on (8), M_2 can achieve ZVS in wide range of load.

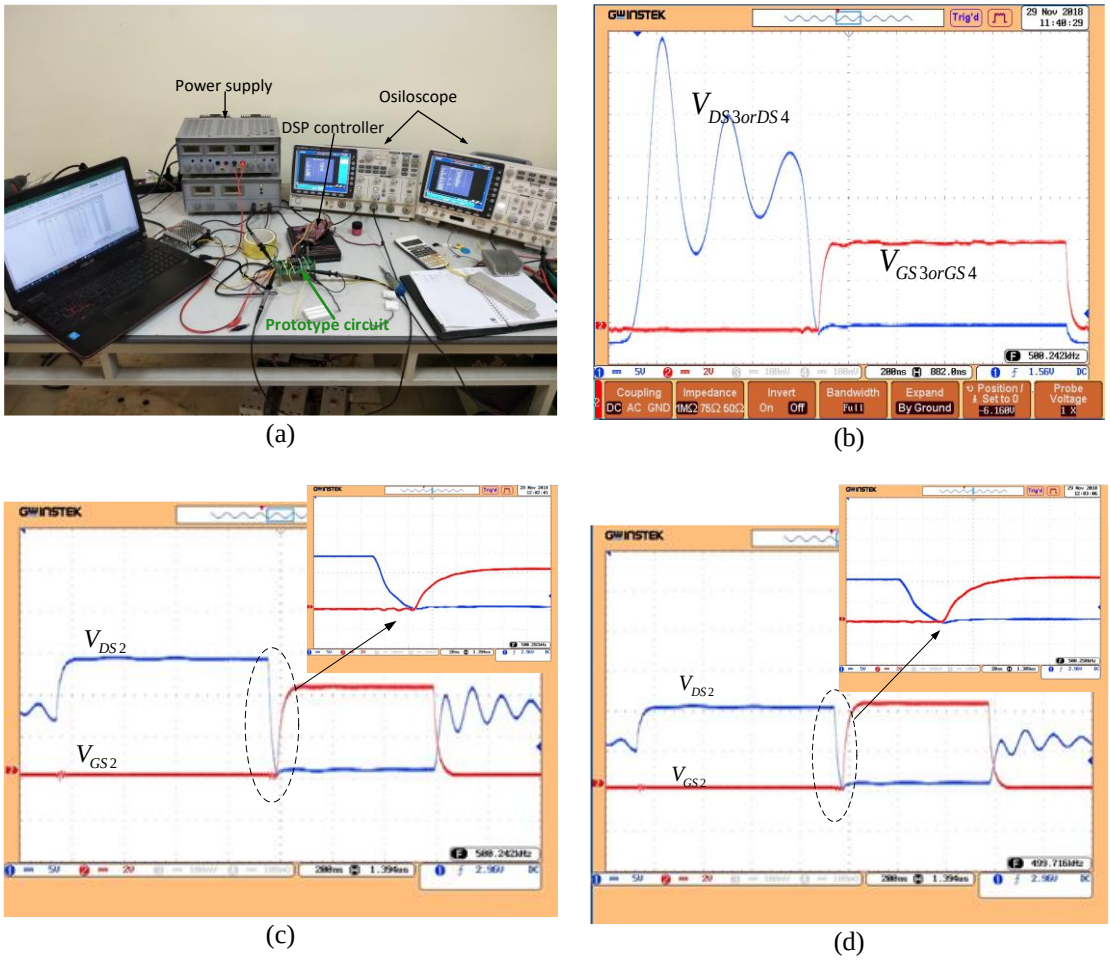


Figure 8. Experimental results with various load condition, (a) Experimental systems, (b) ZVS of M3/M4, (c) ZVS of M_2 with 70% rated load, (d) ZVS of M_2 with 30% rated load

5. CONCLUSION

In this study, ZVS condition for th high frequency GaN FETs-based TPHBC-SR is introduced. Conventionally, the ZVS condition is chosen based on the parasitic elements of the converter. This research shows that the dead-time between two switches of a converter arm also has strong influence on the ZVS condition. Then, the computation of minimum dead-time which guarantees both ZVS and the safe operation of the converter arm is provided. The effectiveness of the method is confirmed by both numerical simulations and experiments with a prototype converter. The matching between the experiment and simulation results proves the validity of the proposed solution.

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BIOGRAPHIES OF AUTHORS

Phuong Vu received his B.S., M.S., and Ph.D. degrees from Hanoi University of Science and Technology, Vietnam, in 2006, 2008, and 2014, respectively, all in Control Engineering and Automation. Since 2006 he has been employed at Hanoi University of Science and Technology, where he is a lecturer and researcher at school of electrical engineering. His research interests include modeling and controlling of power electronics converters for applications such as photovoltaic, wind system, electrical machine drive.

Nguyen Manh Linh received his B.S. and M.S. degrees in electrical engineering from Hanoi University of Science and Technology, Hanoi, Vietnam, in 2008 and 2011, respectively, and the Ph.D. degree from Graduate School of Engineering and Science in Shibaura Institute of Technology, Tokyo, Japan in 2018. He is currently working as a lecturer in the Department of Industrial Automation, School of Electrical Engineering, Hanoi University of Science and Technology, Hanoi, Vietnam. His research interests include model predictive control, sliding mode control, disturbance observer, advanced control theory and its applications to micro/nano positioning systems, digital control design for power electronic converters.

Viet Phuong Pham received his B.S. degree in Electrical Engineering from Hanoi University of Science and Technology, Vietnam, in 2003, his M.S. and PhD. degrees both in Electrical Engineering from Tokyo Institute of Technology, Japan, in 2006 and 2009, respectively. He is currently with Department of Industrial Automation, School of Electrical Engineering, Hanoi University of Science and Technology. His research interests are high power multilevel converters including modular multilevel converters.