Hardware in the loop co-simulation of finite set-model predictive control using FPGA for a three level CHB inverter

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Article Info

ABSTRACT

Along with the development of powerful microprocessors and microcontrollers, the applications of the model predictive controller, which requires high computational cost, to fast dynamical systems such as power converters and electric drives have become a tendency recently. In this paper, two solutions are offered to quickly develop the finite set predictive current control for induction motor fed by 3-level H-Bridge cascaded inverter. First, the field programmable gate array (FPGA) with capability of parallel computation is employed to minimize the computational time. Second, the hardware in the loop (HIL) co-simulation is used to quickly verify the developed control algorithm without burden of time on hardware design since the motor and the power switches are emulated on a real-time platform with high-fidelity mathematical models. The implementation procedure and HIL co-simulation results of the developed control algorithm shows the effectiveness of the proposed solution.

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1. INTRODUCTION

Nowadays, most commercial inverters for AC machines are installed with field-oriented-control (FOC). To further improve the dynamic response of the FOC, new control strategies have been studied for the current control loop such as synchronous vector control, state feedback control, deadbeat control, neural network and fuzzy control [1]. Among them, model predictive control (MPC) has been considered as a powerful alternative control method for power converters and electrical drives [2-8]. The MPC, which was early developed in the 1960s, is an application of the optimal control theory [2], in which the system model is used to predict the future behavior of the system states in a predefined time horizon and then obtain the optimal control action which minimizes a given cost function. Despite of advantages such as intuitive concept, quick dynamic response, ability to handle constrained linear and nonliner multivariable dynamic systems [3], the application of MPC is restricted in the field of process control due to its relatively high computational cost. In recent years, with the development of of high-speed microcontroller and FPGA, the high computational cost problem of the MPC can be solved following that the application of the MPC has been expanded to fast dynamical systems such as power electronic converters and electrical drives. Due to the fact that the power electronic converters only have finite switching states, finite control set model predictive control (FCS-MPC) has been developed to select the switching state for the converters directly

instead of using a modulator which is also complicated, especially in multi level inverters. The FCS-MPC has been successfully applied to the current control in three-phase inverters [9-14], matrix converter [15]. And induction machine [16-18]. An improved FCS-MPC is also proposed to solve the variable switching problem ininduction motor (IM) fed by 2-level voltage source inverter (VSI) [19].

Multilevel converters is widely used for medium-voltage (HV) and high power applications due to its remarkable advantages over the conventional two-level VSI such as: lower voltage stress, lower rate of voltage change (dv/dt), reduced total harmonic distortion (THD) and lower switching frequency which results in improved switching loss [9,20]. Among the multilevel inverter topologies, the CHB is the most successful configuration and already commercialized because of its modularity [21-23]. Typically, a motor control system consists of a conventional controller such as proportional-integral-differential (PID), state feedback, etc., and a pulse width modulation (PWM). For multilevel inverters, the higher the level, the more complex the PWM algorithm is, especially when other inherent problems of the multilevel topologies such as capacitor voltage balance, fault tolerant ability are considered. Hence, this research focuses on the application of FCS-MPC to IM fed by multilevel cascaded H-bridge (CHB) inverters. Instead of using the conventional PWM, the voltage vector which minimizes the predictive current tracking error is selected directly in every consecutive sampling cycle. Without PWM algorithm and by using FPGA [24-26] as the controller, the FCS-MPC algorithm can easily be sovle in very short time following that the response of the inner current is significantly improved in comparison with the conventional PID controller. Besides, multiple objectives can also be achieved by appropriately choosing the cost function. To avoid wasting time on hardware design and the risky experiments with high power systems, HIL platform manufactured by Typhoon is employed to quickly verify the developed control algorithm. By using the Typhoon HIL, the behavior of the motor and the CHB inverter are precisely evaluated in real-time by high-fidelity mathematical models. Realtime simulations with various scenarios are conducted and the results show that the employed FCS-MPC applied to CHB-fed IM drive can achieve good performance not only in terms of tracking accuracy but also dynamic response.

2. SYSTEM DESCRIPTION
2.1. Overview of CHB inverter
The typical configuration of a three-phase multilevel CHB is shown in Figure 1 (a). The fundamental component of the CHB is a single-phase H-brigde inverter which is normally called a power cell. Each phase of the CHB consists of several cells connected in series.
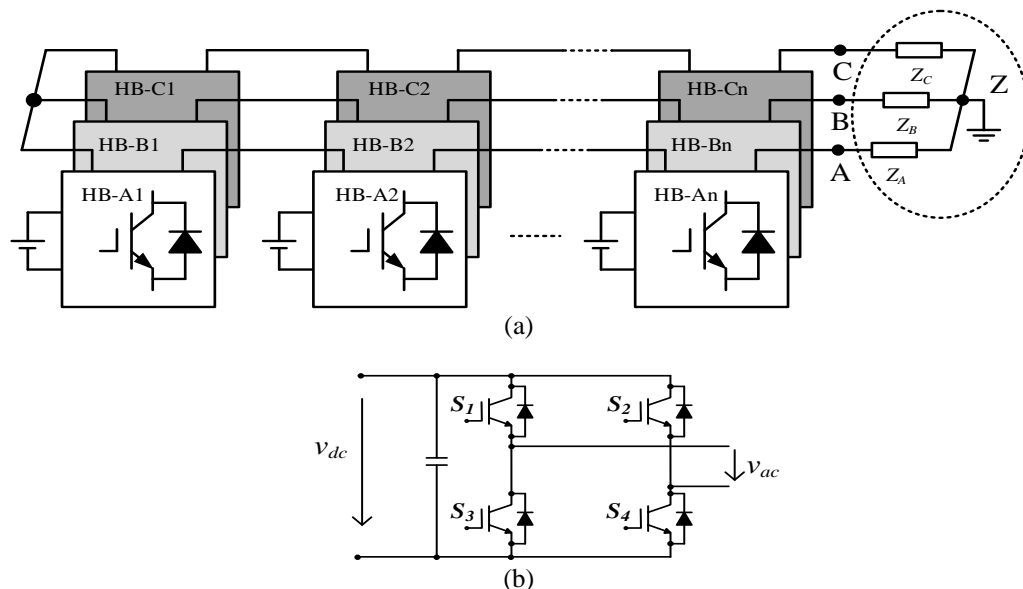

(a)

(b)

Figure 1. (a) Structure of a CHB inverter; (b) Topology of a cell

Assume that each phase consists of n cells connected in series and each cell is fed with an independent dc voltage source V_{dc}. The power switches S_1-S_4 in cell i of a phase can be controlled to generate

three voltage levels $\{+V_{dc}, 0, -V_{dc}\}$ corresponding to cell state $S_{xi} = \{1, 0, -1\}$ where x represents phase a, b or c. The voltage level of a phase is defined as the sum of all cell states in that phase as following:

$$S_x = \sum_{i=0}^{n} S_{xi} \tag{1}$$

The number of possible voltage levels for one phase is:

$$m = 2n + 1 \tag{2}$$

The output voltage of each phase is calculated by

$$v_{AN} = V_{dc} \sum_{i=0}^{n} S_{ai} \; ; v_{BN} = V_{dc} \sum_{i=0}^{n} S_{bi} ; v_{CN} = V_{dc} \sum_{i=0}^{n} S_{ci} \tag{3}$$

2.2. Space voltage vector of 3-level CHB inverter

A voltage vector is formed by a combination of switching states. The total combinations of the CHB inverter is as follow:

$$K_m = (2n + 1)^3 \tag{4}$$

$$K_v = 12n^2 + 6n + 1 \tag{5}$$

In multilevel CHB converters, same voltage vector can be implemented by several combination of switching states. Hence, the number of voltage vectors are normally less than the total switching states as following [9]. In this research, a three phase three level CHB inverter is used with 27 possible voltage vectors in static αβ coordinate. By eliminating the switching states which generate high common-mode voltage, the number of employed voltage vectors are reduced to 19 as shown in Figure 2. These voltage vetor are employed in the FCS-MPC in the next section.
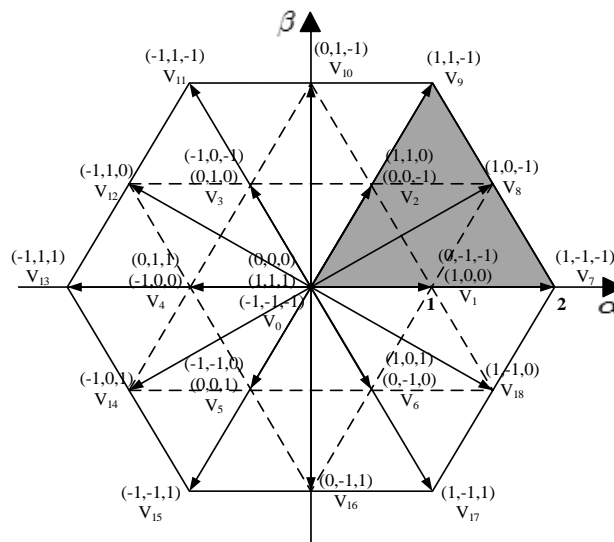

Figure 2. Space voltage vector of a 3-level CHB inverter

2.3. Modeling of the induction motor

In stationary frame αβ, the behavior of the IM can be represented by the following equations:

$$\mathbf{u}_s^s = R_s \boldsymbol{i}_s^s + \frac{d\boldsymbol{\Psi}_s^s}{dt} ; \; 0 = R_r \boldsymbol{i}_r^s + \frac{d\boldsymbol{\Psi}_r^s}{dt} - jz_p \omega \boldsymbol{\Psi}_r^s \tag{6}$$

$$\boldsymbol{\Psi}_s^s = L_s \boldsymbol{i}_s^s + L_m \boldsymbol{i}_r^s \,;\, \boldsymbol{\Psi}_r^s = L_m \boldsymbol{i}_s^s + L_r \boldsymbol{i}_r^s \qquad (7)$$

In which $R_s, L_s R_r, L_r$ are resistance and inductance of the stator and rotor, respectively.

The current and flux of the stator and rotor are expressed in vector form as follow:

$$\boldsymbol{u}_s^s = [u_{s\alpha} \ u_{s\beta}]^T \,;\, \boldsymbol{i}_s^s = [i_{s\alpha} \ i_{s\beta}]^T \,;\, \boldsymbol{i}_r^s = [i_{r\alpha} \ i_{r\beta}]^T \,;\, \boldsymbol{\Psi}_s^s = [\Psi_{s\alpha} \ \Psi_{s\beta}]^T \,;\, \boldsymbol{\Psi}_r^s = [\Psi_{r\alpha} \ \Psi_{r\beta}]^T \qquad (8)$$

Defining new variables as:

$$\boldsymbol{\Psi}_{rm}^s = \frac{1}{L_m} \boldsymbol{\Psi}_r^s \,;\, T_r = \frac{L_r}{C_r}, T_s = \frac{L_s}{R_s} \,;\, \delta = 1 - \frac{L_m^2}{L_s L_r} \qquad (9)$$

A fundamental manipulation on (1) and (2) results in:

$$\frac{d\boldsymbol{i}_s^s}{dt} = A_1 \boldsymbol{i}_s^s + B_1 \boldsymbol{u}_s^s + P \boldsymbol{\Psi}_{rm}^s$$

$$\frac{d\boldsymbol{\Psi}_{rm}^s}{dt} = A_2 \boldsymbol{\Psi}_{rm}^s + B_2 \boldsymbol{i}_s^s \qquad (10)$$

with

$$A_1 = \begin{bmatrix} -\left(\dfrac{1}{\delta T_s} + \dfrac{1-\delta}{\delta T_r}\right) & 0 \\ 0 & -\left(\dfrac{1}{\delta T_s} + \dfrac{1-\delta}{\delta T_r}\right) \end{bmatrix}, B_1 = \begin{bmatrix} \dfrac{1}{\delta L_s} & 0 \\ 0 & \dfrac{1}{\delta L_s} \end{bmatrix}, P = \begin{bmatrix} \dfrac{1-\delta}{\delta T_r} & \dfrac{(1-\delta)\omega}{\delta} \\ -\dfrac{(1-\delta)\omega}{\delta} & \dfrac{1-\delta}{\delta T_r} \end{bmatrix}, A_2 = \begin{bmatrix} -\dfrac{1}{T_r} & -\omega \\ \omega & -\dfrac{1}{T_r} \end{bmatrix}, B_2 = \begin{bmatrix} \dfrac{1}{T_r} & 0 \\ 0 & \dfrac{1}{T_r} \end{bmatrix}$$

For MPC control design, the continuous-time model (10) needs to be transformed into discrete-time model with sampling period T_s by using forward-Euler method as following:

$$\boldsymbol{i}_{s,k+1}^s = \Phi_1 \boldsymbol{i}_{s,k}^s + \Gamma_1 \boldsymbol{u}_{s,k}^s + D_k \boldsymbol{\Psi}_{rm,k}^s$$

$$\boldsymbol{\Psi}_{rm,k+1}^s = \Phi_2 \boldsymbol{\Psi}_{rm,k}^s + \Gamma_2 \boldsymbol{i}_{s,k}^s \qquad (11)$$

in which

$$\Phi_1 = I_2 + T_s A_1 \,;\, \Phi_2 = I_2 + T_s A_2 \,;\, \Gamma_1 = T_s B_1 \,;$$

$$\Gamma_2 = T_s B_2 \,;\, D_k = T_s P \,;\, I_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

Based on (11), the predictive current in N step ahead can be computed by:

$$\begin{bmatrix} \boldsymbol{i}_{s,k+1}^s \\ \boldsymbol{i}_{s,k+2}^s \\ \dots \\ \boldsymbol{i}_{s,k+N}^s \end{bmatrix} = \begin{bmatrix} \Gamma_1 & 0 & \dots & 0 \\ \Phi_1 \Gamma_1 & \Gamma_1 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ \Phi_1^{N-1}\Gamma_1 & \Phi_1^{N-2}\Gamma_1 & \dots & \Gamma_1 \end{bmatrix} \begin{bmatrix} \boldsymbol{u}_{s,k+1}^s \\ \boldsymbol{u}_{s,k+2}^s \\ \dots \\ \boldsymbol{u}_{s,k+N}^s \end{bmatrix} + \begin{bmatrix} \Phi_1 \\ \Phi_1^2 \\ \vdots \\ \Phi_1^N \end{bmatrix} \boldsymbol{i}_{s,k}^s + \begin{bmatrix} D_k & 0 & \dots & 0 \\ \Phi_1 D_k & D_k & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ \Phi_1^{N-1}D_k & \Phi_1^{N-2}D_{k+1} & \dots & D_{k+N-1} \end{bmatrix} \begin{bmatrix} \boldsymbol{\Psi}_{rm,k}^s \\ \boldsymbol{\Psi}_{rm,k+1}^s \\ \dots \\ \boldsymbol{\Psi}_{rm,k+N-1}^s \end{bmatrix}$$

$$(12)$$

3. CONTROL DESIGN
3.1. FCS-MPC design

The block diagram of the IM control system is shown in Figure 3(a) which conists of two outer loops including a speed regulator, a flux regulator and an inner current loop using FCS-MPC. The two outer loops designed in synchronous reference frame *dq* generate the reference stator currents. Then, these reference currents are transformed into αβ coordinate and used for the FCS-MPC design. Based on the IM

model, the optimal voltage vector is chosen to minimize a cost function in which one or several objectives may be considered such as: minimal tracking error, capacitor volage balance, minimal switching loss, etc. The detail FCS-MPC algorithm which is activated in every consecutive sampling period is shown in Figure 3(b), in details.
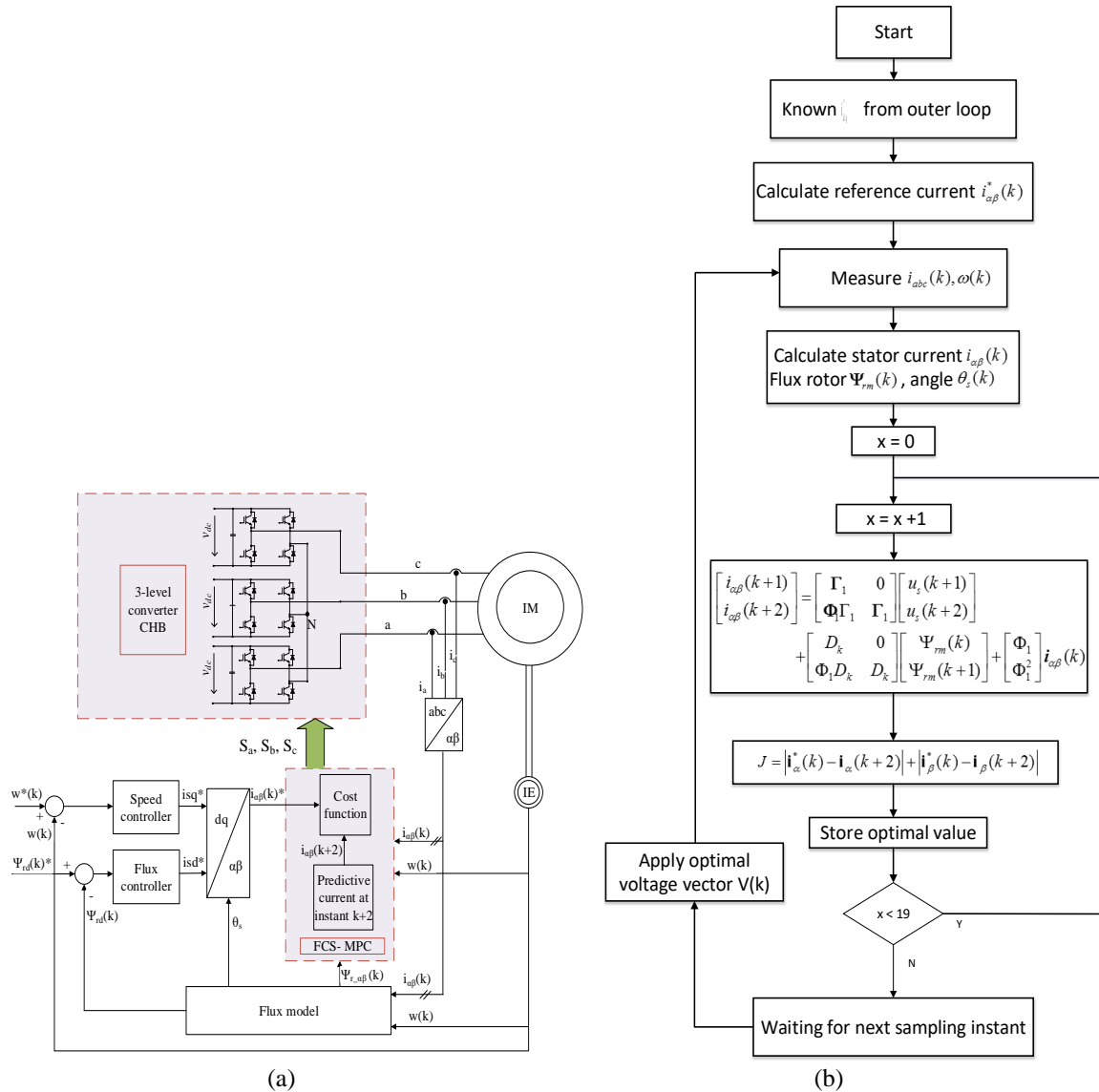

Figure 3. FCS control strategy, (a) IM control scheme, (b) Predictive current control algorithm

3.2. Cost function selection

In this research, the cost function is chosen based on the predictive current error in αβ coordinate of the induction motor.

3.2.1. Formulation of the current error

The error between the predictive current and its reference can be expressed as an absolute value, square value or integral value [3]. If only the present tracking error is used by the cost function, absolute error and square error give same performance. When the present and past values of the tracking error are considered, the square of error gives better tracking performance than the absolute error while the integral of error gives the best performance. However, a cost function with integral of tracking error also requires higher computational cost.

3.2.2. Delay compensation

In the ideal case, the time needed for calculation is negligible. Assume that the currents are measured at time instance t_k, the optimal voltage vector that minimizes the error at time instance t_{k+1} is chosen and applied immediately at t_k. Therefore, the load current tracks the predicted current at t_{k+1}. However, if the calculation time is significant compared to the sampling time, there is a delay between the measured current insant and the applied new voltage vector instant. During the delay time, the previous voltage vector is still applied, which makes the load current move away from the reference and increases the current ripple. A simple solution to compensate this delay is to take the calculation time into account and apply the selected voltage vector after the next sampling instant [3, 14, 16]. The load current reaches the predicted value at t_{k+2}.

3.2.3. Prediction of future references

In general, the future references are unknown and needed to be estimated by using a second-order extrapolation [10]. However, for sufficiently small sampling time, the future reference value at time t_{k+2} is assumed to be approximately equal to the present reference value at time t_k [3]: $i_{\alpha\beta}^*(k) \approx i_{\alpha\beta}^*(k+2)$. Based on the aforementioned analysis, the cost function is chosen as:

$$J = \left| i_\alpha^*(k) - i_\alpha(k+2) \right| + \left| i_\beta^*(k) - i_\beta(k+2) \right| \tag{13}$$

$i_{\alpha\beta}^*(k)$: Reference stator current of the motor in $\alpha\beta$ coordinate at time instance t_k.

$i_{\alpha\beta}(k+2)$: Predictive stator current of the motor in $\alpha\beta$ coordinate at time instance t_{k+2}.

4. FPGA IMPLEMENTATION

4.1. Functional internal circuit (IC) design.

A complicated algorithm can be divided into many smaller calculation steps and an internal circuit needs to be designed and programed functionaly to perform each step. An IC includes two fundamental blocks: a finite state machine (FSM) and a processing unit (PU) as shown in Figure 4(a). The FSM block contains all finite states of the IC and control signals to processing unit. Meanly or Moore method are usually used to design the FSM with several typical signals: *clk*, *rst*, *init* and *done*. In which, *Clk* and *rst* are operating clock and reset signal for the circuit, respectively. *Init* and *done* signal is set to '1' for only one clock period when the IC starts and finishes its operation. The *done* signal is connected to the *init* signal of the other circuit so that sequential calculation can be implemented. Since an internal circuit only operates in a fixed small time and is inactive most of the time, this design avoids the propagation of unespected glitches and reduces the FPGA power consumption. The PU block contains operators +, -, x, / and takes *Data_in* as input data to calculate and then send the results to the *Data_out* under the control of the FSM. The structure of the PU is designed by the pipelined structure as shown in Figure 4(b) to synchronize the data and signals. c. Predictive current control implementation based on FPGA platform.

The flow chart shown in Figure 5(a) illustrates how to implement the FCS-MPC for current loop of the IM on a FPGA platform. To solve the algorithm described in the previous section, there are nine steps corresponding to nine internal circuits. The name of *Step1 to Step9* are: *ADC_read*, *abc_to_αβ*, *Dq_to_αβ*, *Is_to_flux*, *Pre_model*, *J_calc* circuit, *Find_mindJ*, *αβ_to_dq* and *Flux_model*, respectively. Since *Step2* requires the data calculated in *Step1* while *Step3* requires the data from *Step2*, the operation of circuits 1,2,3 is sequential. Similarly, the circuits 3,5,6,7 and 8,9 must run sequentially. Meanwhile, *Step5* requires the data from both *Step3* and *Step4*, so that circuit 3 and 4 must operate in parallel. Because circuit 4 needs more calculation time than circuit 3, circuit 5 only take the input data when circuit 4 ends its operation, which means the *done* signal of circuit 4 is the *init* signal of circuit 5. On the other hand, *Step9* only requires data from *Step8* which means circuit 8 and 9 operate in parallel with circuit 3,5,6,7. Finally, the execution time of the FCS-MPC is shown in Figure 5b. As can be observed, several steps can be carried out in parallel which reduces the computational time of the implemented algorithm. The parallel computation ability of the FPGA, which is not available in conventional DSP/microcontroller, allows the MPC to be applied to many other fields without having to worry about the computational time.
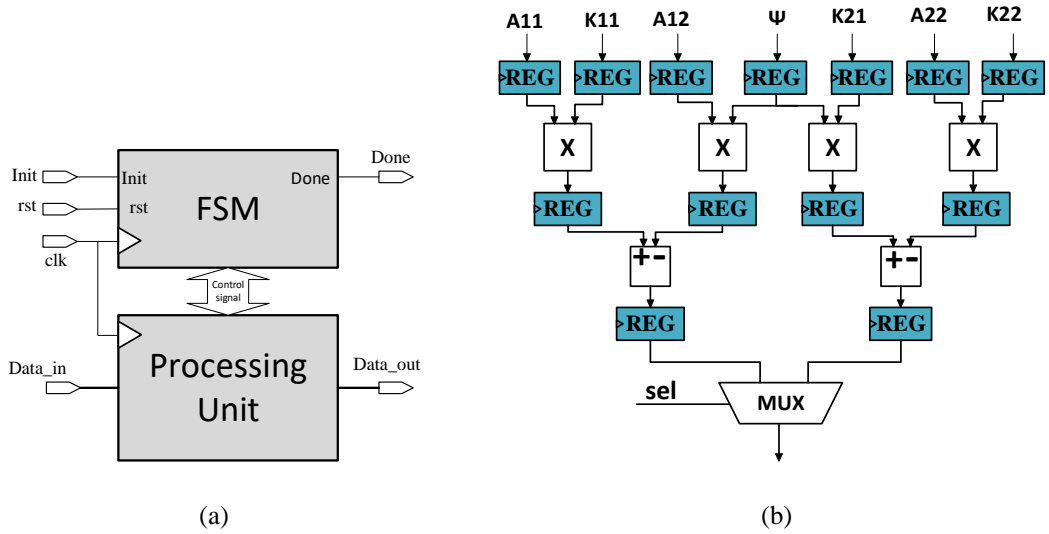
(a)   (b)

Figure 4. Functional, (a) IC structure, (b) Pipelined structure

(a)   (b)

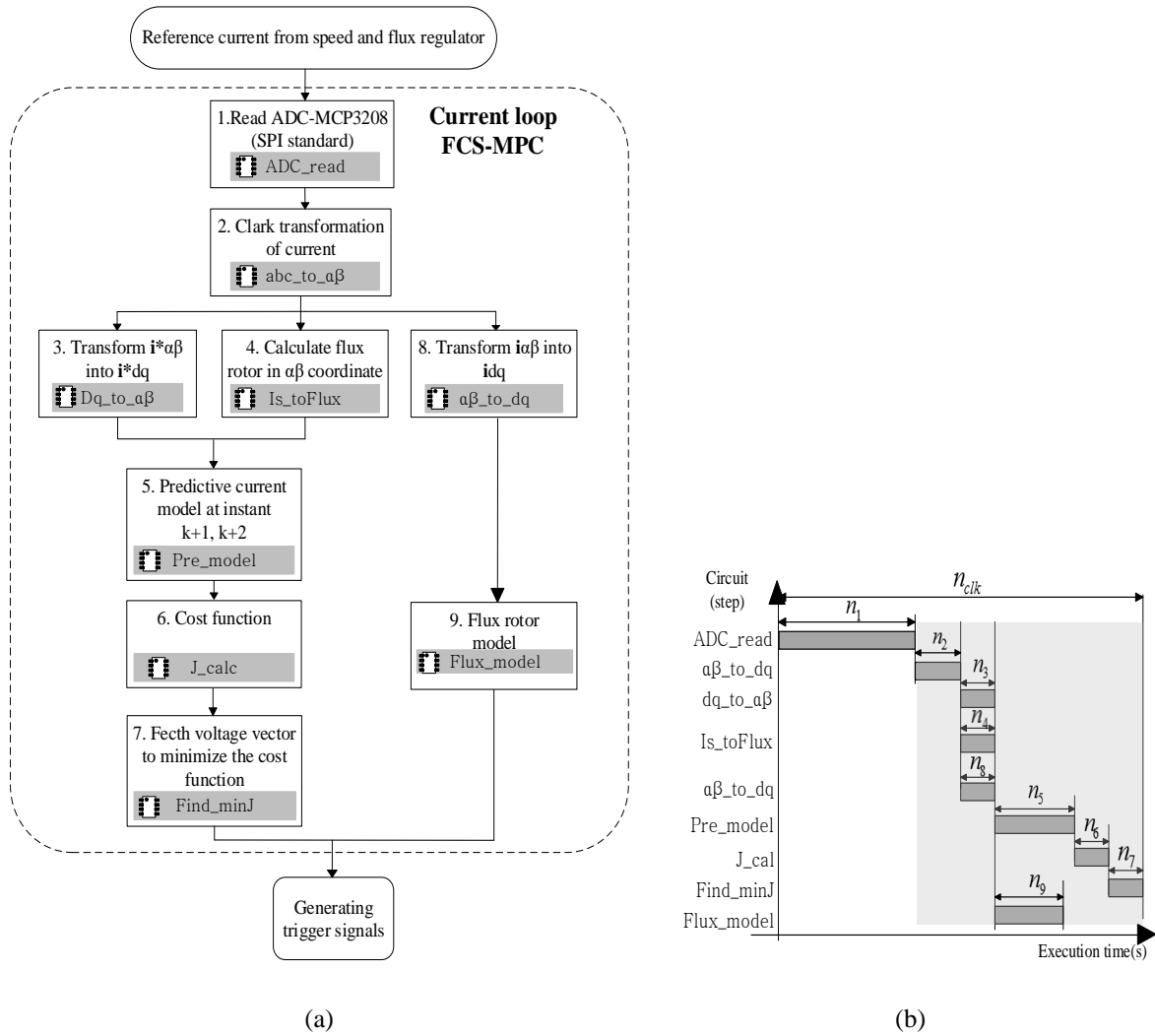Figure 5. Flowchart, (a) FPGA implementation (b) IC's execution time

4.2. HIL-FPGA platform

To quickly verify the FCS-MPC for IM without risky experiments, real-time simulation based on HIL platform are conducted. The virtual IM motor with parameters provided in Table 1 and the 3-level CHB inverter are simulted by Typhoon HIL 402 device. The control algorithm is implemented by a FPGA card named ZYBO-27. The block diagram and the experimental devices of the real-time simulation system are shown in Figure 6 and Figure 7, respectively.
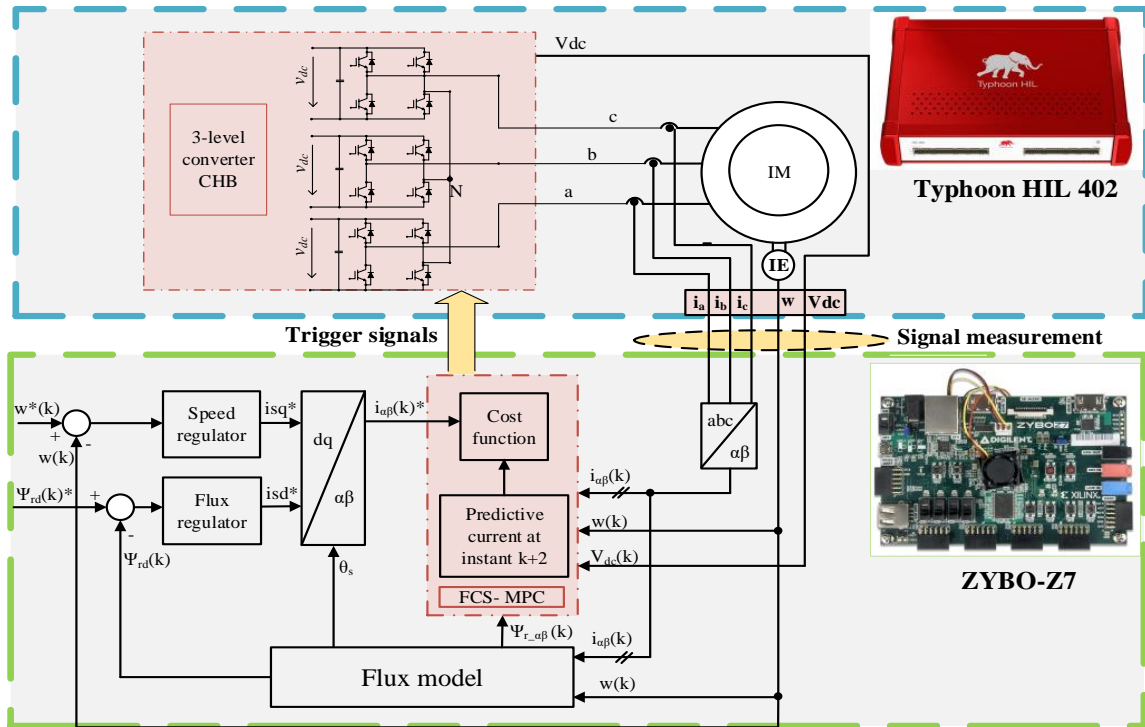

Figure 6. Block diagram of the HIL-based simulation system

Table 1. Parameters of the IM

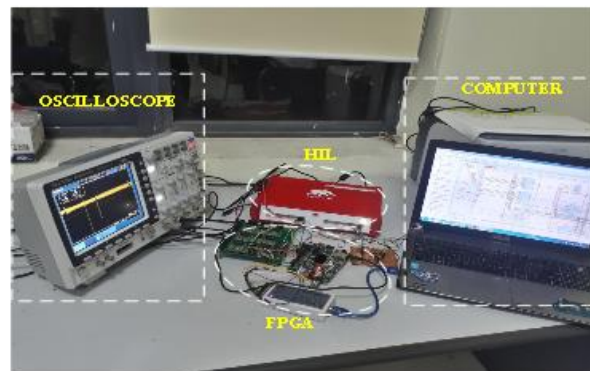| Symbol	Quantity	Value
P_{rate}	Rate power	2.2kW
T_{rate}	Rate torque	7.3Nm
I_{rate}	Rate phase current	4.7A
V_{rate}	Rate phase voltage	400V
f_{rate}	Rate frequency	50Hz
N_{rate}	Rate speed	2880 rpm
R_s	Stator resistance	1.99 Ω
R_r	Rotor resistance	1.84 Ω
L_m	Mutual inductance	0.37 mH

Figure 7. Experiment devices

5.   RESULTS AND DISCUSSION

In this section, various real-time simulations are carried out to verify the developed FCS-MPC applied to IM control. First, the transient response of the control system with the load disturbance is tested. At time instance $t=\{0.05s, 0.5s, 0.75s\}$, the load torque is suddenly changed with corresponding values $T_L=\{0, 0.5T_{rate}, T_{rate}\}$ while the reference speed is fixed at $\omega_{ref}=300(rad\ s^{-1})$. As can be observed in Figure 8, the electromagnetic torque generated by the IM quickly tracks the load torque to maintain the rotor

speed at its desired value. From time instance *t=1.5s*, speed reveral of the IM with constant load is investigated. The reference speed is changed at time instance *t=1.5s* and *t=4.3s* with corresponding values $N_{ref=}-N_{rate}$ and $N_{ref=}0$. In this case, the rotor speed also quickly trackes its reference with negligible tracking error, i.e., about 0.2 *rad/s*. In the second scenario, the ability to generate electromagnetic torque at standstill of the IM control system is clarified. With employed FCS-MPC for the current loop, the generated electromagnetic torque quickly tracks the load torque at zero speed in just *3ms* as shown in Figure 9. This quick response is sufficient for most practical applications and comparable to the well-known direct torque control (DTC).
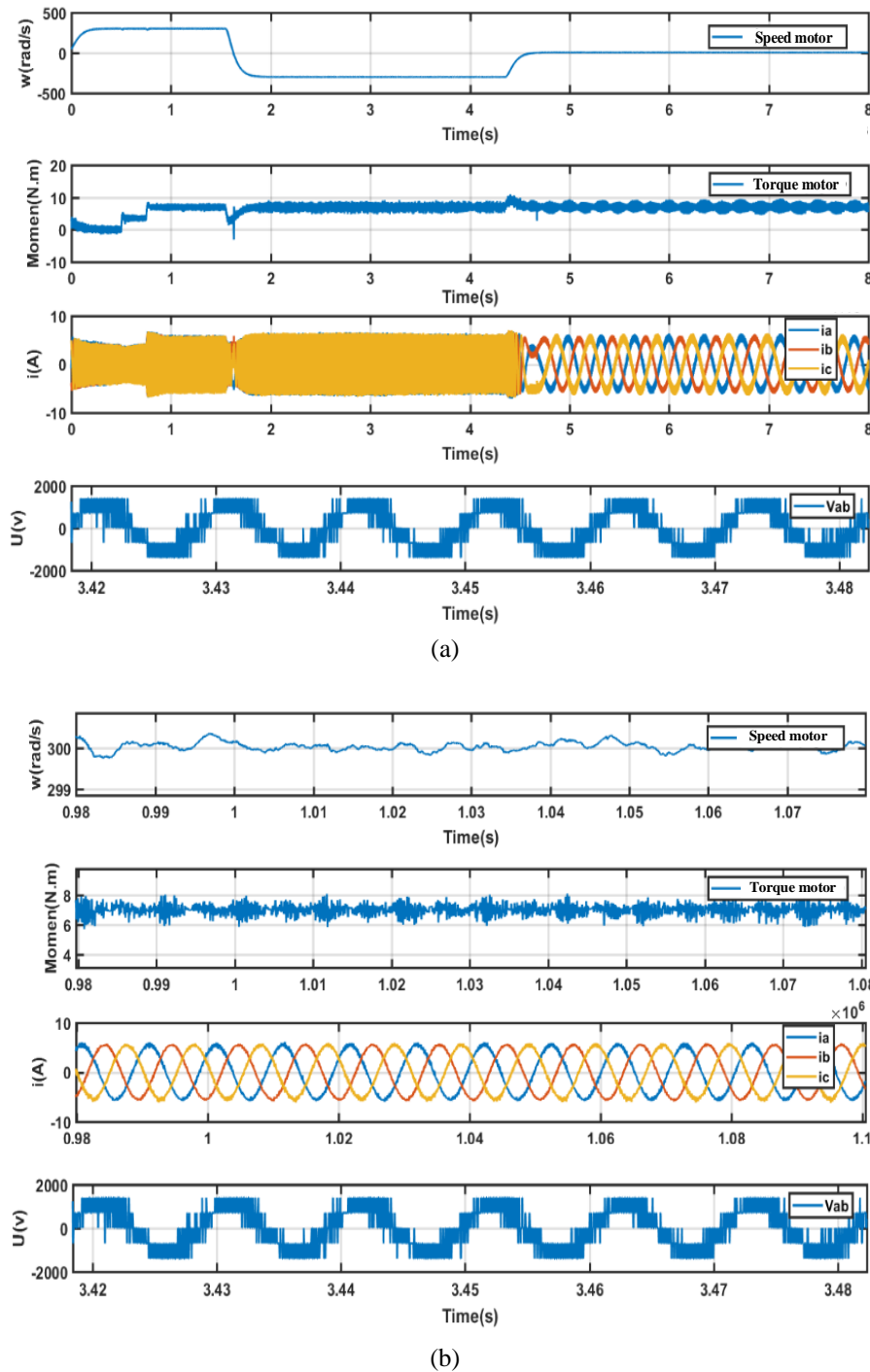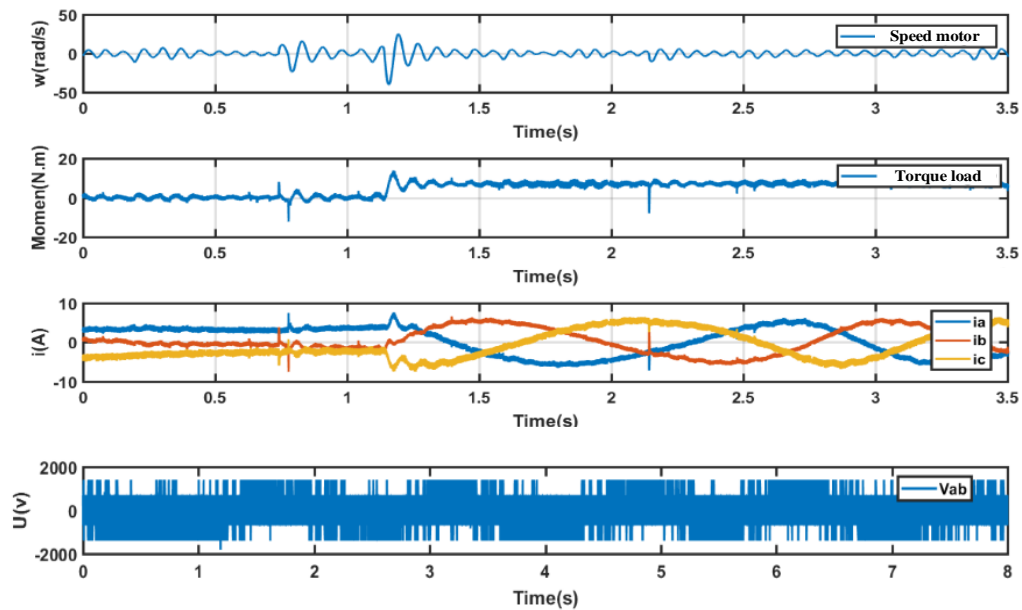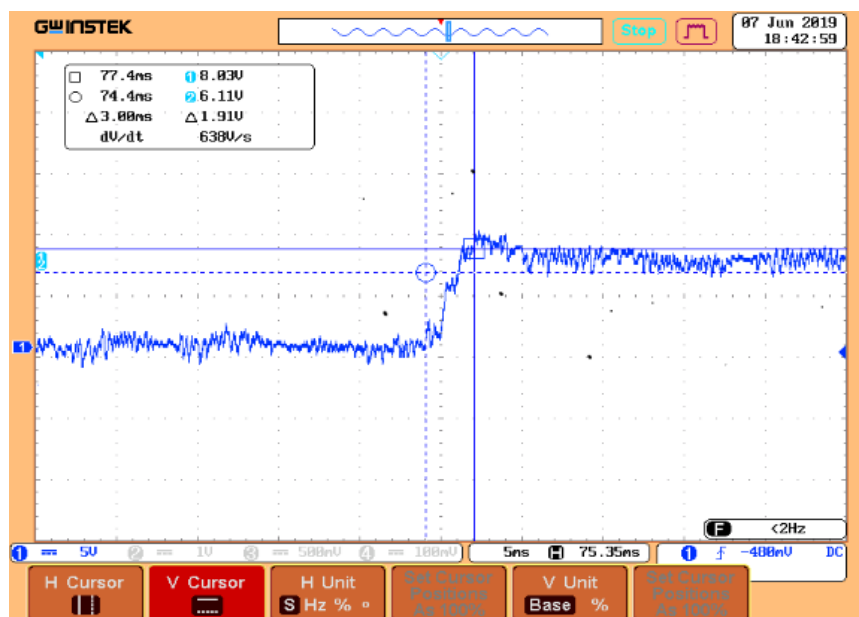

(a)

(b)

Figure 8. Electromagnetic torque, (a) Time-varying speed motor and load torque, (b) Zoom-in result

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(a)

(b)

Figure 9. Generated torque, (a) Load torque and load current at standstill, (b) Torque step response

6.   CONCLUSION

In this paper, an advanced solution to quickly develop the FCS-MPC for IM fed by multilevel CHB inverter is discussed. First, the behavior of the stator current in future is predicted with each of possible voltage vector based on the explicit discrete-time mathematical model of the IM. The optimal voltage vector which fulfill the objective of a predefined cost function is selected and applied to the CHB inverter. Second, the FPGA with parallel calculation ability is used to minimize the computational time of the complicated control algorithm like MPC. Finally, to eliminate the burden of time on hardware design as well as to avoid potential risks with high power experimental systems, real-time simulations with high-fidelity mathematical models implemented by HIL platform are conducted to verify the control algorithm. Achieved real-time simulations show that the developed FCS-MPC gives good performance not only in steady-state but also in transient-state.

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