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A high-performance multilevel inverter with reduced power electronic devices

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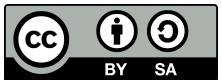
ABSTRACT

This paper introduces a new topology of multilevel inverter, which is able to operate at high performance. This proposed circuit achieves requirements of reduced number of switches, gate-drive circuits, and high design flexibility. In most cases fifteen-level inverters need at least twelve switches. The proposed topology has only ten switches. The inverter has a quasi-sine output voltage, which is formed by level generator and polarity changer to produce the desired voltage and current waveforms. The detailed operation of the proposed inverter is explained. The theoretical analysis and design procedure are given. Simulation results are presented to confirm the analytical approach of the proposed circuit. A 15-level and 31-level multilevel inverters were designed and tested at 50 Hz.



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1. INTRODUCTION

With the rapid development of power electronics, the demand of power converters are high performance, low cost and high power quality applications [1–3]. Reducing the number of switches in power electronics can improve the power density and leads to low voltage stress on switches [4–7]. Multilevel converters can attain both fundamental switching frequency and high switching frequency PWM [8–10]. Therefore, multilevel inverters with separate DC sources are suited for operation at low frequency to achieve low switching losses and high efficiency [11–13]. Inverters in such application handle high voltage and extensive power. Thus, high-level inverters, which are composed of switching power devices integrated gate bipolar transistors (IGBTs), are suitable to achieve high voltage applications [14, 15]. Most conventional multilevel inverters, such as Flying Capacitor (FC), Neutral Point Clamped (NPC), and Cascaded H-Bridge (CHB) suffer from high-voltage stress on switch, high Electro Magnetic Interference (EMI) and poor power quality output [16–18]. In order to solve these issues, a new topology of multilevel inverter is presented.

In last few decades, several authors have been increasingly focused on multilevel inverter topologies with reduction in numbers of power switches [19–23]. Topology [24] is combined of IGBT and diode causing reduction in efficiency. In addition, the losses and cost will be increased and its industrial applications will be restricted. In [25] sub-multilevel converter blocks are connected in series. This circuit consists of capacitors and four bi-directional switches are utilized in each unit. Thus, the installation area is increased in the proposed topology. Most of the multilevel inverters suffer from high voltage stresses at the power switches and require different voltage rating of the power switches. In addition, switching frequency leads to a decrease in efficiency

due to switching losses. Therefore, the proposed topology is attractive for high-performance applications.

This work proposes a high power quality multilevel inverter with reduced in numbers of power semiconductor devices. The proposed topology can attain a large number of levels with asymmetric DC voltage sources. This topology is based on the conventional inverter that utilizes level generation and polarity change. The new circuit can be utilized for 15-level and 31-level inverter. To implement a 15-level inverter, ten IGBT switches and three dc voltage sources are selected. The multilevel inverter generates staircase voltage waveform with decreased electromagnetic compatibility (EMC) issues and low distortion. The new topology also utilizes low number of power switches and includes a low-design complexity. The described topology also shows in details the analysis of the steady-state voltage waveforms. In order to determine an appropriate characteristics of the multilevel inverter, a design procedure has been applied. The proposed circuit was simulated and tested at a frequency of 50 Hz. A control unit of signals are used to generate fixed values of operating frequency and duty ratio. Collectively, these features make the new multilevel inverter advantageous in applications, such as AC drives and FACTS devices.

2. ANALYSIS OF THE PROPOSED MULTILEVEL INVERTER TOPOLOGY

Figure 1 shows the proposed multilevel inverter circuit. The proposed topology consist of level generate and polarity change. The level generation has power switch P_i and power switch S_i, which is connected in series with the DC voltage source V_i. The circuit of polarity change is comprised H-Bridge power switches HS_i and connected in parallel with the load. In this study, IGBT transistors, which have high switching performance, are used in the proposed topology. We focus on identifying the characteristics of the proposed inverter to provide a flexible output voltage waveform across the load of the circuit with minimum number of switches.

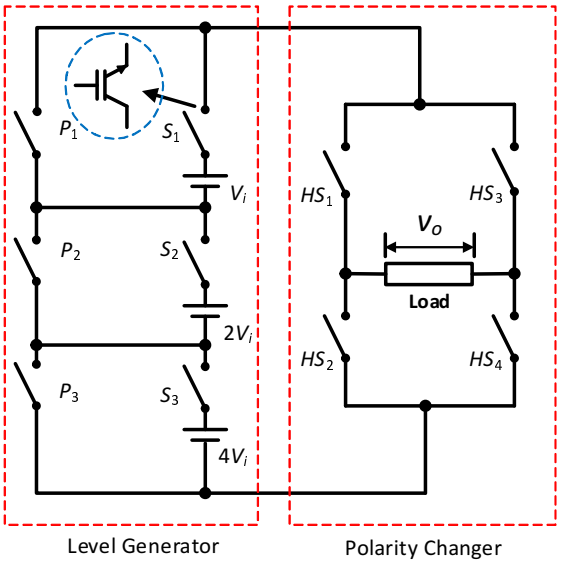

Figure 1. Proposed multilevel inverter circuit

The new topology can produce fifteen-level output during asymmetric condition. The operating modes during asymmetric operation of the circuit to obtain alternating output voltage across the load is shown in Figure 2. The proposed topology requires six switches and three DC voltage sources to generate positive-levels steps output voltage at the load as shown in the left part of the inverter. A polarity changer, which is comprised of four switches, is added to generate the negative-levels steps output voltage at the load. The switches HS_i are utilized to reverse the polarity of the output voltage of the inverter. The analysis of the proposed circuit is based on the the ON-state and the OFF-state of the switches P_i and S_i, respectively. The switches HS_1 and HS_4 are ON during the positive cycle of the operation, while the switches HS_2 and HS_4 are OFF during the negative cycle of the operation.

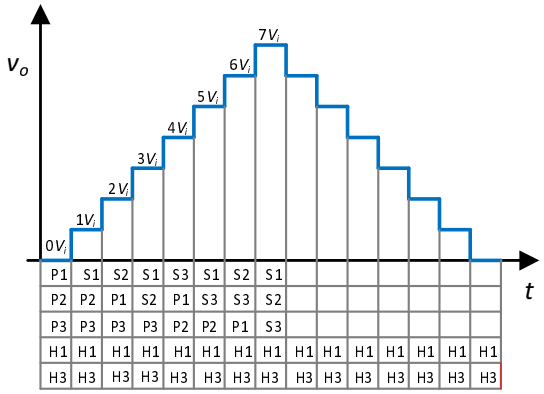

Figure 2. Operation mode of switches.

Figure 3 shows the illustrating operation of idealized steps of the circuit over a period. As can be seen, each step for output voltage is double of the voltage source V_i. The switches P_i and S_i of the inverter can be derived according to the control unit circuit to generate pulse width modulator waveforms as shown in Figure 4.

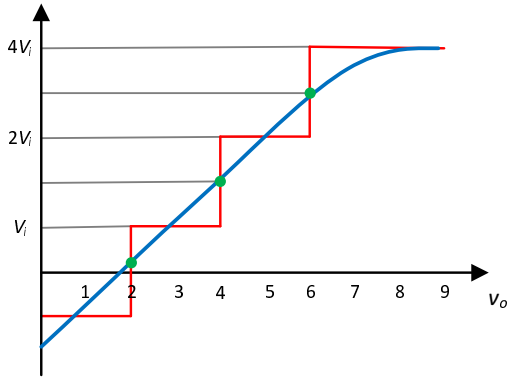

Figure 3. Level modulation technique

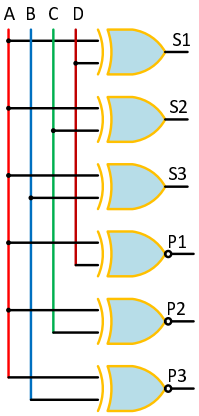

Figure 4. Control unit of signals for 15-level switches

To establish the design equations, the circuit behavior is analyzed in each interval. It is considered V_i as a reference voltage in the proposed multilevel inverter. The number of DC voltage sources NV base on the number of unit cell m in the inverter

$$N = 2^m, \tag{1}$$

where, $m = 0, 1, 2, 3...i$. The steps of output voltage D_{steps} can be found as

$$D_{steps} = 2^{i+2} - 1. \tag{2}$$

The maximum output voltage v_O is the sum of DC voltage sources N

$$v_O = \left(\frac{D_{steps} - 1}{2}\right) V_i. \tag{3}$$

The power switches of the proposed topology can be switched at any duty cycle D. It can be determined based on the specifications of the multilevel inverter.

3. DESIGN PROCEDURE

A design procedure for the new multilevel inverter is presented to supply a resistive load at operating frequency $f_s = 50$ Hz. In the design procedure, the following design parameters V_i, v_O, and D are determined. The reference DC voltage source V_i for 15-level and 31-level were chosen to be 45 V and 20 V , respectively. Furthermore, the duty cycle of power switches is 50%. The reference DC voltage V_i can be selected basing on the application of the inverter. In the proposed circuit, the designer can easily adjust the value of duty cycle to achieve the required driven voltage waveform of the power switches. For 15-level output and step voltage 45 V, the peak-to-peak output voltage of the multilevel inverter is varied from +312 to -312. For the 31-level inverter, the reference DC voltage $V_i =$ 20 V is applied at the proposed circuit, the peak value of voltage stress is 312 V at duty cycle $D =$ 50%. The peak value of the voltage stress depends on the total DC source voltage on the power switch. The value of v_{GE} voltage based on the characteristics of the power switch IGBT in the inverter. Therefore, it is important to select a proper driving voltage rating for the power switch. In this work, the voltage v_{GE} rating of the power switch, which is utilized in the gate driver, is 20 V. The transistor BUP306D was utilized as a IGBT power switch in circuit. The load of the proposed inverter is chosen to be a resistive load $R_L = 50\ \Omega$.

The major differences between the proposed topology and the popular multilevel inverters are the number of power switches and the type of switching. Thus, most multilevel inverter circuits operate at least twelve power switches. To operate fifteen-level inverter, the proposed multilevel inverter has six switches in the level generation and four switches in the H-bridge. Furthermore, the switching behavior of IGBT transistors in the proposed multilevel inverter can achieve high voltage applications. Therefore, the performance of the inverter can increase the efficiency of the inverter. These features show the the advantage of the new circuit. The specifications and parameters of the circuit are given in Table 1.

Table 1. List of parameters for multilevel inverter at $f_s = 50$ Hz

Components	Value
BUP306D	$V_{CE} = 1200$ V, $V_{GE} = 20$ V, $I_C = 23$ A $C_{iss} = 1300$ pF, $C_{oss} = 100$ pF, $C_{rss} = 50$ pF
R	50 Ω
V_i	45 V, 20 V

4. SIMULATION RESULTS

Based on the design methodology and the circuit operation, the proposed multilevel inverter has been verified through MatLab simulation. The performance of the proposed topology during the asymmetric operation is analyzed. A 50 Hz PWM signal is used to supply the power switches, and the value of duty cycle is $D =$ 0.5. A BUP 306D IGBT power switch with anti parallel diode (1200 V, 23 A) from Siemens was used as the power transistor in the multilevel inverter circuit. In order to make the circuit operates in high performance, this power switch is optimized for low switching losses and high-speed operating. The proposed topology is simulated for 15-level inverter and 31-level inverter, respectively.

4.1. 15-level multilevel inverter

To generate appropriate switching Pulse Width Modulation schemes for the power switches, the circuit in Figure 4 is used. The fundamental frequency is utilized to generate the switching pulses in the circuit. According to the switching states, the pulses are generated at each step to drive the power switches as shown in Figure 5. If the pulses form accurately, the efficiency and harmonic distortion can be controlled effectively in the proposed multilevel inverter. The switches of H-bridge are operated in a complementary mode to produce the positive and the negative levels steps output voltage at the load. The inverter provides the AC signal with a peak magnitude 312 V to the load, when the dc voltage source is 45 V. In order to observe the step voltage waveform at the output resistor, the zoomed waveform of the output voltage for the multilevel inverter is shown in Figure 6. It can be seen that the step size of the waveform is 45 V. The step level of the inverter was captured in Figure 7. It is clear that the output voltage is close to sine waveform. The presented approach proves that the new inverter provides low-voltage stress and small-valued components.

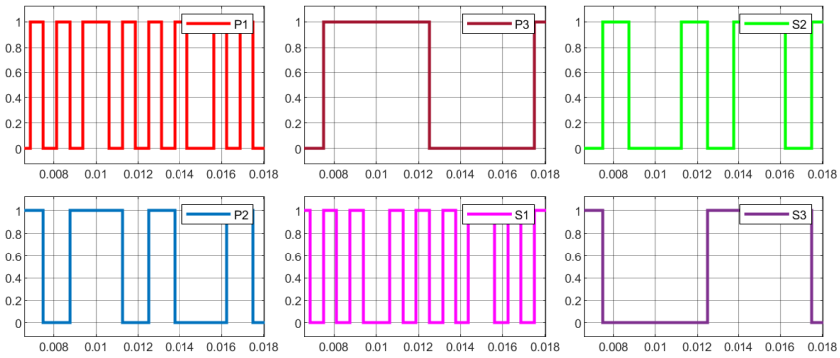

Figure 5. Simulated 15-level switching pulse waveforms of multilevel inverter

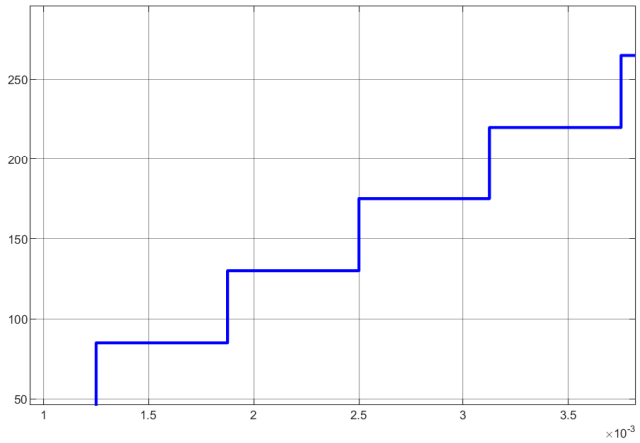

Figure 6. Simulated of 15-level zoomed output voltage waveform

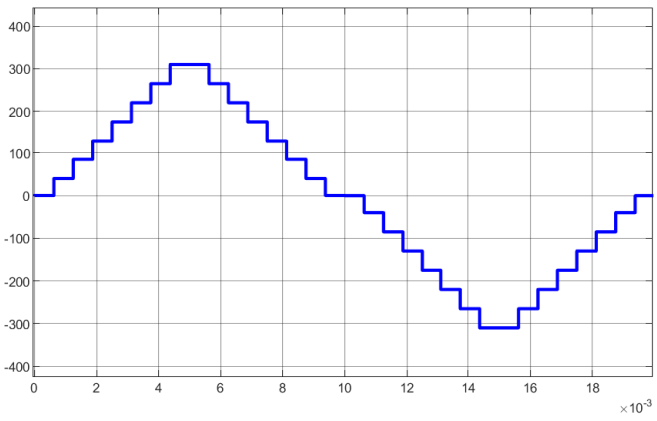

Figure 7. Simulated of 15-level multilevel inverter waveform

4.2. 31-level multilevel inverter

The proposed topology can be utilized for 31-level to generate AC waveform close to sine signal. The power switches of 31-level circuit are derived by the control circuit to form switching pulses as shown in Figure 8. The output voltage waveform in Figure 9 shows the operation of 31-level of the proposed topology. It is clearly shows that the operation of the circuit is obtained by the level generation and change polarity circuit to supply the AC signal to the load. The maximum value of the voltage stress was measured as 312 V for the input voltage $V = 20$ V. The peak-to-peak output voltage of the multilevel inverter across the load is varied from +185 to -185. It can be noticed that the output voltage is close to sine waveform.

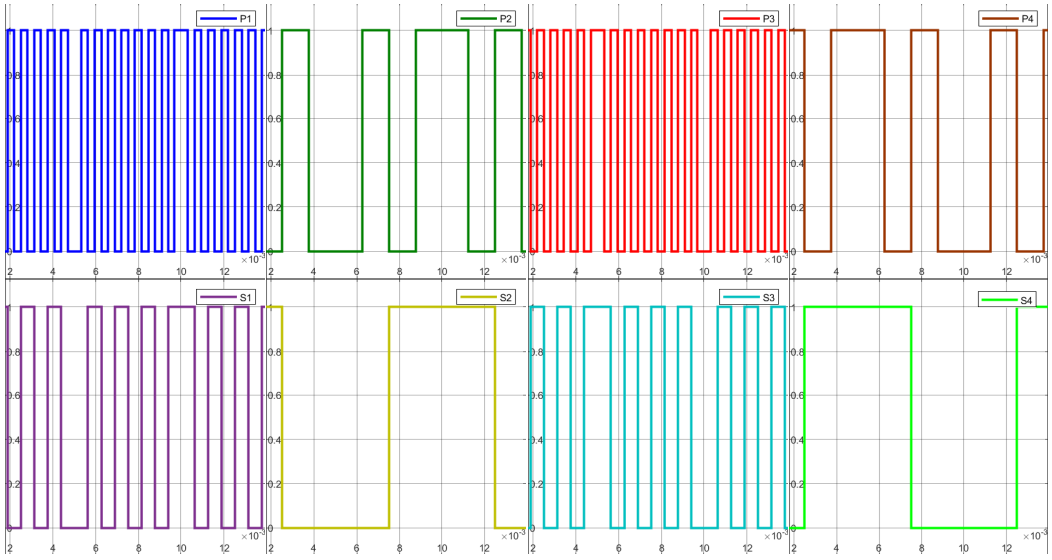

Figure 8. Simulated 31-level switching pulse waveforms of multilevel inverter

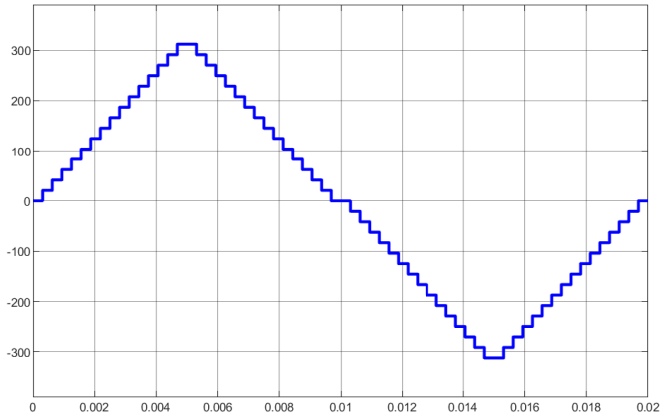

Figure 9. Simulated 31-level multilevel inverter waveform.

5. CONCLUSION

A new switched-mode multilevel inverter, which is derived from conventional multilevel inverter, has been introduced. This topology operates at constant duty cycle and frequency. The new topology can be designed for 15-level and 31-level inverter. An H-bridge is added in the proposed topology to generate negative voltage levels. It has a low number of power switches, low switch voltage stress, low DC voltage sources, and flexible design. The new circuit is designed to supply AC signal to the load even when low-input voltage of the inverter is available. Based on above analysis, the prototype with 50 Hz was designed and simulated. The simulation testing results demonstrate a good agreement between the simulations and the calculations. The proposed circuit can be used in applications that demand high performance, such as FACTS controllers and adjustable motor drives.

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