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Design of a high performance AC-DC LED driver based on SEPIC topology

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ABSTRACT

Light emitting diodes (LEDs) are current driven devices. So, it is essential to maintain the stability of LED voltage and current. Variation of temperature may cause of instabilities and bifurcations in the LED driver. Driving LEDs from an offline power source faces design challenges like it have to maintain low harmonics in input current, to achieve high power factor, high efficiency and to maintain constant LED current and to ensure long lifetime. This paper proposes the technique of harmonics reduction by using parametric optimization of Single ended primary inductor converter (SEPIC) based LED driver. Without optimization of SEPIC parameters input energy will not be properly transferred to the load and this un-transferred energy will be transmitted to the source. Consequently, the quality of input current will be hampered i.e. harmonics will contaminate the input current. Focussing this, the paper has presented the design of a non-isolated integrated-stage single-switch constant current LED driver operating in discontinuous conduction mode (DCM) in SEPIC incorporating the design of control circuit with soft start mechanism. This LED driver has achieved a good efficiency (90.6%) and high-power factor (0.98) with reduced harmonics (3.35%). System stability has been determined and simulation studies are performed to confirm the validity of the LED driver circuit. A laboratory prototype is built to verify the functionality and performance of the proposed LED driver.

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1. INTRODUCTION

The advancement of lighting technology is mostly due to the advent of high-luminance light emitting diode (LED). In order to ensure good exploitation of LEDs, a highly energy-efficient and reliable LED driver with constant current output is utterly necessary. In AC-DC LED application systems input AC goes through rectification and DC/DC conversion according to the load requirements. The use of some circuit elements like diodes, MOSFET are the cause of extreme deformation in input current. PFC converters are required in AC/DC conversion to ensure high power factor. For PFC applications some circuit topologies like boost, buck-boost, SEPIC, and Cuk are immensely used.

Classic LED systems are based on single-stage or multi-stage or integrated stage LED drivers. Single stage single switch AC-DC converters are more accepted for lower cost and size. But output voltage control and power quality are sacrificed [1] relative to two stage approach. The two stages and multiple stages are used for higher power level and multiple load conditions [2], [3], but in small and medium power application it has some drawbacks such as low efficiency, multiple control and high cost. A lot of research

works has been done on harmonic reduction and power factor corrections (PFC) in LED application over the last ten years [4]-[7].

High power factor and low input-current harmonics are becoming the mandatory design criteria for switching power supplies. In order to obtain high PF and low THD, a family of single-stage isolated PFC cell like buck, boost are advanced [8]-[13]. Those LED drivers suffer from voltage spikes arisen across the switch, high complexity, and zero-crossing distortion of input current. LED Driver in reference [14], [15] suffers from low efficiency.

In comparison to various topologies, the SEPIC is more satisfactory solution for achieving high power factor in low-power LED lighting application. Jha [16] proposes a LED driver with good power factor and good total harmonic distortion (THD) with constant LED current. But complexity of the driver decreases efficiency. In Hwu [17] the LED driver is capacitor and inductor less and harmonics are reduced but THD is not good enough. In LED driver such as bridgeless boost converter with single inductor and single capacitor as in Pandey [18] harmonics are satisfactory but switching losses are higher. Harmonics are compensated in LED driver in Anwar [19] but complex harmonic compensation unit is added. Low pass filter is installed in LED driver in Karim [20] for harmonic mitigation but the obtained harmonics was 25.3%. Ref. [21] comprises of the method of harmonic injection where third harmonics reduction is not so good. In ref. [22] in single stage PFC LED driver the LED output is not constant as there is no closed loop control of the converter. On the other hand THD reduction process is complex. In the AC LED driver harmonic compensation is not satisfied for low order harmonic currents [23].

This paper proposes a constant current LED driver based on SEPIC where harmonics are reduced by optimization of SEPIC parameters. The SEPIC is chosen for PFC due to some advantages: positive dc output, high-low output level, low switching stress and low output ripple current. SEPIC is also a good Power Factor Corrector. On the other hand, though buck converter operates at lower DC output but it gives poor power factor and buck-boost operates in lower and higher DC output but with negative polarity. The proposed driver also improves efficiency and power factor and it does not need extra component for harmonic reduction. A complete control circuit has also been designed in favour of reduced harmonics with soft start. The proposed constant current LED driver operates with single switch, simple control circuit with reduced complexity and cost. The proposed circuit operates in 100 kHz frequency at global voltage range of 90-270V, so it can be simply used in different geographic location.

This paper is organized in the following order: SEPIC PFC converter in Section 2, Proposed LED driver circuit in 3, Harmonic reduction by SEPIC parameter optimization methodology in 4, Transfer function and feedback control in 5, Results and discussions on prototype are stated in Section 6 and conclusion in Section 7.

2. SEPIC PFC CONVERTER

For an input voltage v_{in} , let V_g is the rectifier output voltage and the inductor current i_{L1} and i_{L2} flows through inductor $L_1$and L_2 respectively. The (1)-(4) are taken from Rui [24] to derive some useful relations in DCM mode (Figure 1).

Input voltage, $v_{in} = V_m Sin\omega t$,

So according to the SEPIC functionality $v_{L1} = v_{L2}$.

The total inductor current.

$$i_L(t) = i_{L1}(t) + i_{L2}(t) \quad (1)$$

The relationship between voltage and current in an inductance is as follows, $\frac{di_{L1}(t)}{dt} = \frac{v_{L1}(t)}{L}$

So, the inductance current changes as.

$$\frac{di_L(t)}{dt} = \frac{v_{L1}(t)}{L_1} + \frac{v_{L2}(t)}{L_2} \quad (2)$$

$$\frac{di_L(t)}{dt} = \frac{L_1 + L_2}{L_1 L_2} v_{L1}(t)$$

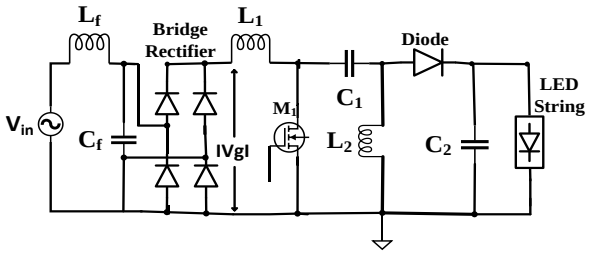


Figure 1. Basic SEPIC with LED load. Input filter (L_f, C_f) is connected before the bridge rectifier followed by the SEPIC

The waveforms of gate voltage driving switch $M1$, inductor voltages v_{L1}, v_{L2}, current flowing through inductance, $i_{L1}(t)$, $i_{L2}(t)$, diode i_D are depicted in Figure 2. The maximum value of inductor current is given as:

$$i_{pk} = \frac{di_L(t)}{dt} DT \; = \; \frac{L_1+L_2}{L_1 L_2} V_g DT \tag{3}$$

From Figure 2 the maximum value of diode current:

$$i_{dpk} = \frac{V_g}{L_{eq}} DT \tag{4}$$

where $L_{eq} = \frac{L_1 L_2}{L_{1+}L_2}$ and D is the duty cycle. Diode conduction time t_d is determined by the volt- sec balance.

$$t_d = D_1 T = \frac{V_g}{V_o} DT \tag{5}$$

$D_2 T$ is the off time of MOS switch. For operating in DCM $T > (t_{on} + t_d)$, where t_{on} is the ON time of the MOS switch M_1 and T is the time period of one switching cycle. Figure 2 shows the voltage and current at different points of the driver. Average of Diode current,

$$I_{Davg} = \frac{1}{2}\frac{1}{T} i_{dpk} t_d \tag{6}$$

Putting the values of $i_{dpk}$and t_d from (4) to (6).

$$I_{Davg} = \frac{DD_1 V_g}{2fL_{eq}} \tag{7}$$

Diode current $I_D = I_{C2} + I_O$, where I_O is the average output current. Since average of $I_{C2} = 0$, we get average of $I_O = I_{Davg}$. So, the average output current is as.

$$I_o = \frac{DD_1 V_g}{2fL_{eq}} \tag{8}$$

If the average output current flows through resistor R.

Average output current $I_O = \frac{V_O}{R}$,

Output voltage: $V_o = \frac{RDD_1 V_g}{2fL_{eq}}$, (9)

and diode conduction time $t_d = \frac{2L_{eq}V_o}{V_g DR}$. (10)

Then the duty cycle can be specified.

$$D = \frac{V_O}{V_g}\sqrt{\frac{2fL_{eq}}{R}} \quad (11)$$

$$D_1 = \sqrt{\frac{2fL_{eq}}{R}} \quad (12)$$

Both MOSFET and Diode Off-time.

$$D_2T = (1 - D - D_1)T \quad (13)$$

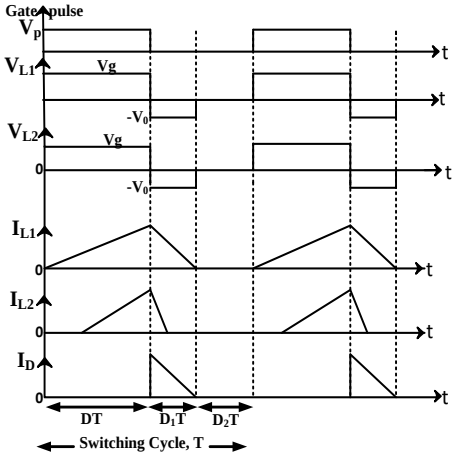


Figure 2. Waveform of gate pulsev_p,inductor voltage v_{L1}, v_{L2},inductor current $i_{L1}, i_{L2}$and diode current i_D

If we assume the power conversion efficiency is 100%, so input power equals the output power.

$$P_{in} = P_{out}$$

$$V_g i_{in}(t) = V_O\, I_O$$

Hence,

$$i_{in}(t) = \frac{V_O\, I_O}{V_g}$$

By putting the values of V_g and I_O we get.

$$I_{in}(t) = \left(\frac{DD_1}{2fL_{eq}}\right)^2 RV_m sin\omega t \quad (14)$$

The (14) shows that in SEPIC DCM input current follows input voltage and it is possible to achieve unity power factor. However, as discussed earlier, for bridge rectifier diode input current wave shape becomes distorted and harmonics is contaminated in the input current. So, harmonics reduction is essential to achieve high power factor.

3. PROPOSED LED DRIVER CIRCUIT

The LED driver circuit consists of single-phase ac voltage source, inductor, capacitor, diode, MOS switch and LED module. The schematic diagram of LED driver circuit is shown in Figure 3. Control circuit design, the control circuit consists of two closed loops control units- outer circuit controls output current by

regulating the output voltage and inner circuit controls input current to improve power factor. Outermost closed loop realizes the current through the LED module and keeps it constant. This current is sensed with a resistor and the corresponding sensed voltage is compared with a fixed reference dc voltage in a voltage error amplifier. Voltage error amplifier is an integrator and generates an error signal. The current generated from it is passed through the current error amplifier as its reference current. Current error amplifier is shown in Figure 4 (a). The inductor current (I_L) is sensed and compared with the reference. Current error amplifier performs proportional and integral function (PI control). It addresses the slow response of voltage error amplifier. It ensures stable operation and makes compensation easier.

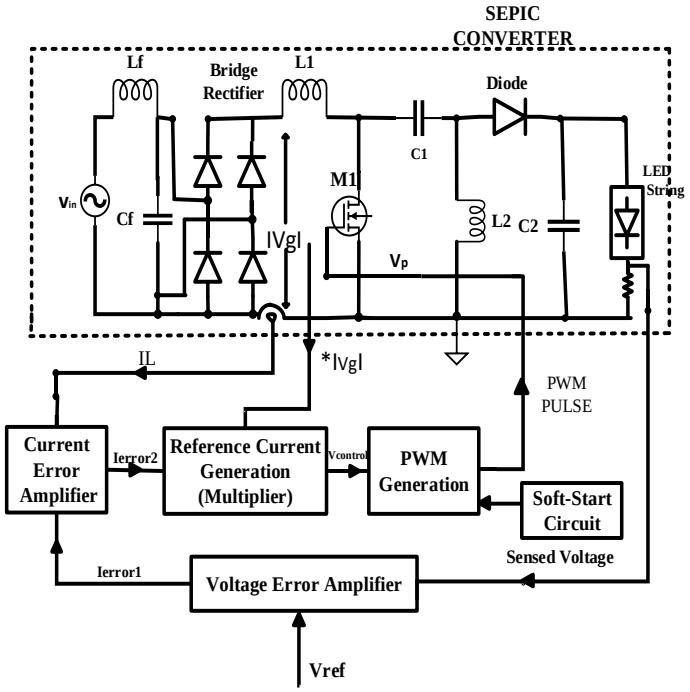


Figure 3. SEPIC Circuit. The outer circuit keeps output current constant and inner circuit controls input current and improves power factor and THD

Gain of the Current error amplifier (Compensator) $G(s) = \frac{-Z_f(s)}{Z_i(s)}$.

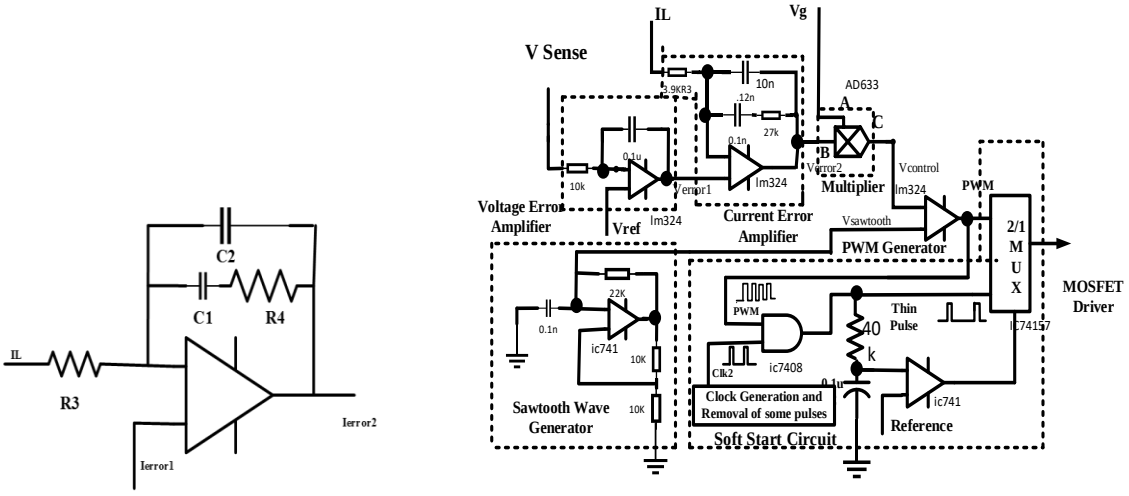
$$Z_i(s) = R_3\,, Z_f(s) = \left(R_4 + \frac{1}{C_1 s}\right) \| \frac{1}{C_2 s} \; and \; G(s) = \frac{-1}{R_3 C_2} \frac{(s + \frac{1}{R_4 C_2})}{s\left(s + \frac{C_1 + C_2}{R_3 C_1 C_2}\right)}$$

Proportional Gain $K_p = \frac{R_4}{R_3}$ and Integral Gain $K_i = \frac{1}{R_3 c_1}$. If K_p increases rise-time decreases, overshoot increases and overshoot error decreases. If K_i increases rise-time decreases, overshoot increases, settling time increases, eliminates steady state error. First the parameters of the compensator are optimized by the simulation of LED driver (Main circuit +control circuit). By using the circuit parameter, the transfer function has been determined. The following steps are taken to choose gain in order to get the desired response, i) obtaining the open loop response and determine what needs to be improved, ii) adding proportional control to improve rise time, iii) adding integral control to eliminate the steady state error and, iv) adjustment K_p and K_i by changing circuit parameters until obtaining a desired overall response. If stability is bad and gain is needed to change to meet stability criterion the above procedure will be repeated. Finally, the stability has been determined by (i) step response and (ii) root-locus method explained in Section 5.

In DCM though power factor is high, the input current harmonics is high. Bridge rectifier draws distorted current from input AC and causes high THD, very low PF and very low efficiency to the LED

module. In order to reduce harmonics in the input current, multiplier is used in the control circuit. It eliminates the distortion in input current wave shape by multiplying the output of current error amplifier with replica of the input ac voltage. The output signal of multiplier is naturally synchronized and symmetric to the input AC voltage, which is the condition to achieve unity power factor with reduced harmonics. Then PWM pulses are generated by comparing a saw-tooth wave with the reference produced by the multiplier. The details control circuit is shown in Figure 4 (b). The function of the soft start circuit is to prevent sudden rise of input current and overshoot of voltage in the starting period to prevent damage. Pulse thinning mechanism is used to remove some pulses from a clock pulse and generates thin pulse. In the soft start circuit, clock pulse is generated by using A stable multivibrator. The output of the multivibrator is clamped to get only positive pulse. Clk2 is obtained from clock pulse generator after removing some pulses' waveform is generated from control circuit. Clk2 and PWM are the inputs of AND gate and thinner pulse is obtained from the output. This thinner pulse is fed directly to the MOSFET through MUX at the onset of starting. The selector of 2-1 MUX determines starting period and normal operation. In normal operation regular PWM pulses are fed to the MOS gate.

It is to be noted that all wave forms required in the driver is generated internally and no external source is needed in the drive circuit. In the designed LED driver, the voltage error amplifier uses single Op-amp for both comparison and amplification purposes. Similarly, the current error amplifier uses a single Op-amp for comparison and PI controlling purposes. The function of sawtooth wave is obtained from square wave generator by using single Op-Amp only. Thus, the number of components in the control circuit is reduced. The overall control circuit is used to improve the step response and increase the stability of the circuit. It also plays the role in reducing THD and improving power factor.



(a) (b)

Figure 4. (a) current error amplifier (PI controller), (b) the details control circuit with soft start

4. HARMONICS REDUCTION BY SEPIC PARAMETER OPTIMIZATION METHODOLOGY

LEDs are a nonlinear load that generates harmonics. LED driver delivers constant current to LED lamp. In order to get desired DC output from AC input a full bridge rectifier is used before SEPIC. These diode rectifiers cause highly distorted input current and generates harmonicist of the input current is an important factor in LED driver and it should be kept as low as possible. Lower THD in LED driver ensures higher Power Factor, lower peak currents and higher efficiency.

We know that for a sinusoidal source and nonlinear load

$$PowerFactor = Displacement\ Power\ Factor(dpf) \times Distotion\ Factor(df)$$
$$P.F = dpf \times df = cos\theta \times I_{1rms}/I_{rms} \quad (15)$$

I_{1rms} is the RMS value of input current of fundamental frequency and I_{rms} is the RMS value of total component of input current frequency. According to (14) for the LED driver operating in discontinuous

mode, $dpf = cos\theta = 1$ But in practical circuit due to bridge rectifier and MOS switch unity power factor cannot be achieved. So, control circuit is required to improve the power factor.

$$\text{Now, } P.F = df = \frac{I_{1rms}}{I_{rms}} = \frac{1}{\sqrt{1+THD^2}} \quad (16)$$

The (16) if the RMS value of input current of fundamental frequency is higher, distortion factor becomes higher and THD becomes lower. Theoretically, if $THD = 0$, distortion factor will be 1 as from (16), and

$$I_{1rms} = I_{rms} \quad (17)$$

This is possible only when the converter parameters are optimized to make input current distortion to zero and to make the input current in phase with input voltage to impose the circuit behavior as a resistive load.

But practically in order to reduce harmonics in the input current the input inductance(L_1), output inductance (L_2) and input capacitance(C_1) are required to be optimized [25]. Output capacitor (C_2) is required to optimize to reduce output voltage and current ripple. This harmonic compensation and power factor improvement can be done by optimizing SEPIC parameters by the following methodology for nonlinear load LEDs along with properly designed feedback circuit.

4.1. SEPIC parameter optimization methodology

Harmonics arises in the input current for bridge rectifier diode, switch, and nonlinearity of LEDs. The factors that effect on harmonics in the input current are the value of inductor L_1, capacitor C_1, energy transfer between capacitor C_1 and inductor L_2. Output current ripple depends on the filter capacitor C_2.

4.1.1. THD reduction

a. Fixing the value of input Inductor L_1

The relationship between input inductor L_1 and input ripple current $\triangle I_{L1}$.

$$L_1 = \frac{V_{in}.D}{\triangle I_{L1}.f_s} \text{ ; where } f_s \text{ switching frequency} \quad (18)$$

Input inductor current ripple $\triangle I_{L1}$ can be reduced by using greater value of L_1, otherwise harmonics will be high.

b. Fixing of output inductor $\boldsymbol{L_2}$

The voltage conversion ratio M can be obtained by applying the Power-balance principle [26]: $M = \frac{V_O}{\sqrt{2}V_{in}} = \frac{D_1}{\sqrt{2K_e}}$ where conduction parameter $K_e = \frac{2L_{eq}}{R_o T_s}$; here $L_{eq}$is the equivalent inductance of $L_1$and L_2 in parallel and R_o is the dynamic resistance of LED load, For DCM operation, $D_1 < 1 - D$
Thus, the value of $K_{e-critical}$can be evaluated [28] by:

$$K_e < K_{e-critical} = \frac{1}{2(M+2)^2} \quad (19)$$

For DCM operation $K_e$should be $K_e = 0.85\ K_{e-critical}$.
Thus, by evaluating K_e an equivalent inductance $L_{eq}$is obtained as (20).

$$L_{eq} = \frac{K_e R_o}{2\ f_s} \quad (20)$$

The value of L_2can be expressed as (21).

$$L_2 = \frac{2L_1 L_{eq}}{L_1 - L_{eq}} \quad (21)$$

c. Fixing Input capacitor $\boldsymbol{C_1}$

C_1has a significant influence in the input current wave shaping. The value of C_1[27] will be such that $f_L < f_r < f_s$, where f_L, $f_r\ are$ line current and resonance frequency respectively.

$$f_r = \frac{1}{2\pi\sqrt{C_1(L_1+L_2)}} \quad (22)$$

L_1, L_2 and C_1should be optimized for THD reduction. Without optimization harmonics in the input current becomes high. The simulated plot in Figure 5 (a). is obtained without optimization of C_1 but $L_1$and L_2 optimized. Here $C_1 = 0.05uF, L_1 = 10mH\ and\ L_2 = 36.24uH$. It shows $P.F.$=0.76, $THD = 64.89\%$ and hence P.F. and THD are not satisfactory. It is found that the effect of C_1 is dominating in the input current THD.

After optimization of C_1, THD is significantly reduced but still high which is shown in Figure 5 (b). In this simulation L_1 is not optimized but $C_1 and\ L_2$ are optimized. L_1 has less influence in harmonic minimization than C_1. Here, $L_1 = 5.0mH, L_2 = 36.24\mu$H, $C_1 = 0.01\mu F$ and we obtained $P.F. = 0.885$, $THD = 24.58\%$.

Capacitor C_1 is fundamental in obtaining a high-quality input current. L_2has comparatively less effect on THD. Without optimization of L_2 and C_1, the energy of L_2 will not be properly transferred to the load and this un-transferred energy will be transmitted to the source, as a result harmonic will be contaminated in the input current. Again, current ripple of input inductor(L_1) also effect the THD and it can be reduced by increasing L_1 as discussed before. By using the (18), (21), (22) $L_1, L_2\ and\ C_1$ are optimized as $L_1 = 10mH$, $L_2 = 36.24\mu H$ and $C_1 = 0.01\mu F$.Simulated output of the optimized result is shown in Figure 5 (c). After optimization we obtained $P.F. = 0.98$ and $THD = 3.7\%$. The results are satisfactory.

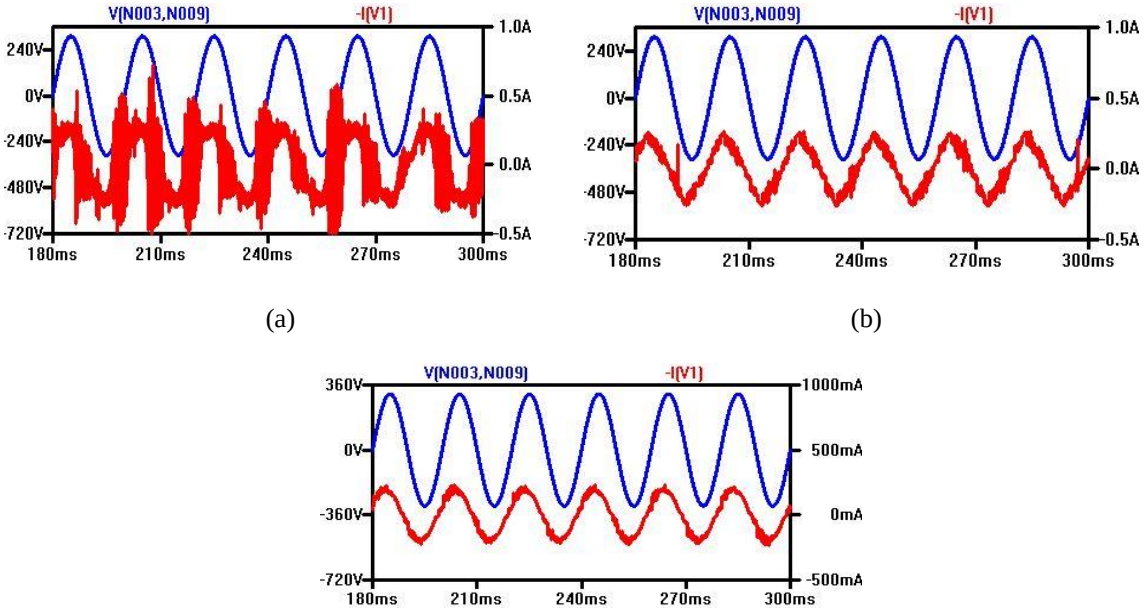


Figure 5. (a) Simulated plot of input voltage, input current without optimization. Here, power factor = $0.76, THD$ 64.89%when $L_1 10mH, L_2$ =$36.24uH, C_1 = 0.05uF$. (b) Simulation of input voltage, input current with PF= 0.885 and THD = 24.58% when $L_1 = 5.0mH$, $L_2 = 36.24\mu$H and $C_1 = 0.01\mu F$. (c) Simulation of input voltage and input current when L_1, L_2 andC_1 are optimized and we obtained $P.F. = 0.98$ and $THD = 3.7\%$ when $L_1 = 10mH$, $L_2 = 36.24\mu$H and $C_1 = 0.01\mu F$.

4.1.2. Reduction of output voltage and current ripple

Fixing output capacitor C_2, according to the (23) relationship, C_2 can be obtained for the desired ripple value of output voltage (ΔV_{CO}).

$$C_2 \geq \frac{I_{output}}{2\omega \Delta V_{CO}} \quad (23)$$

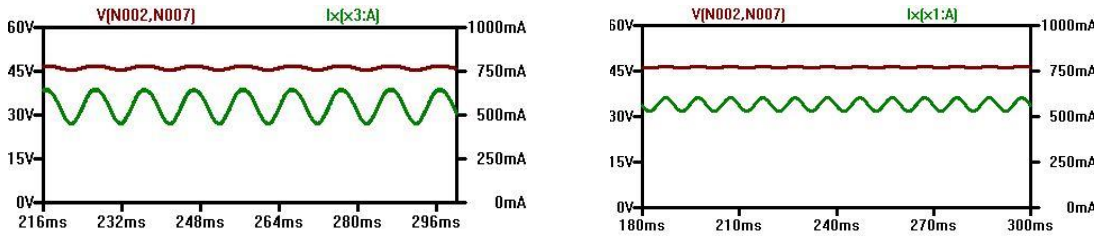
If capacitor current is i_c and capacitor voltage ripple is$\Delta\ v_c$ then

$$\Delta\ v_c = \frac{1}{C_2}\int i_c dt \quad (24)$$

By proper choice of C_2 output voltage and current ripple can be made low as required from (24). For high frequency capacitive impedance ($X_c = \frac{1}{2\pi fc}$) is low, so the AC part will flow through the output capacitor. A ripple voltage is produced at the output. This ripple of output voltage needs to be sufficiently low so as output current does not flicker. From the (23) and (24), the large the capacitor, the better it reduces the ripple. The simulation of output voltage and current before and after optimization of C_2 are shown in Figure 6. After optimization LED voltage and current becomes smoother. Thus, a high-performance LED driver can be designed by optimization of SEPIC parameters along with a well-designed feedback control circuit.

Table1 shows the simulated data of optimization of SEPIC parameters (L_2, C_1), for harmonic reduction. From the data in Table 1 and simulation result, it is found that the input capacitor C_1 plays the main role of transferring energy from input port to output port and via output inductor L_2 . C_1 must be a low valued capacitance. The energy of $L_2$and C_1 must be reimbursement to each other. Input current ripple mainly depends on Inductor L_1 so it also plays a vital role in harmonics reduction. C_2 is filter capacitor and it smooths the output.

The total power loss shown in simulation is 6.2%, Efficiency is 93.78%, THD 3.7% at 220V. The Simulated Power losses are shown component wise in Figure 7. Here Divider is the resistance used to take replica of input voltage to the Multiplier and R-diode and S-diode denote rectifier diode and SEPIC diode respectively. It is seen that the largest power loss occurs in MOS Switch(2%), slightly above 1% is in divider resistance, below 1% in rectifier diode and then in SEPIC diode and least power loss occurs for biasing.



(a) (b)

Figure 6. (a). Simulation of output voltage, output current when $L_1 = 10mH$, $L_2 = 36.24\mu H$ and $C_1 = 0.01\mu F$ (b) without optimization of C_2 (when $C_2 = 1mF$) and (ii) after optimization of C_2 (when $C_2 = 3mF$)

Table1. Optimization of SEPIC parameters for harmonic reduction

Input Inductor $L_1(mH)$	Output inductor $L_2(\mu$H)	Input Capacitor $C_1(\mu$F)	THD (%)	Power Factor	Efficiency (%)
10.0	100.0	0.01	10.49	0.918	94.12
10.0	10.0	0.01	13.37	0.926	89.2
10.0	36.4	0.01	3.70	0.923	95.0 Optimized
5.0	36.4	0.01	24.85	0.885	92.24
10.0	36.4	0.05	64.89	0.760	78.49
10.0	36.4	0.005	15.43	0.887	93.89
2.0	300.0	0.01	32.32	0.863	95.47
1.8	36.4	0.01	99.81	0.63	96.76

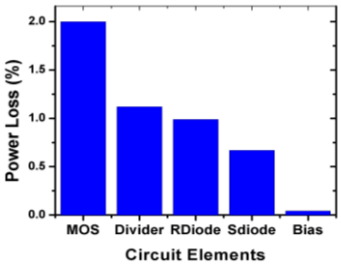


Figure 7. Major power loss components of the LED driver found in simulation

5. TRANSFERFUNCTION AND FEEDBACK CONTROL

The power stage (SEPIC) of closed loop system is nonlinear system. Nonlinear system is usually difficult to model and it is also difficult to predict the system behavior. So, it is better to approximate nonlinear system to linear system. For this state space averaging technique is used to describe SEPIC using a system of linear differential equations. Differential equations of SEPIC and average matrices are given in section 5.1. in the paper. Details Operating point is not discussed here as it is a well-known phenomenon.

5.1. State space equations

The state space equations for SEPIC during three switching states in DCM as shown in Figure 8.

for state A: $\mathbf{0 < t < DT}$

$$\dot{X} = A_1 X + B_1 v_{in}(t)$$
$$Y = C_1 X + E_1 v_{in}(t) \quad (25)$$

for state B: $\boldsymbol{DT < t < D_1 T}$

$$\dot{X} = A_2 X + B_2 v_{in}(t)$$
$$Y = C_2 X + E_2 v_{in}(t) \quad (26)$$

for state C: $\boldsymbol{D_1 T < t < D_2 T}$

$$\dot{X} = A_3 X + B_3 v_{in}(t)$$
$$Y = C_3 X + E_3 v_{in}(t) \quad (27)$$

where the rectified input voltage is $v_{in}(t)$ and $\dot{X} = \frac{dx}{dt}$ and the state vector is defined as (28).

$$X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} \quad (28)$$

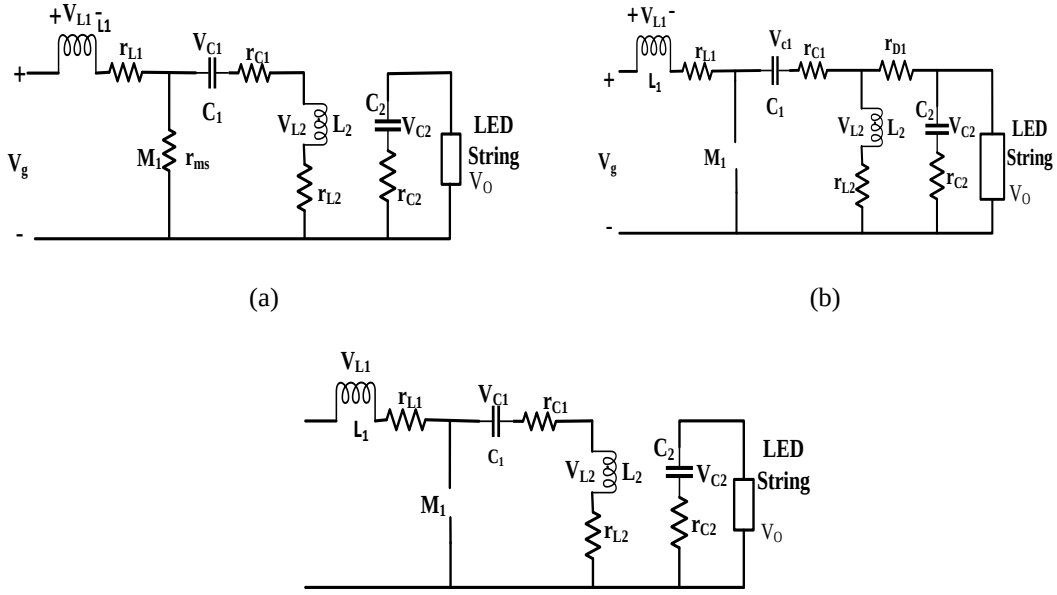


Figure 8 (a). SEPIC circuit when M_1 is ON, Diode is OFF, (b) when M_1 is OFF, Diode is ON, (c) SEPIC circuit when M_1 is OFF, Diode is OFF

The output vector $Y = v_0$. The averaged matrices for the steady-state and linear small-signal state-space equations can be written as $A = A_1D + A_2D_1 + A_3D_2$ and $B = B_1D + B_2D_1 + B_3D_2$. From the equivalent circuit the matrices $A_1, A_2, A_3, B_1, B_2, B_3$ and more are as (29) to (33).

$$A_1 = \begin{bmatrix} -\frac{(r_{L1}+r_{ms})}{L_1} & -\frac{r_{ms}}{L_1} & 0 & 0 \\ \frac{r_{ms}}{L_2} & \frac{(r_{L2}+r_{C1})i_{L2}}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{c_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{c_2(r_{c2}+R_O)} \end{bmatrix} \quad (29)$$

$$A_2 = \begin{bmatrix} -\frac{R_E}{L_1} & -\frac{R_E}{L_1} & -\frac{1}{L_1} & -\frac{R_E}{r_{c2}L_1} \\ -\frac{R_E}{L_2}+r_d & -\frac{R_E}{L_2}+r_d & 0 & -\frac{R_E}{r_{c2}L_2} \\ -\frac{1}{c_1} & 0 & 0 & 0 \\ \frac{R_E}{c_2r_{c2}} & \frac{R_E}{c_2r_{c2}} & 0 & \frac{R_E}{c_2r_{c2}} \end{bmatrix} \quad (30)$$

$$A_3 = \begin{bmatrix} -\frac{(r_{L1}+r_{L2}+r_{C1})}{L_1+L_2} & 0 & -\frac{1}{L_1+L_2} & 0 \\ 0 & -\frac{(r_{L1}+r_{L2}+r_{C1})}{L_1+L_2} & \frac{1}{L_1+L_2} & 0 \\ \frac{1}{c_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{c_2(r_{c2}+R_0)} \end{bmatrix} \quad (31)$$

$$B = B_1 = B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (32)$$

$$B_3 = \begin{bmatrix} \frac{1}{L_1+L_2} \\ -\frac{1}{L_1+L_2} \\ 0 \\ 0 \end{bmatrix} \quad (33)$$

$$C_1 = \begin{bmatrix} 0 & 0 & 0 & \frac{R_E}{r_{c2}} \end{bmatrix} \quad (34)$$

$$C_2 = [R_E \quad R_E \quad 0 \quad R_E] \quad (35)$$

$$C_3 = \begin{bmatrix} 0 & 0 & 0 & \frac{R_E}{r_{c2}} \end{bmatrix} \quad (36)$$

$$E_1 = E_2 = E_3 \quad (37)$$

5.2. Transfer function of SEPIC with feedback control

The power stage output transfer function of the SEPIC converter is obtained by solving the state space (38) and output to input transfer function is obtained as (39).

$$G_{dv}(s) = \frac{12.94s^3 - 0.07303s^2 - 5.503e^{-6}s + 7.187e^{-15}}{s^4 + .005621s^3 + 1.197e^{-6}s^2 + 9.625e^{-14}s + 4.772e^{-18}} \quad (38)$$

$$G_{vv}(s) = \frac{0.01897s^3 + 1.412e^{-6}s^2 + 5.424e^{-14}s + 1.427e^{-18}}{s^4 + .005621s^3 + 1.197e^{-6}s^2 + 9.625e^{-14}s + 4.772e^{-18}} \quad (39)$$

The open loop transfer function of the whole system can be defined.

$$T(s) = G_{cA}(s)G_{dv}F_r \quad (40)$$

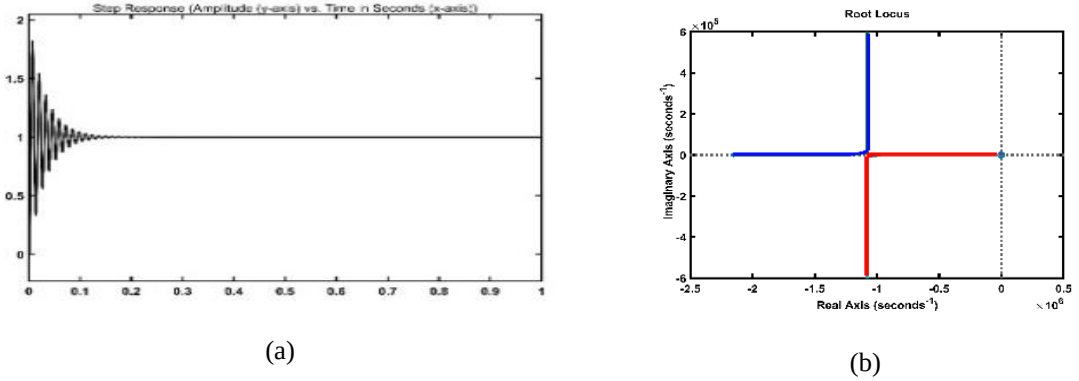
F_r is the transfer function of without parameters of the compensator have been optimized for stable operation of the designed LED driver. The transfer function of the compensator of the designed LED driver is obtained.

$$G_{CA} = \frac{2.137e^6 s + 7.907e^9}{s^2 + 2.16e^6 s} \quad (41)$$

The overall open loop transfer function for the system with compensator is found from (40).

$$T_{comp} = \frac{2.7656e^7 s^4 + 1.023e^{11} s^3 - 5.777s^2 - 4.353e^4 s + 5.685e^{-5}}{s^6 + 2.16e^6 s^5 + 1.224e^4 s^4 + 2.586s^3 + 2.079e^{-7} s^2 + 1.031e^{-11} s} \quad (42)$$

From step response Figure 9 (a) it is found that for compensated model the system reaches to steady state within only 0.2 seconds. From Figure 9 (b) the root locus of the SEPIC converter indicates stable operation of the compensated system.



(a) (b)

Figure 9. (a) step response of SEPIC Converter with compensator (steady-state achieves in 0.2 seconds), (b) Root locus with compensator (no zero found in RHS of imaginary axis)

6. RESULTS AND DISCUSSION ON PROTOTYPE

A prototype of the proposed LED driver is built to obtain the best execution of the driver circuit. Major objective is to reduce harmonics in the input current with the constant output current and to maintain good power quality. The LED Driver is designed for fifteen LEDs connected in series. Each LED is of 0.5W power rating. Voltage drop of 15 LEDs are about 45 volts for optimum operation as voltage drop of each LED is about 3 volts. This is another salient feature of our designed LED driver that it works at constant LED load by keeping output voltage and current constant with the variation of input voltage from 90V to 270V. So, Load disturbance rejection is not applicable. When input voltage changes, inductor current also changes. The amplitude of inductor current controls two loops of control circuit. This change of Inductor current makes change in output voltage. By realizing the change of output voltage, voltage feedback control signal changes. The inductor current and the feedback control signal altogether act to regulate the output dc voltage to the preselected value. Thus, the control circuit functions in such a way that it completely absorbs input disturbance, no input disturbance rejection is needed.

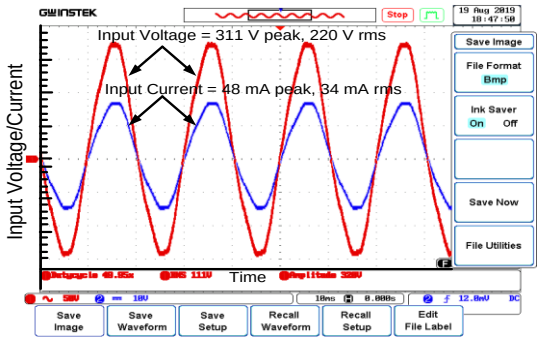
To enhance power quality i.e., to reduce harmonics in the input current optimization of inductor L_2 and capacitor $C_1$are to perform according to (21) and (22). Output capacitor $C_2$is also optimized according to (24) to reduce the output current ripple. L_1 is optimized according to (18) to get desired input current ripple. No extra component is used in the LED driver power circuit. From the measured value it is clear that after optimization THD has been reduced significantly. Multiplier is used in the control circuit to get a low harmonic with high power factor. After rectifier no filter capacitor is used.

Table 2 shows the parameter values of SEPIC and basic specification of the converter. Figure 10 (a) shows measured input voltage (v_s), input current (i_s), at $V_S = 220V$ with 15 LED in the string in steady-state condition. Obtained $THD = 3.35\%, P.F. = 0.98$. when all SEPIC parameters optimized. The result is

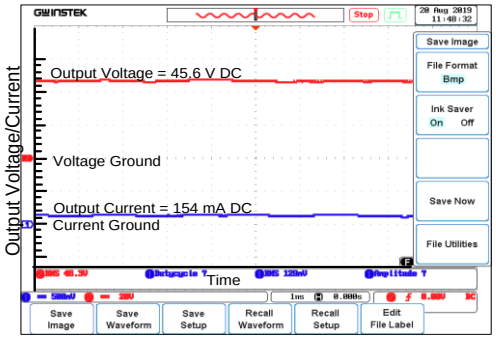
satisfactory. The measured LED voltage and LED current are constant at $45.6V$ and $154mA$ respectively as shown in Figure 10 (b). The result is also satisfactory.

Table 2. Optimized parameters used in simulated and prototype

Parameters	Values
Input inductor,L_1	$10\ mH$
Output inductor,L_2,	$36.24\ uF$
Input capacitor,C_1	$0.01\ uF/600V$
Output capacitor,C_2	$1.0\ mF/63V$
Duty Cycle,D_{max}	0.19
Power Diode	$1000V/10A$
MOS Switch, M_1	$2sk1101-01MR(450V/10A)$
Operating Voltage	$220\ volts$
Switching frequency,f_s	$100\ kHz$
Inductor Current Ripple,$\triangle\ I_{L1}$	$65\ mA$



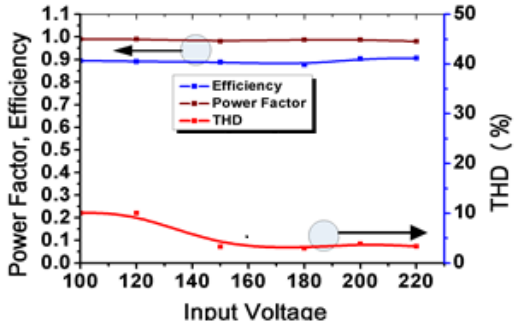
(a)



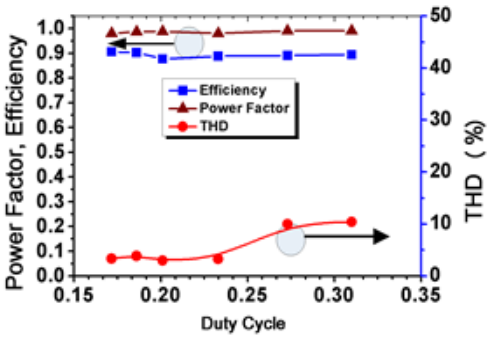
(b)

Figure 10. (a). The measured input voltage $220V$ rms ($50V/Division$) and input current $34mA$ rms ($30mA/Division$). $THD = 3.35\%, P.F. = 0.98$. (b). The measured output voltage ($20V/Division$) and current ($500mAV/Division$) at $220V$ ac input

The measured data shows that the designed LED driver consumes 7.745 watt including dc bias at an input voltage of $220V$ rms and produces an output of 7.0224 Watts. Hence it has measured an efficiency of 90.67% and power loss is 9.33% at power factor= $0.98, THD = 3.35\%$. As we have seen from simulated result in Figure 6 the highest power is consumed in the MOS switch. Figure 11 (a) and Figure 11 (b) shows the power factor and efficiency remains almost constant with increase of input voltage and duty cycle. However, THD decreases with increasing input voltage but increases with increase of duty cycle.



(a)



(b)

Figure 11. (a) measured power factor, efficiency, and THD vs. input voltage and (b) measured power factor, efficiency and THD versus duty cycle

Table 3 shows the performance parameters of the proposed LED Driver as obtained in experiment. We know that it is hard to obtain high PF and high efficiency simultaneously and there is a trade-off between the two. The proposed LED driver shows high PF and relatively high efficiency with constant LED driving current achieved by optimization of SEPIC parameters and well-designed feedback control circuit.

Table 3. The measured parameters of the proposed LED drivers

V_S (V)	I_S (mA)	V_0 (V)	I_O (mA)	DC Bias (W)	PF	THD (%)	CF	Efficiency
100	72	45.0	150	0.415	0.990	10.4	1.41	0.894
120	60	45.1	149	0.415	0.990	10.0	1.40	0.891
150	51	45.6	154	0.415	0.980	3.26	1.39	0.888
180	42	45.5	152	0.415	0.988	2.95	1.41	0.877
200	37	45.6	153	0.415	0.987	3.85	1.41	0.903
220	34	45.6	154	0.415	0.980	3.35	1.40	0.906

Table 4 shows comparisons with LED driver presented in [28], [29] and the proposed one. The proposed LED Driver shows the feature of better input current THD compared to [29] and it offers a smaller number of components with same efficiency compared to ref. [28]. The prototype of LED driver is shown in Figure 12.

Table 4. Comparison of designed LED driver with similar work

Item	LED driver in [28]	LED driver in [29]	Designed LED driver
Circuit stage	Single stage	Single	Integrated
Input Voltage Range	85-265 V	90-130 V	90-270 V
Power Switches	3	2	1
Diodes	7	4	5
Capacitors	3	3	2
Inductors	2	2	3
Transformer	1	1	Not needed
Power Factor	0.994(110V)	0.994 (115V)	0.98(220V)
THD	3.31%	7.27%	3.35%
Efficiency	90.96%	93.05%	90.6%

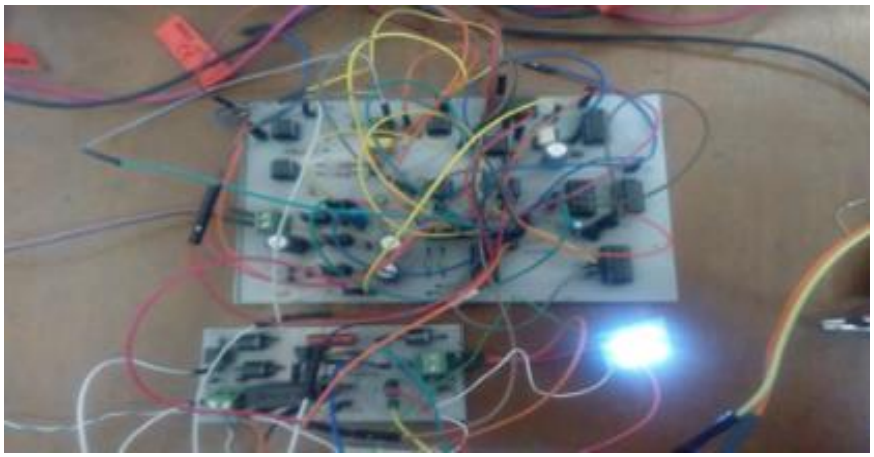


Figure 12. Prototype of LED driver

7. CONCLUSION

In this paper, a high performance SEPIC based LED driver has been designed and a prototype has been built and evaluated. Parametric optimization of SEPIC inductors and capacitors are performed with the design of a double loop feedback control circuit of LED driver. The LED driver maintains around 150mA LED current in universal voltage range 90-270 Volts with 90.6% efficiency, 0.98 power factor and 3.35% harmonics in the input current with a simple control circuit and reduced number of components. These advantages are desirable in residential as well as commercial lighting.

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