International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 12, No. 1, Mar 2021, pp. 121~129
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v12.i1.pp121-129

A fast and robust reference current generation algorithm for three-phase shunt active power filter

Zakaria Chedjara[1], Ahmed Massoum[2], Patrice Wira[3], Ahmed Safa[4], Abdelmadjid Gouichiche[5]
[1,2]Laboratoire ICEPS, Université Djilali Liabes Sidi Bel Abbes, Algérie
[3]Laboratoire IRIMAS Université de Haute alsace, 4 rue des frères lumière, Mulhouse cedex, France
[4,5]Laboratoire LGEP, Université Ibn khaldoun, Tiaret, Algérie

Article Info

Article history:

Received Jun 01, 2020
Revised Jan 6, 2021
Accepted 3 Feb, 2021

Keywords:

Artificial neural network
Shunt active power filter
Synchronization

ABSTRACT

The identification of the reference currents constitutes an important part of the control of the active power filter. This part requires an accurate estimation of the frequency, phase, and proper extraction of the load current harmonics. This makes the modeling more difficult and requests a rigorous selection of techniques to be used. For the sake of simplicity, the direct method is motivated by the need for the simplicity and flexibility than the existing techniques such as the instantaneous power theory and diphase currents method. However, this method requires a robust phase-locked loop to extract the unity voltages and a robust controller to estimate the magnitude of the source current. To this end, this paper proposes the hybrid phase-locked loop (HPLL) as a good option mainly because 1) it achieves zero phase error under frequency drifts, 2) Fast dynamic response, 3) totally block the DC offset, 4) From the control point of view, it is a type 1 control system which results in high stability margin. To the best of authors' knowledge, the HPLL has not been used in active power filter yet. Furthermore, a neural PI regulator is used to estimate the magnitude of the source current. Simulation results show the efficiency of the proposed technique and illustrate all its interesting features. For the sake of comparison, the proposed method is compared to other advanced techniques.

Corresponding Author:

Zakaria Chedjara
Laboratoire ICEPS
Université Djilali Liabes sidi Bel Abbes, Algérie
Email: zakaria.chedjara@gmail.com

1. INTRODUCTION

The increasing penetration of distributed generation (DG) sources into the power grid and the proliferation of domestic non-linear loads have posed serious power quality problems and made the mitigation task more difficult than before [1]-[8].

Shunt active power filters (SAPF) in low-voltage electrical networks remains one of the most studied and developed compensation methods. However, the shunt active power filter remains a complex strategy that needs a thorough and careful study to perform well. Each part in the SAPF control algorithm performs a very precise task and depends heavily on the performance of the other parts. This dependence makes the modeling more difficult and requests a rigorous selection of techniques to be used as shown I Figure 1.

The identification of the current references constitutes an important part of the control of active power filter. This part requires an accurate estimation of the frequency, phase, and proper extraction of the load current harmonics. To this end, many identifications have been reported in the literature [9]-[22]; they

can have categorized into the time domain and frequency domain approaches. The frequency domain such as the discrete Fourier transform (DFT) and recursive DFT [20], the nonlinear least square [21]. However, these techniques require a computational demanding, and its estimation accuracy is affected by the choice of sampling frequency and window length, the time-domain techniques such as the instantaneous power theory (IPT) [4], the diphase current method (DQ) and the direct [2], [22].

All these techniques, regardless of their structure differences, operate satisfactorily under an ideal condition, in which the grid voltage is free of any noise. However, this situation almost never occurs in practice due to more and more frequent power quality problems (presence of harmonics, interharmonics, DC offset and asymmetrical voltage drops).

The most widely used technique is the phase-locked loop (PLL), the conventional types suffer from three critical limitations: 1) only an approximation but not a true amplitude and phase angle of the positive sequence component are detected; 2) the detected positive sequence voltages are distorted and unbalanced; 3) the dynamic response of the system is significantly affected [23].

To deal with this problem, some efforts for designing more efficient PLLs methods have been made recently. A review of recent advances is given in [23]. These efforts improve the filtering capability and disturbance rejection ability of PLLs by including different filters, the moving average filter (MAF), the Delayed Signal Cancelation operator (DSC), Second-Order Generalized Integrator (DSOGI) and others. These techniques suffer from one or more on the following shortcomings: 1) slow dynamic response, 2) inefficiency under large frequency drifts and highly distorted source voltage, 3) are less attractive to deal with the DC-offset problem, 4) require a deep stability analysis.

Furthermore, the IPT and DQ require a low-pass or high-pass filter to extract the fundamental or the harmonic components. However, these kinds of filters must be designed carefully in order to avoid erroneous compensation reference signals during the SAPF operation. For the sake of simplicity, the direct method requires fewer calculations (does not necessitate pre-processing, such as high-pass and low-pass filtering, in order to separate the fundamental and the harmonic components) than IPT, DQ and ensures better accuracy and robustness.

To address these issues, this paper proposes the hybrid synchronous/ stationary filtering technique (HPLL) with the direct method [24] as good option mainly because, 1) it achieves zero phase error under frequency drifts, 2) Fast dynamic response, 3) totally block the DC offset, 4) From the control point of view, it is a type 1 control system which results in high stability margin. To the best of authors' knowledge, the HPLL has not been used in active power filter yet. Besides, a neural regulator to enhance the dynamic of the DC bus voltage.

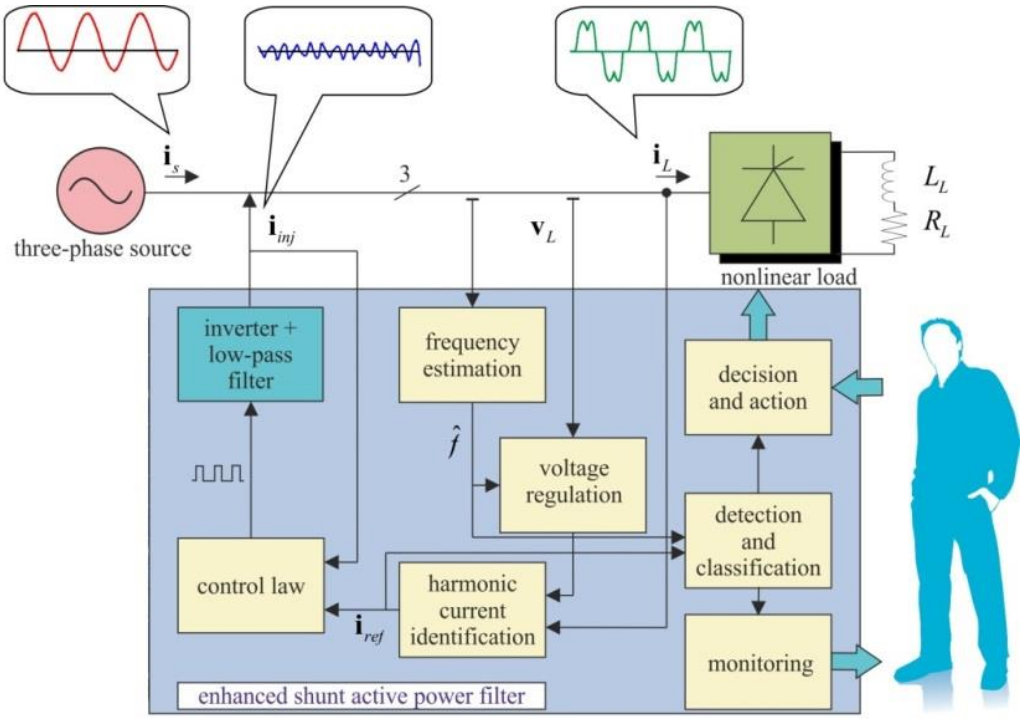

Figure 1. Shunt active power filter control

2. REFERENCE CURRENT GENERATION USING THE DIRECT METHOD

In this work, the direct method has been adopted as shown in Figure 2 [2]. There are three blocks for this control strategy. The first block estimates the maximum currents of the source using a proportional integrator (PI) with a neural approach. These currents take care of the active power required by the active filter and the losses generated in the inverter. Instantaneous reference source currents are evaluated by multiplying the estimated maximum currents by the unit voltage vectors. The second block determines the reference currents of the filter which are obtained by subtracting from the reference source currents, the instantaneous load currents and compared to the currents of the filter. The third block gives the errors which are used through a PWM (pulse width modulation) to generate control signals for the active filter.

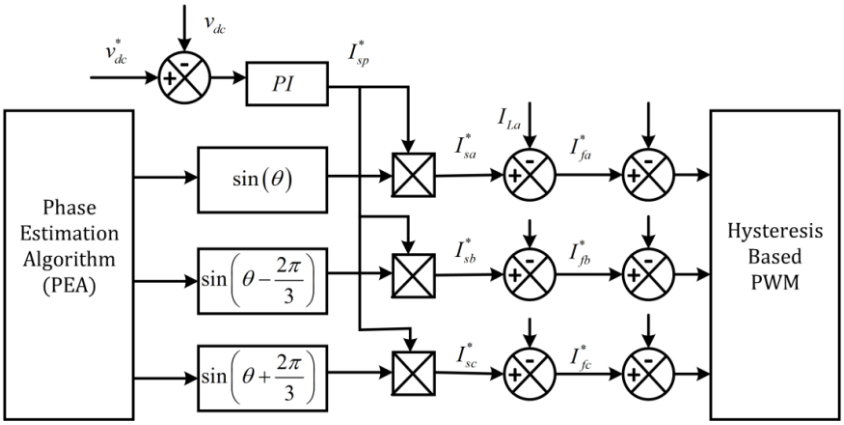

Figure 2. Identification structure of reference currents with the direct method

2.1. Problem formulation

With the direct method, the identification of the reference currents depends on the phase estimation algorithm. A phase-locked loop is the most widely used technique to recover a balanced system.Figure 2 illustrates the conventional SRF-PLL (the synchronous reference frame). Since conventional SRF-PLL is the basic structure for implementing almost all advanced PLLs, a brief description of its operating principle and properties is first presented [23].

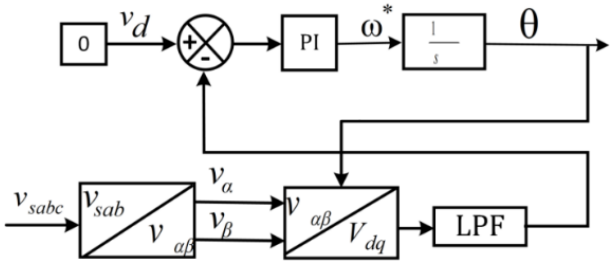

Figure 3. SRF-PLL with LPF

In conventional SRF-PLL, Clarke and Park's transformations are applied to voltage signals to transfer them to the synchronous reference frame (dq). The resulting dq axis signals contain the phase and amplitude error information. The signal containing the phase error, here Vq, passes through the LF, which is an integral proportional regulator (PI). The cooperation of this regulator and the VCO guarantees a zero average phase tracking error at nominal and non-nominal frequencies in steady state. Note that the unit vector generated by the VCO [i.e., sin and cos] is used by the PD (park transformation) to generate the phase and amplitude error information. Also note that the PI controller output and the d-axis signals are estimates of the frequency and magnitude of the grid voltage, respectively. The d-axis signal is transmitted to a low-pass filter in order to reject/attenuate the possible disturbances and accurately estimate the magnitude of the grid voltage. According to the ref, the transfer function of SRF-PLL with additional LPF is (1):

$$\frac{\hat{V}_{\alpha\beta}^{+}}{V_{\alpha\beta}} = \frac{k}{(s - j\omega_c) + k} \tag{1}$$

Figure 4 shows the frequency response of (5) for ω=314 rad/s and three values of k. In these plots, it can be noted that the negative frequency is interpreted as a response to the negative sequence vector signal. The frequency response is asymmetric around the zero and it provides a unit gain with zero-phase shifts at the fundamental frequency of positive sequence, while offering some level of attenuation to the same negative sequence frequency. The dynamic response depends on the parameter k.

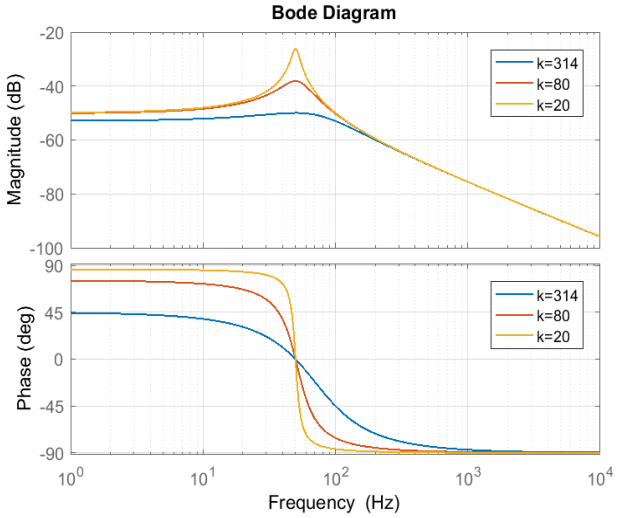

Figure 4. Bode diagram of the. SRF-PLL with LPF

As mentioned before this technique suffers from the following shortcomings:

1) Only an approximation of the detected amplitude and phase of the positive sequence components.
2) Under greatly unbalanced and distorted conditions: The detected fundamental component is unbalanced and distorted.
3) The dynamic response is significantly reduced. These shortcomings are the main motivation behind developing the advanced techniques.

2.2. DC bus voltage

PI regulators generally achieve a good compromise between performance and cost, that is why these kinds of regulators are used in 80% of industrial regulation systems [25]-[30]. Despite this, the determination of the parameters (P, I) is not obvious and fundamentally not optimal. To deal with these challenges, we propose the use of a neural network learning capability to determine these parameters. Figure 5 shows the principle of this technique where an ADALINE with two weights is used: $\omega 0$ as the proportional parameter and $\omega 1$ as an integral parameter. These weights relate the errors e(k) and e(k-1) at time k and k-1 to the output in the linear combination. The error is defined between the reference signal delivered to the regulator and the measured output of the system to be controlled.

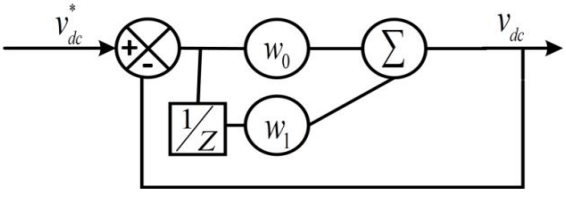

Figure 5. The neural PI regulator

3. THE H-PLL TECHNIQUE

A schematic diagram of this technique is shown in Figure 6. From the control point of view, this technique is a type1 since it characterized by having only one integrator in its control loop and this allows a fast-dynamic response and high stability margin. The key parts of this structure are the MAF in dq space and DSC in αβ space and this is the reason why it referred to the hybrid PLL.

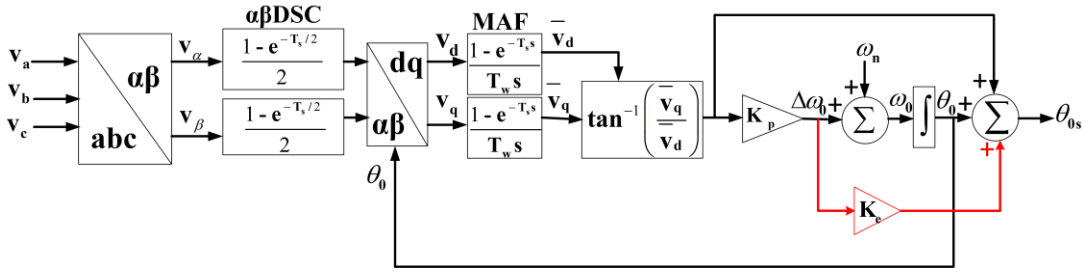

Figure 6. The H-PLL structure

3.1. MAF

A MAF is good alternative to make the SRF immune to the unbalance, harmonic, and DC offset. The MAF described as (2):

$$G_{MAF}(s)=\frac{1-e^{-T_w s}}{T_w s} \tag{2}$$

Where Tw is the length of the MAF window, the MAF passes the DC Component and completely blocks the frequency components of multiple integers from (1/Tw) in hertz. This is the reason why the MAF is sometimes called (quasi-ideal LPF). This selection of Tw is a tradeoff between excellent filtering capability and fast dynamic response. For example, Tw=T removes all harmonics and DC offset but unfortunately, this selection results in slow dynamic response. Besides, to achieve fast dynamic response selecting Tw=T/2. In this case, however, the MAF cannot reject the DC offset [24].

3.2. DSC

To solve this problem, we use the operator (DSC) in the PLL input [24]. DSC is a finite impulse response filter which can be defined in the Laplace domain as

$$\alpha\beta DSC_n(s)=\frac{1+e^{j\frac{2\pi}{n}}e^{-\frac{T}{n}s}}{2} \tag{3}$$

Where n is the delay factor, and it should be determined based on which components are to be removed. According to ref, selecting n=2 to remove the DC component.

4. SIMULATION RESULTS

The proposed algorithm is simulated using Matlab/Simulink. Three scenarios are investigated: ideal source conditions, unbalanced and distorted, DC offset in order to analyze the performance and the effectiveness of the proposed algorithm. Since the MCCF-PLL is mathematically equivalent and perform similarly under different operating conditions to some advanced Type 2 PLLs such as decoupled double SRF (DDSRF), (DSOGI), multiple reference frame PLL (MRF-PLL) and the frequency adaptive discrete filter (FADF) with two stages [30], it has been used as a reference in evaluating the proposed technique.

4.1. Ideal source voltage

This scenario will serve as a reference for two other scenarios. Figure 7 shows the behavior of the active power filter under ideal source voltage condition. Under this condition, the active power filter lowered the THD from 28% to 1.71% with the proposed scheme and 1.89% with the MCCF-PLL. Besides, it can be

seen that, the proposed scheme is fast compared with MCCF-PLL, to be more exact the H-PLL have a settling time about 1 cycle while, the MCCF-PLL have 2 cycles. In addition, the neural regulator enhances the DC bus voltage dynamic.

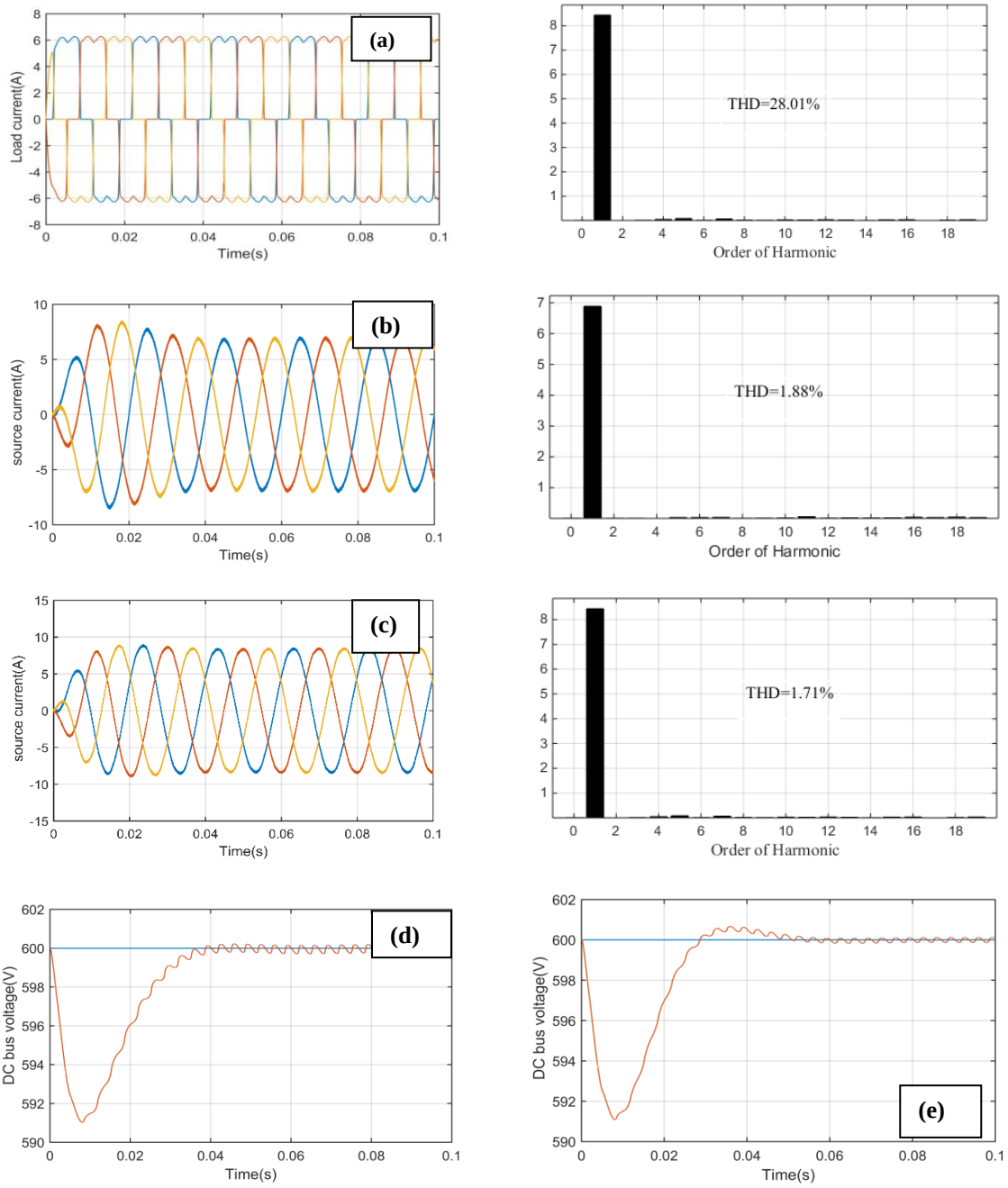

Figure 7. Simulation results under highly unbalanced source voltage: (a) load current and its frequency spectrum, (b) source current and its frequency spectrum with the MCCF-PLL, (c) source current and its frequency spectrum with the H-PLL, (d) DC bus voltage with the neural regulator, (e) DC bus voltage with the classical PI regulator

4.2. DC offset condition

In this scenario, a DC component of phase (a) and phase (c) +50v, -50v is added to the grid voltages. Figure 8 shows the behavior of the active power filter under DC offset condition. Under this condition, the

active power filter had good performances only with the proposed scheme with a source current THD of 1.89%. It can be noted that the proposed algorithm is largely better than the MCCF-PLL.

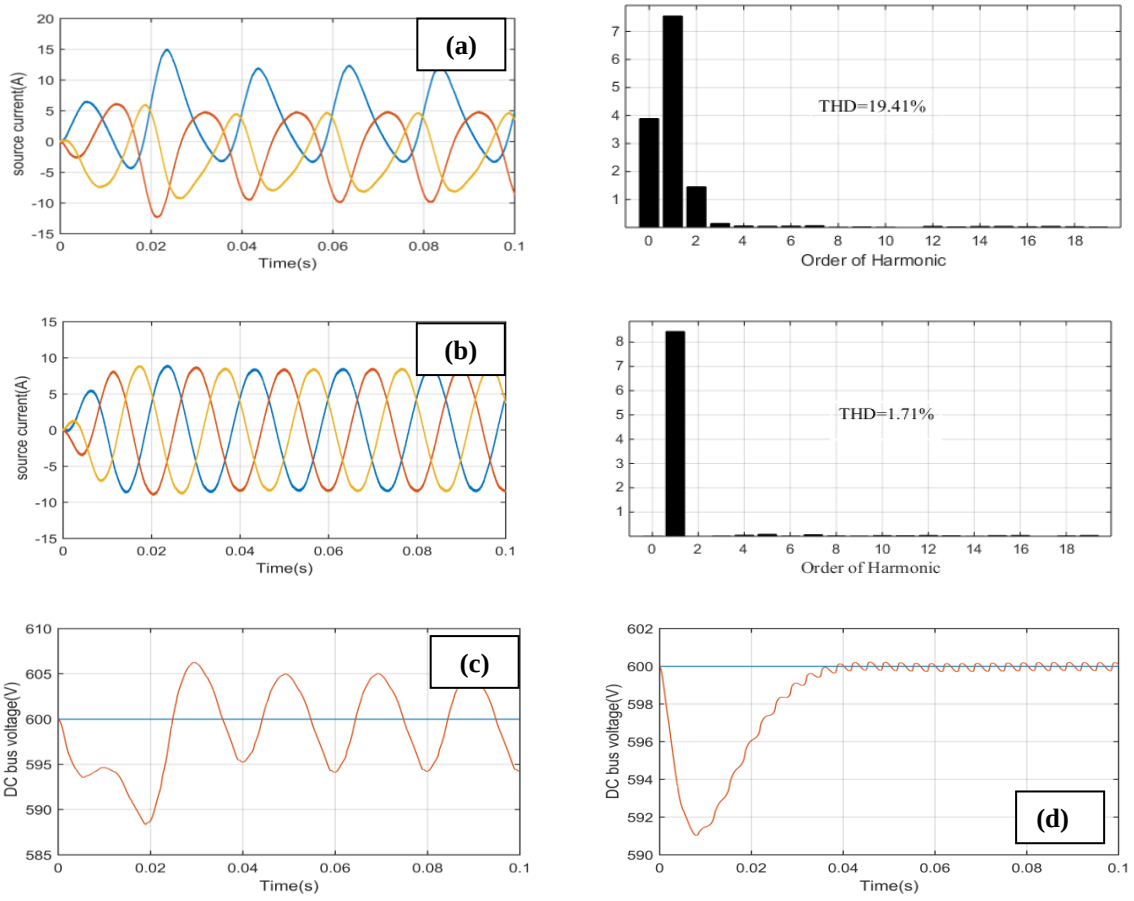

Figure 8. Simulation results under DC offset: (a) source current and its frequency spectrum with the MCCF-PLL, (b) source current and its frequency spectrum with the H-PLL with neural regulator, (c) DC bus voltage with MCCF-PLL, (d) DC bus voltage with H-PLL and neural regulator

4.3. Distorted source voltage condition

In this scenario, the source voltages are unbalanced and distorted with the THD of 10.31%. Figure 9 shows the behavior of the active power filter under unbalanced and distorted conditions. Under this condition, the two schemes converge to similar results.

4.4. Performance comparaison

This subsection provides a comparative study of the proposed H-PLL and the neural regulator to extract the magnitude source of the current with the MCCF-PLL; the methods are compared according to the following standpoints: Unbalance robustness, frequency adaptability, distortions, DC offset, the dynamic of source current and DC bus voltage.

According to Table 1 and Table 2, the proposed H-PLL technique with a neural regulator is recommended as a good alternative mainly because it effectively rejected the unbalance, DC offset, and the harmonic component and offers a satisfactory compromise between the dynamic response, filtering capability.

Table 1. THD under circumstances

THD%	H-PLL	MCCF-PLL
Ideal condition	1.71%	1.89%
Unbalance and distorted	3.48%	2.88%
DC-offset	1.71%	19.41%

Table 2. Comparison of transient responses

Settling time	H-PLL	MCCF-PLL
Frequency step change	<2 cycles [24]	2.5 cycles [28]
Source current	1 cycle	2 cycles
DC bus voltage	2 cycles	3 cycles

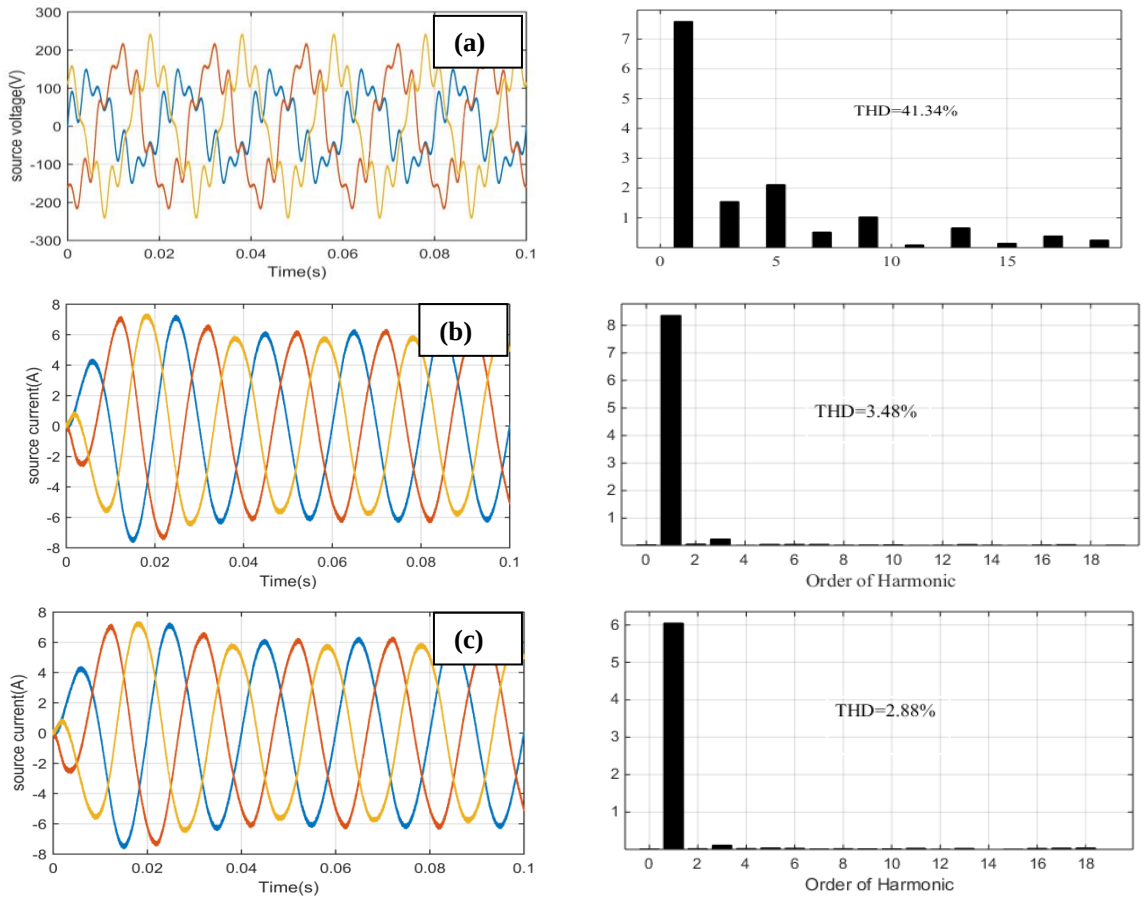

Figure 9. Simulation results under distorted conditions: (a) source voltage and its frequency spectrum, (b) source current and its frequency spectrum with the H-PLL, (c) source current and its frequency spectrum with MCCF-PLL

5. CONCLUSION-

In this paper the H-PLL synchronization technique to enhance the performance of APF under adverse grid conditions with the direct method is presented. The main advantage of the proposed method is the fact of being able to work under adverse grid conditions with the fast-dynamic response and with high stability margin. The neural PI regulator is used to enhance the dynamic of the DC bus. Simulation results have been obtained and show that the proposed H-PLL with a neural regulator is a very suitable for shunt active power filter.

REFERENCES

[1] B. K. Bose, "Global energy scenario and impact of power electronics in 21st century", *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2638-2651, Jul. 2013.

[2] A. Safa, E. M. Berkouk, Y. Messlem, and A. Gouichiche, "An improved sliding mode controller for a multifunctional photovoltaic grid-tied inverter", *J. Renew. Sustain. Energy*, vol. 9, no 6, p. 065506, 2017.

[3] X. Wang and F. Blaabjerg, "Harmonic stability in power electronic based power systems: Concept, modeling, and analysis", *IEEE Trans. Smart Grid*, 2018, in the press, DOI: 10.1109/TSG.2018.2812712.

[4] A. Safa, E. M. Berkouk, Y. Messlem, and A. Gouichiche, "A robust control algorithm for a multifunctional grid-tied inverter to enhance the power quality of a microgrid under unbalanced conditions", *International Journal of Electrical Power & Energy Systems*, vol. 100, pp. 253-264, 2018.

[5] P. Rodríguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, et D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control", *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584-592, 2007.

[6] H. S. Kamil, D. M. Said, M. W. Mustafa, M. R. Miveh, and N. Ahmad, "Low-voltage Ride-through Methods for Grid connected Photovoltaic Systems in Microgrids: A Review and Future Prospect", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 9, no. 4, p. 1834-1841, 2018.

[7] A. Bouknadel, N. Ikken, A. Haddou, N.-E. Tariba, H. E. Omari, and H. E. Omari, "A new SOGI-PLL method based on fuzzy logic for grid connected PV inverter", *International Journal of Electrical & Computer Engineering (IJECE)*, vol. 9, no. 4, pp. 2088-8708, 2019.
[8] H. S. Kamil, D. M. Said, M. W. Mustafa, M. R. Miveh, and N. Ahmad, "Low-voltage ride-through for a three-phase four-leg photovoltaic system using SRFPI control strategy", *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 9, no. 3, p. 1524-1530, 2019.
[9] R. Guzman, L. G. de Vicuña, J. Morales, M. Castilla, et J. Miret, "Model-Based Control for a Three-Phase Shunt Active Power Filter", *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 3998-4007, 2016.
[10] Thirumoorthi, P & T D, Raheni, "Adaptive Method for Power Quality Improvement through Minimization of Harmonics Using Artificial Intelligence," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 8, no. 1, pp. 470-482, 2017, 8. 470.
[11] Laxmi Devi Sahu, Satya Prakash Dubey, "ANN based Hybrid Active Power Filter for Harmonics Elimination with Distorted Mains," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 2, no. 3, pp. 241-248, September 2012, ISSN: 2088-8694.
[12] M. Jauhari, D. C. Riawan, M. Ashari, "Control Design for Shunt Active Power Filter Based On P-Q Theory in Photovoltaic Grid-Connected System," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, no. 3, pp. 1064-1071, Sep. 2018.
[13] M. Qasim, P. Kanjiya, et V. Khadkikar, "Artificial-neural-network-based phase-locking scheme for active power filters", *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3857-3866, 2014.
[14] D. O. Abdeslam, P. Wira, J. Mercklé, D. Flieller, and Y.-A. Chapuis, "A unified artificial neural network architecture for active power filters", *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 61-76, 2007.
[15] Z. Chedjara, A. Massoum, S. Massoum, P. Wira, A. Safa, and A. Gouichiche, "A novel robust PLL algorithm applied to the control of a shunt active power filter using a self-tuning filter concept," in *2018 IEEE International Conference on Industrial Technology (ICIT)*. IEEE, pp. 1124-1131, 2018.
[16] S. Ahmed, G. Madjid, M. Youcef, T. Hamza, "Real-Time Control of an Active Power Filter under Distorted Voltage Condition", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 2, no. 4, pp. 424-433, 2012.
[17] S. Biricik, S. Redif, Ö. C. Özerdem, S. K. Khadem, et M. Basu, "Real-time control of shunt active power filter under distorted grid voltage and unbalanced load condition using self-tuning filter", *IET Power Electron.*, vol. 7, no 7, pp. 1895-1905, 2014.
[18] M. A. Omran, I. I. Ibrahim, A. Z. Ahmad, M. Salem, M. M. Almelian, A. Jusoh, et al., "Comparisons of PI and ANN controllers for shunt HPF based on STF-PQ Algorithm under distorted grid voltage", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 10, no. 3, pp. 1339-1346, 2019.
[19] D. M. Soomro, S. C. Chong, Z. A. Memon, F. Abbasi, "Power quality improvement in QUCEST larkana campus by using three types of power filters", *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 8, no. 4, pp. 1876-1885, 2017.
[20] E. Lavopa, P. Zanchetta, M. Sumner, and F. Cupertino, "Real-Time estimation of fundamental frequency and harmonics for active shunt power filters in aircraft electrical systems", *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2875-2884, Aug. 2009.
[21] R. Chudamani, K. Vasudevan, and C. S. Ramalingam, "Real-time estimation of power system frequency using nonlinear least squares", *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1021-1028, Jul. 2009.
[22] Y. Terriche, J. M. Guerrero, and J. C. Vasquez, "Performance improvement of shunt active power filter based on non-linear least-square approach", *Electr. Power Syst. Res.*, vol. 160, Jul. 2018, pp. 44-55, 2018.
[23] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances", *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1894-1907, 2017.
[24] S. Golestan, J. M. Guerrero, A. M. Abusorrah, and Y. Al-Turki, "Hybrid synchronous/stationary reference-frame-filtering-based PLL", *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 5018-5022, Aug. 2015.
[25] G Abdelmadjid, BM Seghir, S Ahmed, M Youcef, "Sensorless sliding mode vector control of induction motor drives", *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 2, no. 3, pp. 277-284, 2012.
[26] G. Imane, and al., "Neural adaptive kalman filter for sensorless vector control of induction motor", *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 8, no. 4, pp. 1841-1851, 2017.
[27] A. Gouichiche, M. Zabar, Z. Chedjara, A. Safa, and M. Tadjine, "Experimental validation of a fault-tolerant control of induction motor using a voting algorithm", in *2015 3rd International Conference on Control, Engineering & Information Technology (CEIT)*, May 2015.
[28] I.Ghlib, Y. Messlem, and Z. Chedjara, "ADALINE-based speed control for induction motor drive", in *2019 International Conference on Advanced Electrical Engineering (ICAEE)*, Nov 2019.
[29] A. Gouichiche, A. Safa, A. Chibani, and M. Tadjine, "Global fault-tolerant control approach for vector control of an induction motor", *International Transactions on Electrical Energy Systems*, vol. 30, no. 2, p. e12440, 2020.
[30] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Performance Improvement of a prefiltered synchronous-reference-frame PLL by using a PID-type loop filter", *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3469-3479, Jul. 2014.