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Voltage profile and power quality improvement using multicell dynamic voltage restorer

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ABSTRACT

Multi-level converter topologies are increasingly being used in various applications due to their high power, high voltage, and low harmonic levels in the output waveforms. These converter topologies produce different output voltage levels and have a highly modular structure. This paper proposes the design of a dynamic voltage restorer (DVR) based on multilevel topology to enhance the voltage profile and improve the power quality in the network. The DVR is an effective, fast-acting device which detects voltage sags and swells in a transmission line and inject a compensating voltage through a boost transformer. A simulation study is carried out under MATLAB/Simulate to demonstrate the performance of the proposed DVR circuit. The simulation results show improved transient response and enhanced power quality in the transmission network.

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NOMENCLATURE

(α, β)	: NPC	V_S	: Source voltage, v
Θ	: The phase angle to compensate abbreviations	V_C	: Load voltage, v
DVR	: Dynamic voltage restorer	V_{SI}	: Voltage swell, v
THD	: Total harmonic distortion	V_{DVR}	: Voltage injection, v
PSPWM	: Phase shift pulse width modulation	f_C	: The switching frequency, hz
FLC	: Fuzzy logic controller	f_P	: Triangular carrier frequency, hz
NPC	: Neutral-point clamped converter	f_m	: Modulating sinusoidal signal, hz

1. INTRODUCTION

The major causes of electric power quality degradation are caused by asymmetries due to the occurrence of faults in the transmission network. The devices which mitigate the quality of energy are typically installed at the proximity of the critical load to be protected. Those devices may or may not be equipped with an energy storage unit depending on the structure of the network and its rigidity at the point of connection. The dynamic voltage restorer dynamic voltage restorer (DVR) is a series-connected device which is designed to inject a compensating voltage with the required amplitude and frequency to restore the voltage

profile of the network. The DVR is equipped an energy storage unit and an injection transformer which provides the coupling of the device with the grid [1], [2]. The DVR can control the voltage affected by a fault in the network within a few milliseconds, and hence provides efficient protection of the load against disturbances [3]. When equipped with a fast control system, the device is also able to eliminate voltage drops [4], [5]. Proportional-integral (PI) is most used controller for the DVR because of its simplicity and ease of implementation and giving satisfactory performance over a reasonable operating range. However, the main issue with the PI controller is the choice of proportiona and integral gains and in addition, using fixed gains, does not guaranty acceptable control performance over a wide range of operating conditions and system parameters variations. To overcome the limitation of the fixed-gains PI controller, a fuzzy logic-based control strategy is presented in this paper for the DVR based on multi-cell inverter. Fuzzy logic-based controllers have proved to be a powerful and robust control technique in dealing with nonlinear systems and parameter uncertainties.

This paper is organized as follows: section 2 presents th control scheme of the DVR with the implementation of the fuzzy logic controller. Section 3 gives a detailed description of the the multi-cell inverter topology and its switching strategy. Section 4 presents the simulation results and discussion and section 5 summarises the conclusions of this work.

2. CONTROL OF THE DVR

2.1. Control structure of the DVR

As shown in Figure 1, the DVR control scheme consists of two loops: An external voltage generation loop and an internal voltage control loop. The internal voltage control loop calculates the reference voltages for the modulation, which in turn generates the switching signals for the inverter power devices. The external control loop calculates the reference of the compensating voltage to be injected in the network. The voltage generated by the DVR will depend on the compensation strategy used to achieve the desired voltage across the device to be protected [6], [7]. During voltage dips, the supply voltage designated V_{fault} changes in amplitude and phase and the voltage injected by the DVR is denoted V_{DVR}. If the voltage dip is fully compensated by the DVR, the voltage of the load will be restored to its default value. In this paper, pre-fault compensation is applied [8]–[10].

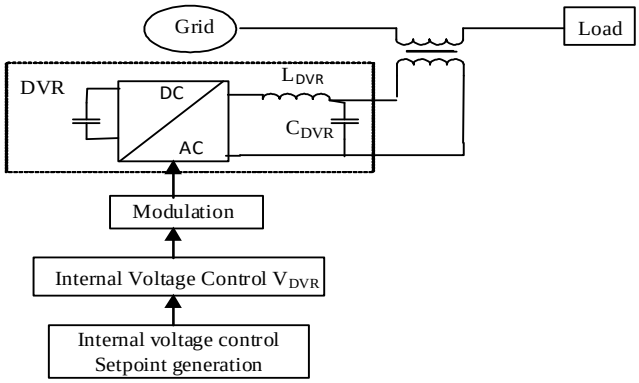


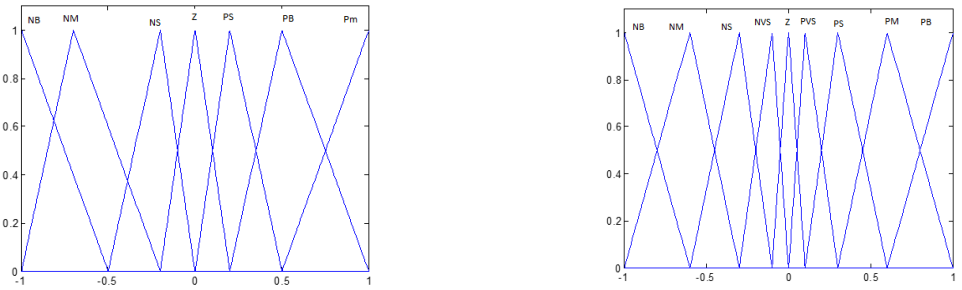
Figure 1. Control scheme of the DVR circuit connected to the network

2.2. Fuzzy logic control in DVR

Applications incorporating fuzzy logic have their inputs, outputs, and control actions specified in terms like those that might be used by human operators [11], [12]. Complex mathematical models of the system are not necessary when using fuzzy logic. The knowledge base is based on the experience of the human expert and comes in the form of a set of rules. The fuzzy rules are expressed in linguistic form in terms of the input variables of the controller and the control variables of the system [13], [14].

Triangular membership functions are used to represent input variables such as negative big (NB), negative medium (NM), negative small (NS), zero (Z), positive small (PS), positive medium (PM), positive big (PB) and for the output variables the fuzzy sets are defined as: negative big (NB), negative medium (NM), negative small (NS), negative very small (NVS), zero (Z), positive very small (PVS), positive small (PS), positive medium (PM), positive big (PB). The membership functions are normalized between -1 to +1. The membership functions of the inputs and outputs are illustrated in Figure 2. There are two inputs, and each input is represented by 7 fuzzy sets, which leads to 49 fuzzy rules. These rules are represented in

Table 1. The output variable is the reference signal for the phase-shifted pulse width modulation (PSPWM) switching control signal of the multi-cell inverter [15], [16].



(a) (b)

Figure 2. Membership functions of the inputs and output variables, (a) error ε, error change Δε and (b) output

Table 1. Rule base of the FLC

Δe / e	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NM	NS	NVS	Z
NM	NB	NB	NM	NS	NVS	Z	PVS
NS	NB	NM	NS	NVS	Z	PVS	PS
Z	NM	NS	NVS	Z	PVS	PS	PM
PS	NS	NVS	Z	PVS	PS	PM	PB
PM	NVS	Z	PVS	PS	PM	PB	PB
PB	Z	PVS	PS	PM	PB	PB	PB

3. OVERVIEW OF THE MULTICELL CONVERTER

In this work, the flying capacitor multilevel converters (FCMC) is used in the DVR configuration. In this work, multicell converters have been used for two purposes; generating a multilevel output voltage and reducing voltage stresses on the power devices [17], [18]. The topology presented in Figure 3 represents a multicellular structure with N switching cells separated from each other by (N-1) floating capacitors [19], [20]. This structure can be adapted to all configurations (chopper or inverter mounting, half-bridge or full-bridge).

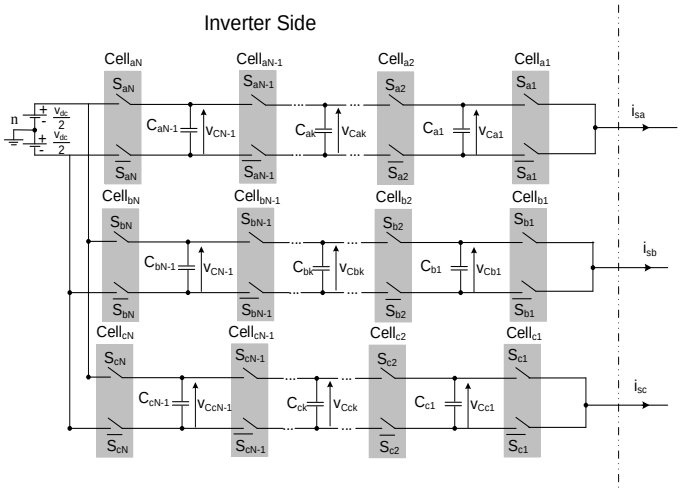


Figure 3. Multilevel inverter topology whit N cells

When the power semiconductor devices are connected in series, it is necessary to ensure a balanced distribution of the supply voltage on the various switches. If we consider the voltage that two switches withstand instead of only one able to withstand V_{dc}, [21] it is necessary to ensure that the voltage applied on these switches is balanced at V_{dc}/N. This work aims to use a three-level multicell inverter topology to demonstrate the following two results:

Table 2 gives the different configurations of a two-cell converter. These configurations describe the states of the switches and define the control states S_k as follows:

- State 1 indicates that the upper switch is on.
- State 0 indicates that the switch is upper switch is open and the bottom on is closed.

In such a structure, the synthesis of the output waveform is much simpler than in the NPC structure [22]-[24]. Table 1 shows the states for a three-level (N = 2 cells) multicell series converter. Here, we must recall that switches of a switching cell are controlled in a complementary manner. This gives 2^N possible logic states (in Table 2, the number of possible states is $2^2 = 4$). In general, a multi-level inverter with N-level voltages requires (N-1) triangular carriers. In phase-shifted multi-carrier modulation, all triangular carriers have the same frequency and amplitude, but there is a phase shift between two adjacent carrier waveforms [25].

Table 2. States of 3 level inverter and its output voltage

Number of States	Output Voltage Level	S_2	S_1	level
1	0	0	0	1
2	$+0.5V_{dc}$	0	1	2
2	$+0.5V_{dc}$	1	0	2

4. SIMULATION RESULTS

The overall system with the DVR power circuit model shown in Figure 4 is implemented in MATLAB/Simulink. Several simulation scenarios are presented to evaluate the DVR control strategy, the pre-default compensation and FLC control technique. The DVR is tested with both multi-cell converter and three-level VSI topologies. Each control strategy will be tested with the following three types of faults that can occur on a parallel distribution line: Three-phase voltage drop, two-phase voltage drop (earth phase) and single-phase voltage drop. For each fault, the waveforms of the disturbed line voltage, the compensating voltage injected by the dynamic voltage restorer and the compensated voltage of the load will be shown in the same figure. The results of the harmonic distortion rate of the load voltage compensated by the DVR for both of topology using FLC controllers Logic Flow will be presented for comparison. The control diagram of the DVR is shown in Figure 5.

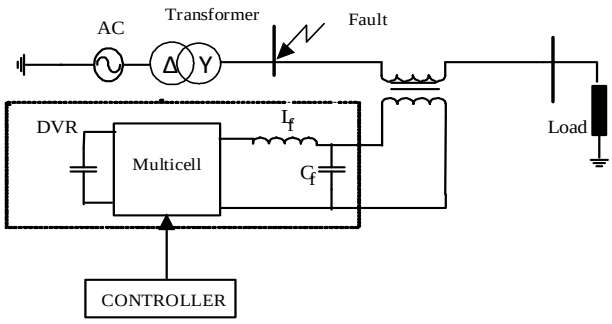


Figure 4. Circuit diagram of the DVR based on the multicell inverter topology

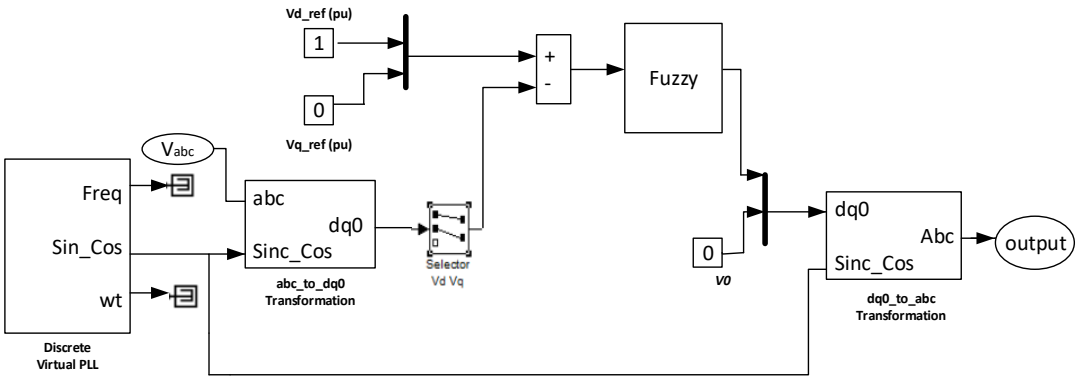


Figure 5. Control scheme of the DVR

4.1. DVR based on multi-cell inverter topology

4.1.1. Single-phase fault

The single-phase fault was simulated as a voltage dip of 0.5 p.u. applied from t=0.2 s to t=0.4 s. Figures 6 demonstrates the effectiveness of the proposed voltage control. A voltage drop of 50% in the zero-sequence voltage for a duration of 0.2 sec is applied to the power system. In Figure 7 present the THD in harmonic order in phase (A) 0.08% and phase (B) 07% and phase (C) 0.09% of the critical load following a single-phase fault. The following Table 3 show the simulation and comparison result carried out with using dynamic voltage restorer in mitigating harmonics. The injection of the pulse-width modulated voltage begins as soon as the interference in the network is detected. The simultaneous emission of harmonics can be reduced considerably by the high cycle frequency of the pulses. The suppression of harmonics occurring at a pulse frequency F_C=2000 Hz.

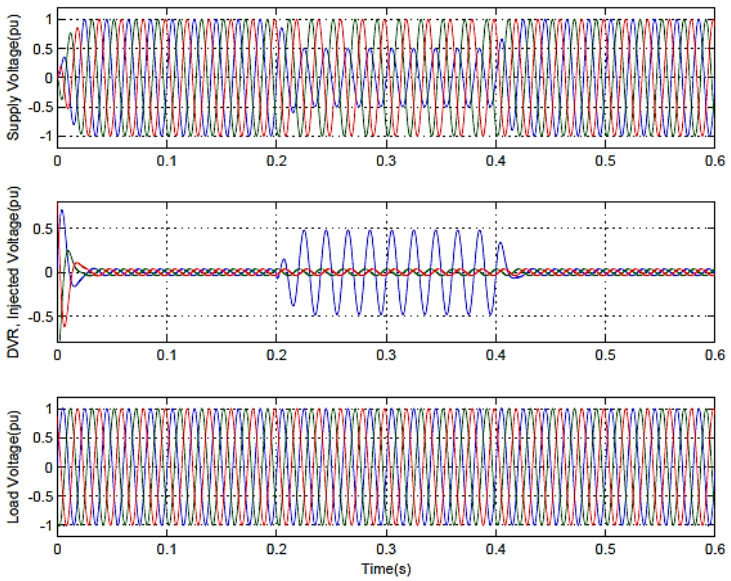


Figure 6. Waveforms of the source voltage, the voltage injected by the DVR, and the critical load voltage for a single-phase ground fault

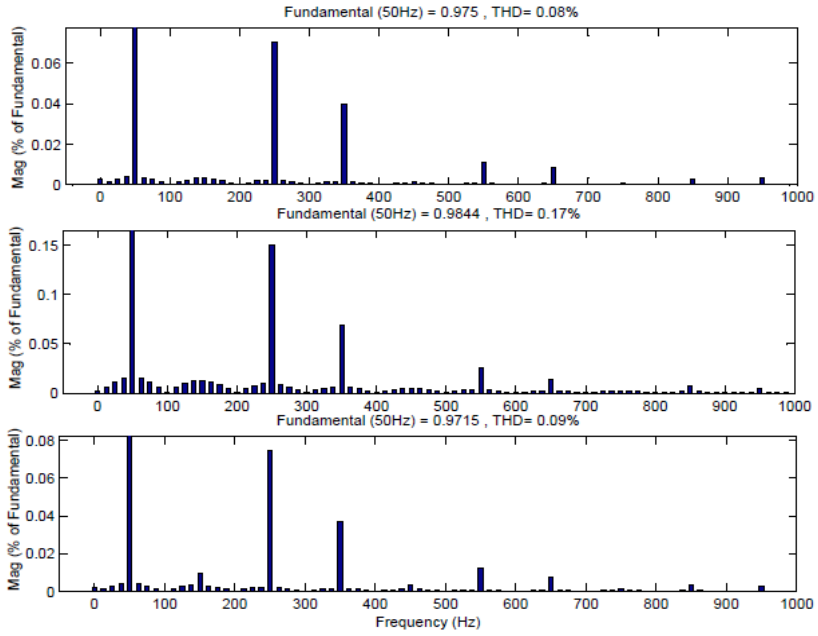


Figure 7. The FFT of the critical load following a single-phase fault

Table 3. Comparison of the voltage levels at the critical load terminals and their THD for a single-phase fault by applying the pre-fault control strategy

	Mutli-cell DVR			Three-level DVR		
Phase of the voltage	A	B	C	A	B	C
THD (%)	0.08	0.17	0.09	0.66	0.60	0.63
Basic voltage (pu)	0.975	0.984 4	0.971 5	0.95 6	0.961	0.959

4.1.2. Two-phase fault

The two-phase fault was simulated as a voltage dip of 0.5 p.u. applied from t= 0.2 s to t = 0.4 s. From Figure 8 it can be observed that following a 50% voltage drop on the two phases of the high-voltage system, the DVR able to maintain good control of the voltage and restore the symmetrical three-phase system back to normal within a time duration of 1 to 2 ms. In Figure 9 we present the THD in harmonic order phase(A) 0.17% and phase (B) 0.08% and phase (C) 0.17% of the critical load following a two-phase fault. The following Tables 4 show the simulation and comparison result carried out with using dynamic voltage restorer in mitigating harmonics.

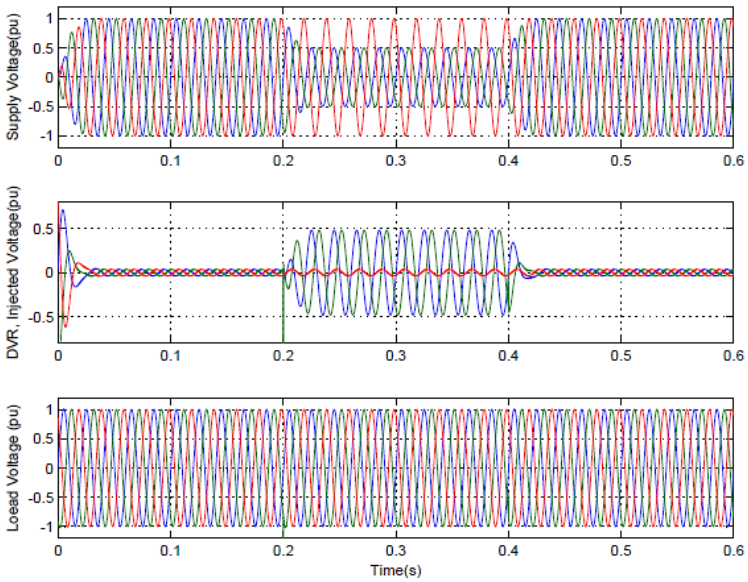


Figure 8. Waveforms of the source voltage, the voltage injected by the DVR, and the critical load voltage for a two-phase ground

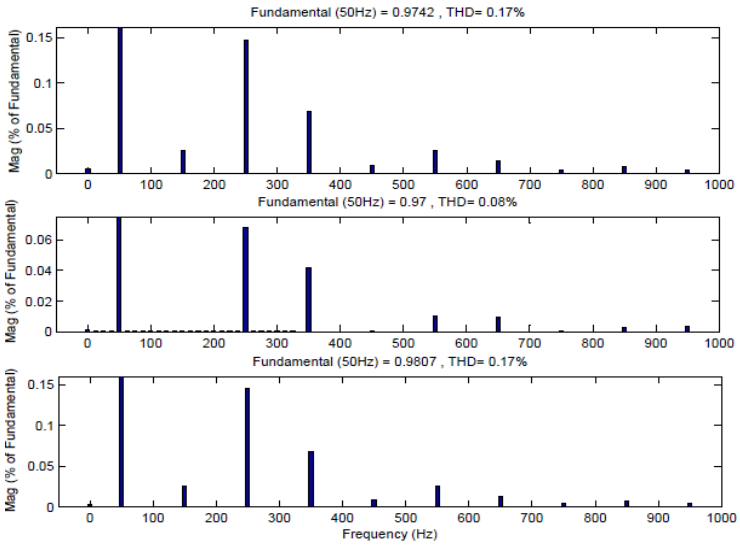


Figure 9. The FFT of the critical load following a two-phase fault

Table 4. Comparison of the voltage levels at the critical load terminals and their THD for a two-phase fault by applying the pre-fault control strategy

	Mutli-cell DVR			Three-level DVR		
Phase of the voltage	A	B	C	A	B	C
THD (%)	0.17	0.08	0.17	0.67	0.64	0.70
Basic voltage (pu)	0.9742	0.97	0.9807	0.956	0.959	0.964

4.1.3. Three-phase fault

The three-phase fault was simulated as a voltage dip of 0.5 p.u. applied from t= 0.2 s to t = 0.4 s. In Figure 10, the DVR reacts by injecting three single-phase voltages in series with the voltages coming from the network to compensate for the difference in voltages existing between the voltages of the front line and after the fault. Each of the injected voltages has an amplitude and a phase that can be controlled independently of the other voltages. In Figure 11 we present the THD in harmonic order in phase (A) 0.17% and phase (B) 0.17% and phase (C) 0.16% of the critical load following a three-phase fault. The following Table 5 show the simulation and comparison of THD between the three-level NPC and multi-cell topologies for the different phases A, B and C. result carried out with using dynamic voltage restorer in mitigating harmonics.

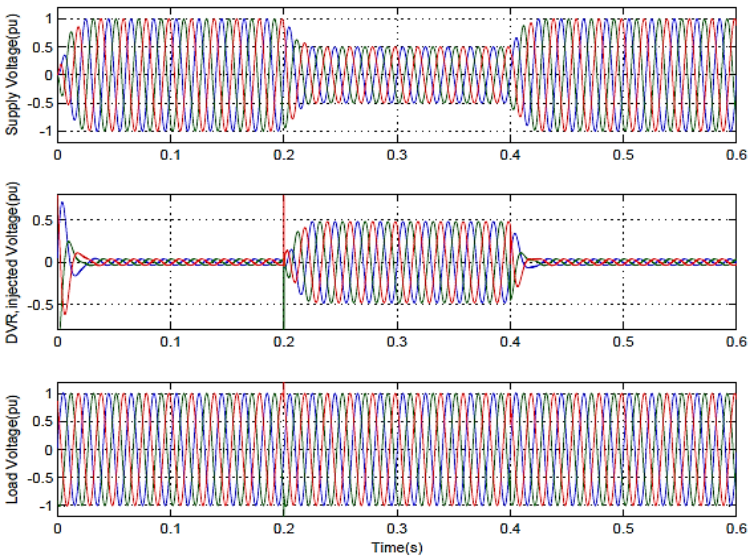


Figure 10. Waveforms of the source voltage, the voltage injected by the DVR, and the critical load voltage for a three-phase ground fault

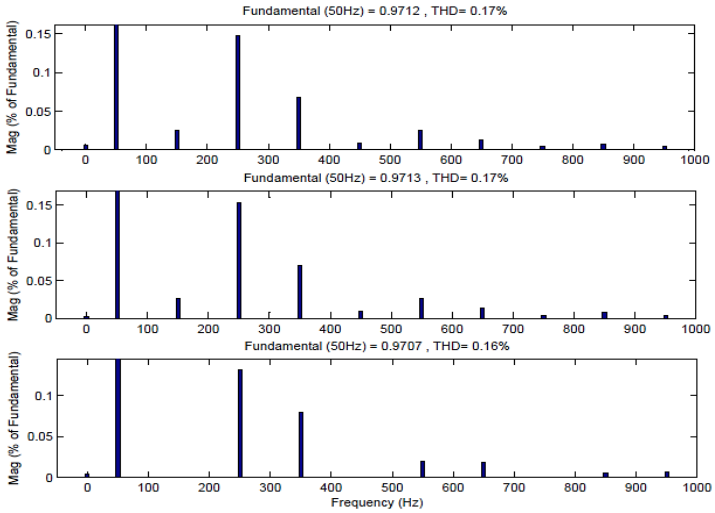


Figure 11. The FFT of the critical load following a three-phase fault

The output voltage delivered by the multilevel inverter has interesting spectral qualities. Through multiplying the number of intermediate levels makes it possible to reduce the amplitude of each rising or falling edge of the output voltage. The amplitude of harmonic lines is therefore even lower. With appropriate PSPWM operation, the use of a multicell converter coupled with a judicious control of the power devices also makes it possible to eliminate certain families of harmonic lines.

Table 5. Comparison of the voltage levels at the critical load terminals and their THD for a three-phase fault by applying the pre-fault control strategy

	Mutli-cell DVR			Three-level DVR		
Phase of the voltage	A	B	C	A	B	C
THD (%)	0.17	0.17	0.16	0.69	0.63	0.63
Basic voltage (pu)	0.9712	0.9713	0.9707	0.95	0.961	0.962

4.2. Three-level neutral point clamped (NPC)

In Figure 12 the structure of three-level inverters is more suited to the conventional structure because the output voltages and currents have a considerably lower harmonic content. The voltage at the terminals of each switch is halved and the level of harmonic content is lower. The space vector modulation (SVM) is used in three-level neutral point clamped inverters [20]. The VSI output voltage will have three voltage levels $-v_{vdc}/2$,0 and$+v_{vdc}/2$, depending on the states of the switches as detailed in Table 6. The following Table 7 shown list of specifications used in the model.

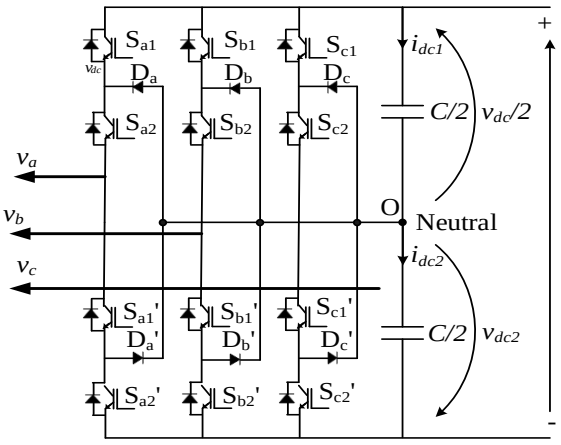


Figure 12. Three level voltage source inverter topologies

Table 6. Switching states for a three level NPC VSI

C_i'	S_{i1}	S_{i2}	S'_{i2}	S'_{i1}	v_{i0}
-1	0	0	1	1	$-v_{vdc}/2$
0	0	1	1	0	0
1	1	1	0	0	$+v_{vdc}/2$

Table 7. Parameters used in the model

Parameter	Value
Grid	Vs=17 KV, f= 50 HZ.
Filtre	L_f =2mH, C_f = 600mF
Load	V_{Load}= 400V, P = 19 KW, Q=1 KVAR
Injection Transformer Yg/ open	S = 20 KVA, Vp =17 KV, Vs =200 V
DC Voltage	200 V
Sampling time *Ts*	10µ s
Capacity, *C*	5000 µF
Switching frequency of PSPWM *Fc*	2 kHz

With: $= a, b, c$, $C'_i$is the switch state variable taking -1, 0, or 1 value, $v_{i0}$is the voltage taken between a phase and the midpoint. The voltage v_{i0} is calculated as (1).

$$v_{i0} = C_1' vdc/2 \quad (1)$$

The output voltages of the three-level inverter will be expressed in α, β plane as (2).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = C_{32} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad (2)$$

Where C_{32} represents the so-called Concordia transformation matrix as (3).

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} C_a' \\ C_b' \\ C_c' \end{bmatrix} \frac{vdc}{2} \quad (3)$$

5. CONCLUSION

To protect the power system from interruptions caused by voltage disturbances, devices to improve the quality of energy such as the DVR can be installed to mitigate these problems. This paper proposed an effective control scheme to improve the voltage profile and enhance the quality of power supplied to critical loads. In this paper we have presented a comprehensive simulation study of dynamic voltage restorer with two inverter topologies based on a three-level multi-cell converter. The control scheme used fuzzy logic control method the phase-shifted PWM (PSPWM) technique which has resulted in significant reduction of the THD to a value of 0.03% as compared to classical three-level inverter which produced a THD of 0.78%. Therefore, critical loads can be effectively protected against different types of voltage dips within a very short period and ensure high quality electrical power delivery to consumers with critical loads hence avoiding financial losses due to these disruptions.

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