# Series FACTS controllers in industrial low voltage electrical distribution networks for reducing fault current levels

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#### ABSTRACT

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#### Keywords:

FACTS Fault current Low voltage switchgear Motor control centre Static synchronous series compensator Thyristor control series capacitor In this paper, series Flexible AC transmission systems (FACTS) devices like Thyristor control series capacitor (TCSC) and Static synchronous series compensator (SSSC) with designed control logic used to reduce the fault current located in LV distribution network at the LV busbar. The electrical distribution network in small and medium scale industries such as steel plants, process and power plants is through low voltage switchgear (LVS) fed from motor control centre (MCC) switchgear through step down transformer of 11kV or 33kV /415V. The designed switchgear in the LV side for these utilities usually is at 50kA. However, the process loads are continuously increasing and sustained with additional feeders with the existing switchgear. Consequently, the fault current at the busbar of the switchgear increases which may require the replacement of entire switchgear to the new design fault current. However, upgrading the existing switchgear is not an economical solution to the industries. Alternatively reducing the fault current at the busbar is feasible. Controller design implemented for reducing the short circuit current with series FACTS devices. A study carried on 800MW Thermal power plant Ash handling LVS in ETAP and Matlab. It is observed that the results are encouraging to use series FACTS devices effectively in the LVS.

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# 1. INTRODUCTION

Industrial plants are fed from 33 kV/11 kV utilities feeder and voltage is step down through a distribution transformer to low voltage (LV) of 415 V. This voltage is provided to different process loads from load centers through motor control centre (MCC) and switchgear arrangement consisting of circuit breakers, fuses, protection equipment, and metering boards. The transformers supply to the LV panel which distributes power to the total demand of the group of loads in the industries as shown in Figure 1.

A short-circuit or fault current rating determines the interrupting capability of the switchgear and the mechanical strength of the bracing and support systems. The load bus fault current mainly depends on impedance and load currents of source transformer. Switchgear fault level and distribution transformer impedance are sized to meet the designed fault level of 50 kA under normal loading conditions. However, loads of industries and capacities of the Plants are expanding as per the demand in the Indian market. Due

to addition of loads the bus fault current will increase beyond of designed value of 50 kA. A consequence of increased fault is shown in Figure 2.



Figure 1. Low voltage side electrical distribution system with and without FACTS device



Figure 2. Effect of fault current on switchgear

Thus the electrical distribution network is to be readjusted without effecting existing circuit designed parameters. As a general industrial practice, plant owners recommend to replace the switchgear to meet the fault current level and occasionally the source transformer should be upgraded. Flexible AC transmission systems (FACTS) [1], [2] devices have been implemented and following are some research papers describing the methodology for reduction of fault current.

#### 2. LITERATURE SURVEY

FACTS [3] devices can regulate active and reactive power as well as voltage magnitude. Placement of these devices in suitable location can lead to the control of the power flow, bus voltage and short circuit [3]. characteristics of a fault current limiter with series compensation is provided in [4]. UPFC [5], [6] is a series and shunt combination FACTS device, and it is applicable for high voltage lines. Fault current limiter is used in 11 kV and 3.3 kV system, and it is not an FACTS device it is a nonlinear reactor added in a circuit to limit the fault current as this reactor is added in series with the circuit there is a voltage drop. For compensating voltage static var compensation (SVC) is connected parallel to the circuit. Static Synchronous Series Compensator [7]-[9] has been used for fault current limit. A novel hybrid current-limiting circuit breaker for medium voltage is presented in [10], [11]. Solid-state circuit breakers and current limiters are used in [12]. A series compensator with fault current limiting function is given in [13]. Fault current limiter by series connected voltage source inverter is provided in [14]. A series connected VSC [15] has been used for limiting the fault current. a New Dual Functional Series Compensator [16] is applied to limit short circuit current. In this paper, Particle swarm optimisation [17] method as proposed to find optimal location with short circuit level and losses. Optimal location can be derived based on losses, as short circuit mainly depends on loading of the line and source, with this approach short circuit limit is not clearly described and also in this grid network is proposed for low voltage

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distribution application is not discussed in this approach. Cascaded H-bridge distribution-static synchronous series compensator [18] has been deployed for finding the short circuit current. Various advantages of TCSC discussed [19] interms of power flow control and fault current reduction. FACTS based fault current limiter is used in thermal power network, and device used in this paper is thyristor protected series capacitor (TPSC) based short circuit current limiter (SCCL) [20]. In this paper SCCL is connected in 400 kV and 230 kV voltage level. And results are compared with 50kA short circuit limit. TCSC will be used for both power flow controller as well as short circuit limiter during faults. Unified power flow controller (UPFC) is used as fault current limiter [21], in this approach predefined impedance are added series to the line to limit the fault current. Fault Current Limiter and SVC are used for short circuit curret analysis in [22]. Inter line power flow controller (IPFC) was used to reduce fault current [23], [24] in this two parallel operation of transformer considered to apply IPFC in a circuit.

# 2.1. Observations and motivation

Distribution static series compensator (DSSC) is used as a fault current limiter in distribution line along with shunt connected STATCOM. DSSC and STATCOM is used to reduce the voltage during the fault condition. As per above different research papers described, fault current limitation of series FACTS devices are more effective in high voltage and medium voltage levels. In this paper utilization of series FACTS devices in 415V distribution for limiting fault current below design fault current value is described with pre-defined fault current settings controller as per Indian standards. And also this paper describes the location of series FACTS devices in LV switchgear for effective control of active and reactive power control in addition to fault current limitation.

#### 2.2. Contributions

- Series FACTs devices are modelled in ETAP and MATLAB.
- Controller design is implemented for reducing the short circuit current.
- The control strategy with series FACTs devices have been applied to 800 MW Thermal power plant Ash handling unit.
- Simulation results are provided.

#### 2.3. Organization

The series FACTS controllers have been developed in ETAP and MATLAB. The rest of the article is as follows: section 2 provides the information of series FACTs devices such as TCSC and SSSC, mathematical modelling of these devices are given in section 3, controller design for TCSC and SSSC are given section 4, case studies are provided in section 5 and finally conclusions are given in the last section.

#### 3. SERIES FACTS CONTROLLER

Two series FACTS controller named TCSC and SSSC are described in this paper. Characteristics of FACTS device are described as shown in,

#### 3.1. Thyristor control series capacitor (TCSC)

Thyristor control series capacitor (TCSC) is shown in Figure 3.



Figure 3. TCSC schematic diagram

For achieving continuous control through the series compensation, thyristor control reactor (TCR) is used in parallel with fixed capacitor. The TCSC is connected in series with the load circuit to obtain desired

voltage rating and operating characteristics. The basic requirement of TCSC scheme is to provide a continuously variable capacitance by means of partially cancelling the effective compensating capacitance by the TCR. The TCR at the fundamental system frequency is a continuously variable reactive impedance, controllable by delay angle  $\alpha$ , the steady state impedance of the TCSC is that of a parallel LC circuit, consisting of a fixed capacitive impedance,  $X_C$ , and a variable inductive impedance,  $X_L(\alpha)$ , that is shown in (1).

$$X_{TCSC}(\alpha) = \frac{X_C X_L(\alpha)}{X_L(\alpha) - X_C} \tag{1}$$

The delay angle measured from the crest of the capacitor voltage. The TCSC thus presents a tunable parallel LC circuit to the line current that is substantially a constant altering current source. As the impedance of the controlled reactor,  $X_L(\alpha)$ , is varied from its maximum (infinity) towards its minimum  $\omega L$ , the TCSC increases its minimum capacitive impedance,  $X_{TCSC,min} = X_C = \frac{1}{\omega C}$  (this mode is known as capacitive compensation). Decreasing  $X_L(\alpha)$  further, the impedance of the TCSC, becomes inductive. Therefore with the usual TCSC arrangement in which the impedance of the TCR reactor is smaller than that of the capacitor. The characteristics [11], [12] of TCSC are shown in Figure 4. When ever a fault appears in the system, TCSC senses the low voltage and firing angle mode changes to operate in inductive region to add additional impedance in the circuit.



Figure 4. Characteristics of TCSC

# 3.2. Static synchronous series compensator (SSSC)

The SSSC is a series compensation device of the FACTS family using power electronic based voltage source converter and DC link to control the power flow in transmission line. It can control the voltage at the bus as well as active power in a transmission line and further improves the transient stability [13], [14]. Typical single line diagram of SSSC is indicated in Figure 5 where the SSSC is connected in series to the load. Depending on load demand SSSC will inject a voltage in a respective line or bus to control the power in order to compensate additional load requirement in a low voltage distribution network. As shown in Figure 6 simplified diagram of series compensation with the phasor diagram, where  $V_s$  is the sending voltage,  $V_r$  is the receiving voltage,  $V_{se}$  is the series injected voltage of the SSSC,  $V_1$  is the voltage drop across the Line impedance and  $\delta$ is the phase difference between  $V_s$  and  $V_r$ .



Figure 5. SSSC single line representation

Figure 6. Phasor diagram of SSSC

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Line impedance and  $\delta$  is the phase difference between  $V_s$  and  $V_r$ . The SSSC can be stated that depending on increased load demand, the series voltage injected by the SSSC is in phase with the generated voltage. It increases the voltage across the transmission line and thus increases the corresponding line current and transmitted power. During fault conditions controller senses the low voltage on faulted bus and provides injection of voltage in the opposite direction of generated voltage, in this region it operates in inductive mode of operation and net effective current will be reduced. The SSSC controls fault current, improves voltage stability, provides power oscillation damping and acts as a fault current limiter. Simplified impedance network of SSSC for 3 phase fault is shown in Figure 7.



Figure 7. Simplified Impedance network for 3 phase fault

# 4. MATHEMATICAL MODELS

# 4.1. Mathematical model with source transformer

Mathematical model for short circuit current of a typical source transformer connected to a switchgear shown in Figure 5 is derived as per below. Consider a 3 phase fault at the bus, simplifying the Figure 7 network which can be represented as the network shown in Figure 8.



Figure 8. Simplified Impedance network for 3 phase fault

Solving impedance network for finding  $I_{SC}$  and given in (2) and (3).

$$Z_{SC} = \frac{Z_L \times Z_T}{Z_L + Z_T} \tag{2}$$

$$I_{sc} = \frac{E}{1.732 \times Z_{SC}} \tag{3}$$

Using the as shown (3), the fault current at bus can be calculated. Bus fault current mainly depends on the source transformer impedance. However, load impedance is process oriented and it cannot be controlled. For any change in fault current at the load bus, it is required to select the transformer impedance appropriately so as to reduce the fault current to the desired level.

#### 4.2. Mathematical model of TCSC

The single line diagram of distribution network with TCSC is shown in Figure 9. During normal operation TCSC acts like a compensation device by improving voltage profile at bus and also it compensates the reactive power by providing additional current to the load without affecting the source parameters. TCSC operates in capacitive mode and current flows to the load as shown in Figure 10.

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Figure 9. TCSC connection in distribution network

Figure 10. Impedance network of TCSC

During this mode currents at bus are added as so that the current will be improved. Figure 11 depicts the fault condition. During the fault condition, sensing no voltage at bus and high current flow, controller of TCSC operate in inductive region as shown in Figure 12.



Figure 11. 3 Phase fault at bus with TCSC

Figure 12. Inductive mode of operation of TCSC

In this region, net current flows will be reduced and required current will be controlled with and the effect of fault current will be reduced. As per above schematics, the fault current at bus is represented as shown in (5)

$$I_C = I_L - I_{TCR} \tag{4}$$

$$I_F = I_C + I_{Load} \tag{5}$$

With the TCSC operation during fault condition as in inductive reason the net fault current will be reduced with controlling current. During fault conditions, the operation of TCSC is in an inductive region so that the net fault current will be reduced by controlling the current, $I_{TCR}$ .

#### 4.3. Mathematical model of SSSC

In Figure 13,  $V_{se}$ ,  $jX_{se}$  are series injected voltage and reactance of SSSC and  $V_{seff}$  is a SSSC selfbus voltage connected between source voltage and load voltage,  $jX_L$  is the line reactance. Assuming fault occurs at load bus, during fault condition the current at respective bus starts increasing and voltage of the same starts decreasing. At this time feedback to controller change the firing angle in order to shift SSSC to inductive mode of operation, considering firing angle changes, SSSC starts injecting voltage in the opposite direction of generated voltage , as a result net fault current will be reduced com in comparison to the case without using SSSC. Figure 13, to find fault current  $I_F$ . From the (8) the contribution of fault current of source  $E_1$  is reduced due to series voltage injection of  $V_{se1}$  with this fault current can be minimized. From this model it can be observed that SSSC can be utilized to improve voltage and support sudden changes of load in a line and also it can minimize fault current SSSC can limit the short circuit due to fault in bus.



Figure 13. SSSC single line diagram

$$V_1 = V_{se} + I_{se} \times jX_{se} + V_{seff} \tag{6}$$

$$I_F = I_{se} + I_L \tag{7}$$

$$I_{se} = \frac{V_1 - V_{se} - V_{seff}}{jX_{se}} \tag{8}$$

#### 5. CONTROLLER LOGIC FOR INJECTION OF VOLTAGE

The main function of the controller is to inject the voltage as per the fault current at the bus. This controller works only when the fault level seen by the current transformer (CT), is greater than 50 KA and as per required ratio, voltage will be injected into the circuit with phase shift to achieve inductive mode of operation. As shown in Figure 14, as a closed indirect controller which consists of pre-defined functional blocks with reference to load current. Assuming losses at DC end is minimal and V1 and V2 are source and load voltages, VDC is generally 1/3rd of the source voltage and the same voltage will be injected in series for compensation. Assuming 3 phase fault at load end and the fault current is greater than design fault current of 50 kA, and voltage of load end on that time as almost zero, and threshold limit is provided to 0.4 V2, during this condition Ki is the injection factor with -1, due to this factor firing pulse generated will be more than -900 and its injection voltage will be in –ve direction of generation voltage0. In addition, the required voltage to be injected in the ratio of fault current of 50 kA. Rewriting the (6), with minimum losses across the capacitor VDC = Vinj. Vse is Vinj voltage and net effective current will be reduced below designed fault current. The same control logic will be represented for TCSC as shown in Figure 15.

$$V_1 = K_f V_{inj} + I_F \times j X_{se} \tag{9}$$

$$I_F = \frac{V_1 - K_f \times V_{inj}}{jX_{se}} \tag{10}$$



Figure 14. Control schematic diagram for SSSC

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Figure 15. Control schematic diagram for TCSC

#### 6. RESULTS AND DISCUSSION

Simulation is carried for different case studies and results are compared. The case studies are considered as per below.

- Case-1 In this case fault current is calculated for normal industrial load distribution MCC switchgear.
  For this case loads are considered at 800MW power plant Ash handling (AHP) unit MCC LV switchgear power distribution board. Short circuit calculation is performed in ETAP. For this model source transformer impedance is considered as per IS 1180-2014 [25].
- Case-2 From the above case-1 analysis short circuit current reduction methodology is applied by increasing transformer impedance.
- Case-3 TCSC is introduced in series with the circuit and short circuit analysis is performed with SIMULINK model.
- Case-4 Introduced SSSC in series is introduced with the circuit and short circuit analysis performed with ETAP and SIMULINK model.

For all above cases, results are compared with and without series FACTS devices.

#### 6.1. Case-1 normal industrial load distribution MCC switchgear

As per load distribution shown in Figure 16, the source transformer is feeding to the load which is connected to MCC switchgear. Source transformer rating is arrived as per load condition and its process operating conditions. In this case transformer impedance is considered as 6.25 % as per IS 1180-2014 condition. Generally, design will be carried for the worst operation condition as single transformer operating with bus coupler closed condition. In this operating condition ETAP short circuit analysis is performed considering 3 phase fault at switchgear bus, and results are as indicated in below Figure 17.



Figure 16. Single line diagram of AHP MCC switchgear

As per calculations and ETAP analysis fault current at bus faults reaches 68.1kA. Standard Low voltage (LV) switchgear is available for 50 kA fault level or 65kA fault level.By increasing fault current capacity at bus the cost of LV switchgear increases. Alternative methods to reduce the fault current to a less value than 50 kA are by increasing the impedance of the transformer or distribute the load with another set of transformer. The second approach which adding of an additional transformer is not an economical solution.



Figure 17. ETAP Short circuit analysis for AHP MCC

# 6.2. Case-2

From the above analysis, to reduce fault current, one of the methods can be adopted is increasing the impedance of the transformer, reducing the fault current up to desired level. As shown in Figure 18, the transformer impedance increased from 6.25 % to 10 %, results in bus fault current reduces to 48.5kA, which is less than designed fault current of 50 kA. The disadvantages of increasing impedance of transformer are, voltage drop increases and design of transformer has to be changed to suit permissible losses with increased impedance, with the effect of increased impedance cost of the transformer also increases. It is suggested to have series FACTS devices in a network for utilizing multiple effects. Among these effective use is to reduce fault current at the bus, the same is described in the below case studies. The disadvantages of increasing the transformer impedance are:

- Voltage drop increases
- Transformer design has to be modified to suit the permissible losses.
- Cost of the transformer also increases

To overcome these demerits, it is suggested to include series FACTS devices in a network in order to serve multiple needs of the network.



Figure 18. ETAP Short circuit analysis for increased transformer percentage impedance

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# 6.3. Case-3

From the above case-1 model simulated in Simulink, the results are shown in below Figure 19 The fault current obtained in Simulink model is 65kA. Including the effect of TCSC in the same model adding in TCSC in series as shown in Figure 20. TCSC connected as a part of LV switchgear and fault is created at LV switchgear bus. From the results it is shown in Figure 21, that when there is a series TCSC device is added in a distribution network, the fault current is reduced to 45kA and it is lower than the design fault current of LV switchgear i.e. 50 kA.



Figure 19. Bus fault current without FACTS device



Figure 20. Simulink model with TCSC for AHP MCC



Figure 21. Bus fault current with TCSC device

#### 6.4. Case-4

In this case, SSSC is connected and a 3 phase fault is created on bus, the ratio of fault current to design fault current is Actual bus fault current 68.85kA from the above ETAP analysis and 50 kA is the design fault current. Normal Vinj is around 138.33V that is the voltage across the capacitor terminal. the SSSC is simulated in ETAP as indicated in Figure 22.



Figure 22. Bus fault current with series voltage injection in opposition direction

The fault current is obtained with the analysis is of 46.9kA and it is below designed fault current. The same model is simulated in Simulink the SSSC is able to reduce bus fault current to 46kA indicated in Figure 23. From the result it is indicated that SSSC device can also reduce fault current to below designed fault current. Both the ETAP and Simulink models are effectively worked with the controller and results are approximately equal. With this predefined logic, controller is effectively working to reduce the fault to below design fault current.



Figure 23. Bus fault current with SSSC device

#### 6.5. Result comparison

In Figure 24 indicates the fault currents for different cases. The fault current including TCSC and SSSC devices are reduced below designed fault current. In all cases, series FACTS devices are placed between LV circuit breaker and LV switchgear Busbar, in order to provide series compensation to entire load and at the same time, reduce fault current to safeguard the switchgear equipment. As per this analysis we can explore the implementation of series FACTS devices in low voltage (415V) Distribution network for reduction of fault current without changing Transformer impedance and switchgear at standard fault currents. Series FACTS devices generally will be used to improve the voltage profile and active power improvement. Apart from

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this in low voltage, 415V distribution, fault reduction is introduced by FACTS devices, this will improve LT distribution network without any change in existing equipment (like LT Switchgear/ Distribution transformers).



Figure 24. Bus fault current comparison chart without and with FACTS devices

# 7. CONCLUSION

This study and analysis is mainly focused on the series FACTS devices locating them in 415V LV switchgear distribution networks and analysing the effectiveness of each series FACTS device in terms of reduction of fault current. As per the results series FACTS devices are suitable for reducing the fault current and it will be effectively utilised for Active power injection, reactive power injection and voltage profile improvement as well fault current reduction. The effective reduction of fault currents, avoids replacing existing LV switchgears and increasing impedance of the transformer. Use of TCSC/SSSC proves to be a cost-effective solution which can be implemented for various process plants.

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Alivelu manga Parimi Alivelu M Parimi has received the B.E. Electrical and Electronics Engineering in 2001 and Master in Control System Engineering from Andhra University. She received her Ph.D. degree in Electrical engineering from University Technology Petronas, Malaysia in 2011. In 2012 she joined as an Assistant Professor in Department of Electrical Engineering in BITS Pilani Hyderabad Campus and at present working as Associate Professor. Her research interests include Renewable Energy Sources, FACTS, Power system stability, Power Quality, Reactive power compensation, Modal analysis, Control Systems applications, Control Systems applications.



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