International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 12, No. 3, September 2021, pp. 1738~1750
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v12.i3.pp1738-1750

The new approach minimizes harmonics in a single-phase three-level NPC 400 Hz converter for airplanes

Do Ngoc Quy[1], Do Ba Phu[2], Nguyen Kien Trung[3]
[1,2]Institute for Control Engineering and Automation, Hanoi University of Science and Technology, Ha Noi, Vietnam
[3]Department of Inducstrial Automation, Hanoi University of Science and Technology, Ha Noi, Vietnam

Article Info

Article history:

Received Ju; 24, 2020
Revised Apr 27, 2021
Accepted Jul 14, 2021

Keywords:

400 Hz inverter
Balance neutral point
Minimize harmonics
NPC

ABSTRACT

This paper provides a new approach to reducing high-order harmonics in 400 Hz inverter using a three-level neutral-point clamped (NPC) converter. A voltage control loop using the harmonic compensation combined with NPC clamping diode control technology. The capacitor voltage imbalance also causes harmonics in the output voltage. For 400 Hz inverter, maintain a balanced voltage between the two input (direct current) (DC) capacitors is difficult because the pulse width modulation (PWM) modulation frequency ratio is low compared to the frequency of the output voltage. A method of determining the current flowing into the capacitor to control the voltage on the two balanced capacitors to ensure fast response reversal is also given in this paper. The combination of a high-harmonic resonator controller and a neutral-point voltage controller working together on the 400 Hz NPC inverter structure is given in this paper.

Corresponding Author:

Nguyen Kien Trung
Department of Industrial Automation
Hanoi University of Science and Technology
No. 1 Dai Co Viet Road, Hai Ba Trung, Ha Noi, Vietnam
Email: trung.nguyenkien1@hust.edu.vn

1. INTRODUCTION

Currently, 400 Hz ground power unit systems (GPUs) are being widely used to power aircraft. The aircraft's electrical equipment requires total harmonic distortion (THD) to be small. The reduction of harmonics caused by the inverter and nonlinear load is a problem being studied. One widely used variable structure is the unipolar inverter [1]-[7]. This structure works very simply. But the inductor-capacitor filter (LC filter) used in very large sizes [1] to ensure the small harmonics are the downside of this structure. The controller can use two loops of voltage and current [2] on the continuous domain but cannot do so on the discontinuous domain [3]. A PI current controller has been implemented on hardware in the loop [6] but has not succeeded in controlling the output voltage. A current deadbeat controller [4] is used to control the current but gives high harmonics.

Another structure that creates three levels of NPC voltage is also being widely used for the 50/60 Hz inverter [8]-[16]. This structure has the advantage of using an LC filter with a smaller value than the unipolar inverter structure [8]. A major problem in this structure is the voltage balance between the two DC capacitors because the capacitor voltage imbalance increases the output harmonics of the converter. There are ways to perform voltage balancing [9], [10]. These methods have balanced the voltage across the capacitor with a small error but the response time is too large [10], [15] for the 400 Hz frequency and the calculation is too complicated [9], [14] to cause a 400 Hz inverter system delay. One method to help keep the two DC

capacitors balanced is to use a single DC/DC pulse inverter to ensure that the two capacitors are always equal in [13]. However, this method is too complicated.

In recent years, the study of variable structure for 400 Hz inverters has paid more attention. As in [17] a 3 phase NPC 400 Hz inverter was used, the LC filter circuit structure and the switching process were of interest. As Mathew *et al.* [18] the structure of single limb of the diode clamped inverter is simulated on hardware in the loop, FPGA. However, the higher harmonic components of the output voltage have not been considered. Another multilevel inverter that is also used to generate 400 Hz is the ANPC structure, with which the voltage on the two DC capacitors will be balanced as shwon in [19] and [20]. However, this structure uses too many switching devices. This paper presents a new approach with three-level NPC single phase inverters for 400 Hz inverters. A proposed voltage balancing controller on the capacitors has a very fast response speed. An output voltage control loop using resonant controller combined with harmonic compensation of order 3rd, 5th, 7th makes a small THD on the output voltage waveform.

The next section of this paper describes how to modulate three levels of output voltage. Next, the design of neutral point voltage controller is presented. Section 4 shows the output voltage controller design. Finally, the simulation results on MATLAB and the experiment results with 5kW inverter is shown on section 5. A 1.46% on THD with a small output filter is obtained in the experiment result.

2. STRUCTURE AND MODULATION METHOD OF NPC INVERTER

The structure of the NPC inverter is shown in the Figure 1, this structure is also shown in [13]-[15]. The NPC single-phase inverter uses four pairs of semiconductor switches and two pairs of clamping diodes along with two capacitors C_1 and C_2 to generate three levels output voltage [11]. The switching states of the semiconductor switches are shown in Table 1. The converter uses a 400 Hz high frequency transformer with integrated filter inductor combined with the output AC filter capacitor.

The NPC inverter are modulated by the space vector method. A vector of magnitude V and angular velocity ω is treated as the modulation input in Figure 2. To generate output voltage of the inverter with voltage levels {-E, -E/2,0, +E/2, E} the space vector modulation diagram is divided into 4 regions [16]. From the switching states, as shown in Table 1 and the spatial vector modulation graph Figure 2, each small voltage vector and zero voltage vector are generated from 2 to 3 switching states, respectively. The switching states in each voltage region will be selected to ensure voltage balance across the DC-link capacitor and reduce the number of switching states. The switching order in each modulation region is show in Table 2. Specifically, if you want to modulate the output voltage {E, E/2}, the semiconductor valves switch by region 1. Similarly, region 2 will generate voltage {0, E/2}, region 3 will generate voltage {-E/2,0}, region 4 will generate voltage {-E, -E/2}.

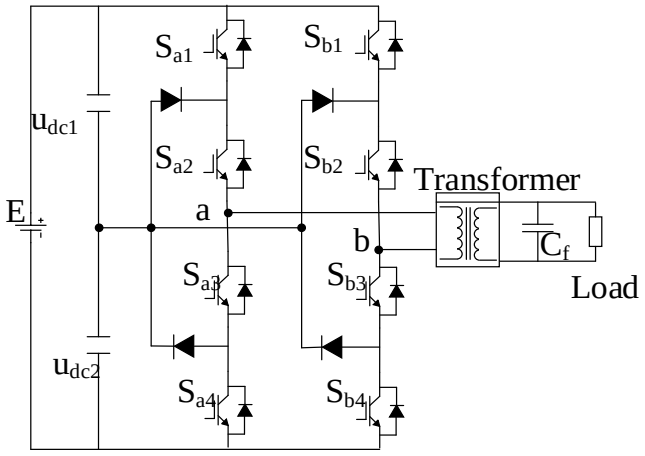


Figure 1. Main circuit for diode-clamped single-phase three-level inverter

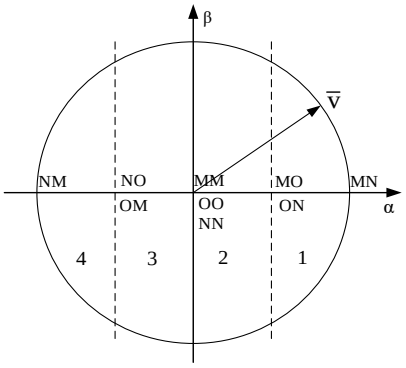


Figure 2. Space voltage vector diagram

Table 1. Switching states

Switching state	Sx1	Sx2	Sx3	Sx4
M	ON	ON	OFF	OFF
O	OFF	ON	ON	OFF
N	OFF	OFF	ON	ON

Table 2. Switching order

Region	Order of switching
1	MO → MN → ON → MN → MO
2	MO → OO → ON → OO → MO
3	OM → OO → NO → OO → OM
4	OM → NM → NO → NM → OM

3. NEUTRAL-POINT POTENTIAL CONTROL

3.1. Effects of neutral-point voltage controller

The neutral-point voltage control aims to control the voltage across the two DC capacitors equally and equal to half the input DC voltage [15]. In fact, the impedance of the two capacitors is not equal, charging and discharging time of capacitors when the system is operating is not equal. As a result, one of the two capacitors will be over-voltage, which will endanger the system when operating at high capacity. Because the exact E/2 voltage cannot be created, high-order harmonics will appear that adversely affect the output voltage quality, which will be shown in the simulation results.

3.2. Modeling control objects

The voltage on the two capacitors depends largely on the current at the neutral point. In this case, the main control object model is to find the relationship between the two capacitors voltage and current at the neutral point. Figure 3 shows the voltage across the two capacitors and direct current to the capacitor. Where R_1 and R_2 correspond to the internal resistance of the capacitor; V_{C1}, V_{C2} and I_{C1}, I_{C2} correspond to the voltage and current on each capacitor; i_0 is the load current. Application of Kirchhoff's law [21]:

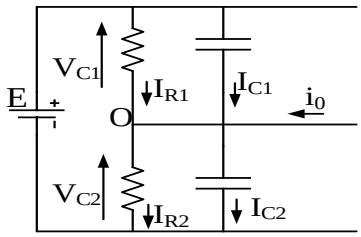


Figure 3. Capacitor loading model

$$i_0(t) + C_1 \frac{dV_{C1}(t)}{dt} + \frac{dV_{C2}(t)}{R_1} - C_2 \frac{dV_{C2}(t)}{dt} - \frac{V_{C2}(t)}{R_2} = 0 \quad (1)$$

$$\Rightarrow \frac{dV_{diff}(t)}{dt} - \frac{1}{RC} V_{diff}(t) = -\frac{1}{C} i_0(t) \quad (2)$$

where $C_1=C_2=C$ and $V_{C1}(t)-V_{C2}(t)=V_{diff}(t)$.

Assuming that the voltage is in region 1 as shown in Figure 2, the MO combination will perform during ton1 and generate current $i_0(t)= -i_L(t)$. The average current passing through the neutral point in the PWM cycle is as shown in (3):

$$\langle \overline{i_0(t)} \rangle_{T_{PWM}} = \frac{t_{on1} - t_{on2}}{T_{PWM}} \langle \overline{i_L(t)} \rangle_{T_{PWM}} \quad (3)$$

Like other regions, the average value of $i_0(t)$ in a PWM cycle is as ashown in (4):

$$\langle \overline{i_0(t)} \rangle_{T_{PWM}} = m(v_{ab}) \,.\, n(t) \,.\, \langle \overline{i_L(t)} \rangle_{T_{PWM}} \quad (4)$$

The function n(t) denotes the amount of time i_0 current is in the opposite and opposite direction to i_L current on the inductor in the T_1 period.

$$n(t) = \frac{t_{on1} - t_{on2}}{T_1} \quad (5)$$

where t_{on1} is the time that $i_0(t)=i_L(t)$, t_{on2} is the time that $i_0(t)=-i_L(t)$.

The function $m(v_{ab})$ is a function that shows the valve's opening and closing time in each region, specifically:

$$m(v_{ab}) = \begin{cases} 2 - 2v_{ab}/E; E/2 < v_{ab} \leq E \\ v_{ab}.2/E; 0 < v_{ab} \leq E \\ -v_{ab}.2/E; -E/2 < v_{ab} \leq 0 \\ 2 + 2.v_{ab}/E; -E < v_{ab} \leq -E \end{cases} \quad (6)$$

From (2) and (4) shows the relationship between the two capacitors voltage and the current at the neutral point as shown in (7) and (8):

$$\frac{dV_{diff}(t)}{dt} + \frac{1}{RC}V_{diff}(t) = -\frac{1}{C}m(v_{ab})\overline{\langle i_L(t)\rangle}_{T_{PWWM}}n(t) = \phi(t, v_{ab}) \quad (7)$$

$$G(s) = \frac{V_{diff}(s)}{\phi(t,v_{ab})} = \frac{1}{s+\frac{1}{RC}} \quad (8)$$

in (8) shows the modeling of the object.

3.3. Design of the balances neutral-point voltage controller

G(s) is a stable transfer function without control. However, to achieve a fast response rate and eliminate static deviations, an integral has one point not added to improve quality.

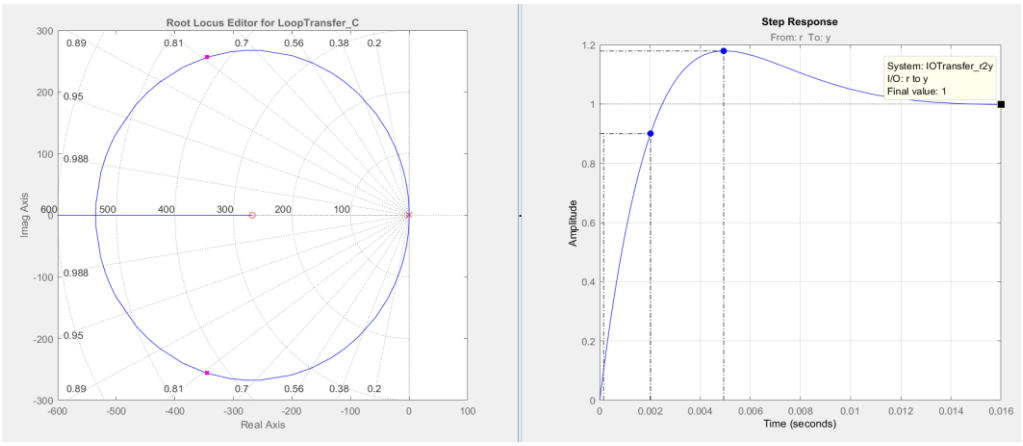
$$G_c = K\frac{s+c}{s} \quad (9)$$

To fulfill these two requirements, a control system can be designed as a zero-pole network in which a null pole will meet the first item and a zero is placed precisely on the negative part of the real axis. Its module should be larger than the plant pole one. Figure 4 (a) and Figure 4 (b) shows the root locus diagram and response of the system after the addition of a neutral point voltage controller.

For the system parameters in this paper, the controller parameters are: K=700.2 and c= 271. The essence of the control of the neutral point voltage is to control the timing of charge and discharge current for two capacitors, which is to control the variable n(t).

$$n(t) = \phi(t, v_{ab})\frac{-C}{i_{L(t)}\, m(v_{ab})} \quad (10)$$

From (10), to avoid the case of division by zero, a limit [-1000, +1000] is used. Moreover, there is also a limit [-1, +1] for the output value of n(t). Figure 5 shows the control structure of the neutral-point voltage. In the case, the value set corresponds to the state of the voltage on the two DC capacitors are equal.



(a) (b)

Figure 4. Root locus diagram and system response, (a) root locus diagram; (b) system response

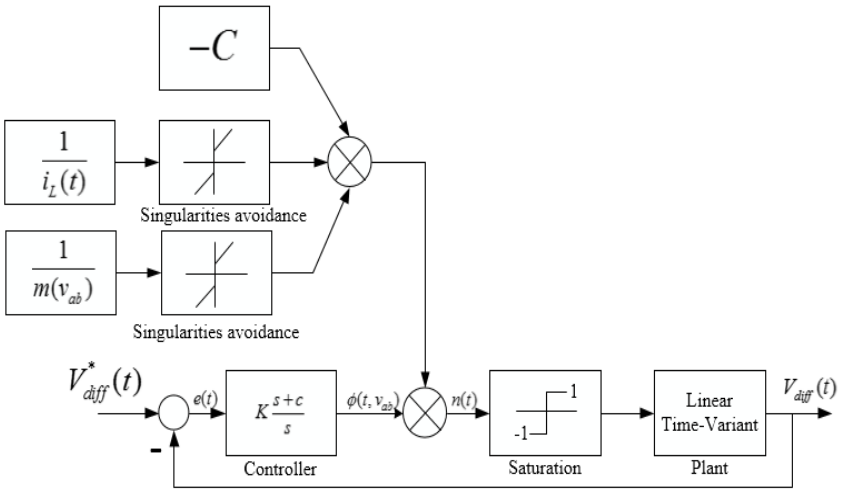


Figure 5. Neutral-point voltage control structure

4. RESONANCE VOLTAGE CONTROLLER

Figure 6 (a) shows the overall structure of the system. The control of the neutral point voltage shall be from the input DC voltage, the voltage on a DC capacitor and the current on the winding to calculate the switching time of each region in SVPWM modulation. The next part is designing the voltage controller.

4.1. Model of GPU

Figure 6 (b) shows the structure of the 400Hz NPC inverter with switching frequency is 16 kHz using the transformer equivalent diagram, which is converted on the secondary side. Consider L_m and X_m to be extremely large and can be ignored. The system was then equivalent to using an LC low-pass filter as Figure 6 (c), where L is an inductance with an internal resistance of r, C_f is an AC filter capacitor, the parameters of the filter are shown in detail in Table 2. With this system, the switching frequency is 16 kHz, this is a multiple of 400 Hz. The dynamic equations of this circuit can be expressed as [4]:

$$\begin{bmatrix} di_L/dt \\ dv_o/dt \end{bmatrix} = \begin{bmatrix} -r/L & -1/L \\ 1/C_f & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & -1/C_f \end{bmatrix} \begin{bmatrix} v_i \\ i_o \end{bmatrix} \quad (11)$$

$$U_o(s) = \frac{U_i(s)}{LC_f s^2 + rC_f s + 1} - \frac{(Ls+r)I_o(s)}{LC_f s^2 + rC_f s + 1} \quad (12)$$

$$U_o(s) = G_P(s)U_i(s) - G_{dis}(s)I_o(s) \quad (13)$$

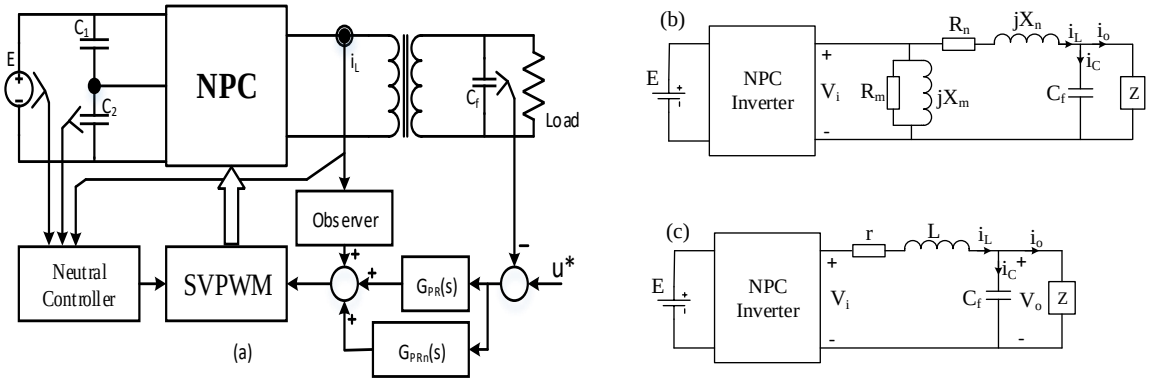


Figure 6. The overall structure of the system

The corresponding continuous-time-domain model is shown in Figure 7.

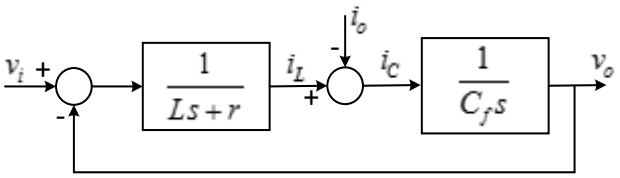


Figure 7. Continuous-time model for the analysis of the GPU

Table 2. GPU Parameters

Filter Inductor	L = 200μH
Filter Capacitor	C_f = 25μF
Filter Resistance	r = 0.2 Ω
Power	P = 5kVA

4.2. Single-loop control with PR controller

Because the PWM pulse generator frequency is quite close to the 400 Hz operating frequency of the inverter, using two circuits to control the current and voltage is not reasonable in this GPU structure. Figure 8 shows a control structure using a voltage control loop. This structure uses a first-order resonant controller, along with 3rd, 5th, 7th harmonic controllers connected in parallel. This control structure has the effect of eliminating static deviations compared to when using the PID controller [18], while minimizing the harmonic steps that ensure small THD. The PR resonance controller is more convenient than the PI controller in the αβ coordinate system [22]. Because while working on the αβ coordinate system need to convert the coordinate system to the frequency angle ωt, and the PR controller does not need [23]. The transfer function of the controller is as shown in (14).

$$G_C(s) = \sum_{n=1}^{2k+1} K_{rn} R_n(s) = \sum_{n=1}^{2k+1} K_{rn} \frac{s.cos(\theta_n) - \omega_n sin(\theta_n)}{s^2 + \omega_n^2} \quad (14)$$

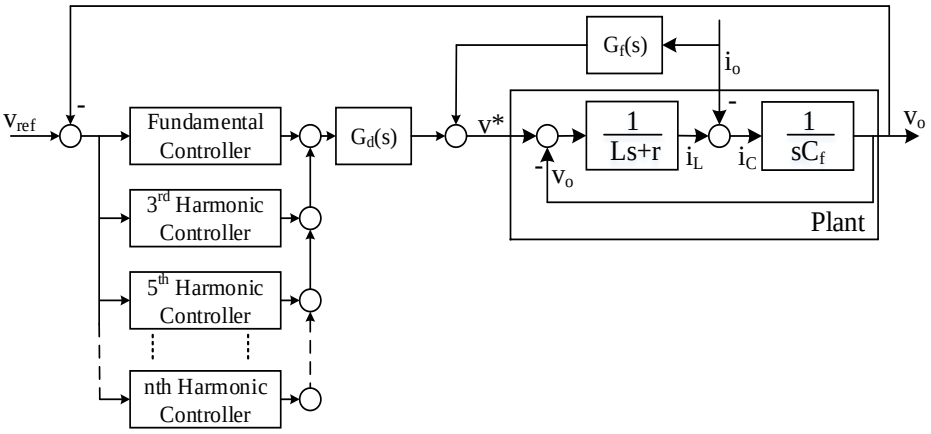


Figure 8. Single-loop control of a 400 Hz GPU

Where ω_n is the resonant frequency at the 1st, 3rd, 5th, 7th…;$\theta_n$is phase angle of the resonant at the frequency which can be used to compensate for the phase delay of the controlled system. $G_d(s)$ function is a late function, it represents the PWM stage in the system. In this system, the PWM stage causes 1 to 2 cycles of T_S pulse delay.

$$G_d(s) = \frac{1}{1{,}5.T_S.s+1} \quad (15)$$

4.3. Design of the feed-forward controller

Only one voltage control loop for the 400 Hz inverter has the disadvantage of a slow response and cannot control the load current. A current feed-forward controller $G_f(s)$ on the inductor is necessary. The feed-forward controller based on the Figure 8 should look like:

$$G_f(s) = \frac{Ls+1}{K_{SPWM}} \quad (16)$$

Where K_{SPWM} is a linear gain

However, when the high-harmonic of the current will be fed to the output of the voltage controller, this increases the high-harmonic at output voltage. Therefore, to increase resistance to interference, an equivalent filter $\frac{s}{as+b}$ is used instead of the derived transfer function, then:

$$e = s - \frac{s}{as+b} \quad (17)$$

where, e is the error between the equivalent filter and the derived transfer function.

With the method of squaring the smallest error, the optimal values a and b are determined as shown in (18) and (19):

$$J = e^2 \quad (18)$$

$$J' = 2ee' = 2s\left(\frac{as+b-1}{as+b}\right)\left(\frac{(as+b)^2-b}{(as+b)^2}\right) = 0 \Rightarrow \begin{cases} s = 0(N.A) \\ as+b = 1 \\ (as+b)^2 = b \end{cases} \quad (19)$$

With the frequency of the inverter is 400Hz so s = 2π.400. Therefore:

$$a.800\pi + b = 1 \rightarrow \begin{cases} a = \frac{1}{1600\pi} \\ b = 0.5 \end{cases} \quad (20)$$

As a result, the equation of the optimum noise-robust smooth derivative will be equal to:

$$s = \frac{s}{\frac{1}{1600\pi}s+0.5} = \frac{1600\pi s}{s+800\pi} \quad (21)$$

The transfer function of the feed-forward controller will be as (22):

$$G_f(s) = \frac{L\left(\frac{1600\pi}{s+800\pi}\right)+r}{K_{SPWM}} \quad (22)$$

5. RESULTS

5.1. Results with MATLAB/Simulink

The continuous model is modeled on MATLAB/Simulink with an input DC voltage of 400 V, pulse frequency of 16 kHz, LC filter parameters are shown in Table 4. To verify the response time of the neutral point voltage controller, the initial voltage on capacitor C_1 is 400 V and the initial voltage on capacitor C_2 is 0V. Figure 9 (V_{diff}) shows the voltage on the two DC capacitors, initially the voltage on the two DC capacitors is 400 V apart (without the controller). At 0.06 s for the neutral point voltage controller to operate, only after 10 ms the neutral point voltage is only 0.3 V apart.

For a period of up to 0.06 seconds, the voltage pattern after the NPC inverter in Figure 9 (V_{int}) cannot generate three levels of voltage; voltage after LC filter cannot stick to set value, orange line is set value, blue line is meet Figure 9 (V_{out}). Figure 10 THD of the output voltage (a) without and (b) with neutral-point voltage controller Figure 9 shows that the neutral point voltage has a great impact on the THD of the system. When the unbalance of neutral point voltage Figure 10 (a) THD = 10.38% is much larger than that of the neutral point voltage Figure 10 (b) THD = 0.88%.

Figure 11. THD of the output voltage when first-order PR controller and high-order harmonic PR controller. Figure 11 show the high harmonic elimination capability of the resonant controller when working with nonlinear loads, the harmonic results using only the first harmonic resonance controller, THD=2.09%, 3rd and 5th order harmonics have great values, respectively 1.1% and 0.95% (blue line). When using the combination of the 3 and 5 harmonic resonance controllers, the harmonic value of these two orders has been significantly reduced, which is 0.05% (3rd order) and 0.55% (5th order); THD = 1.53% (red line).

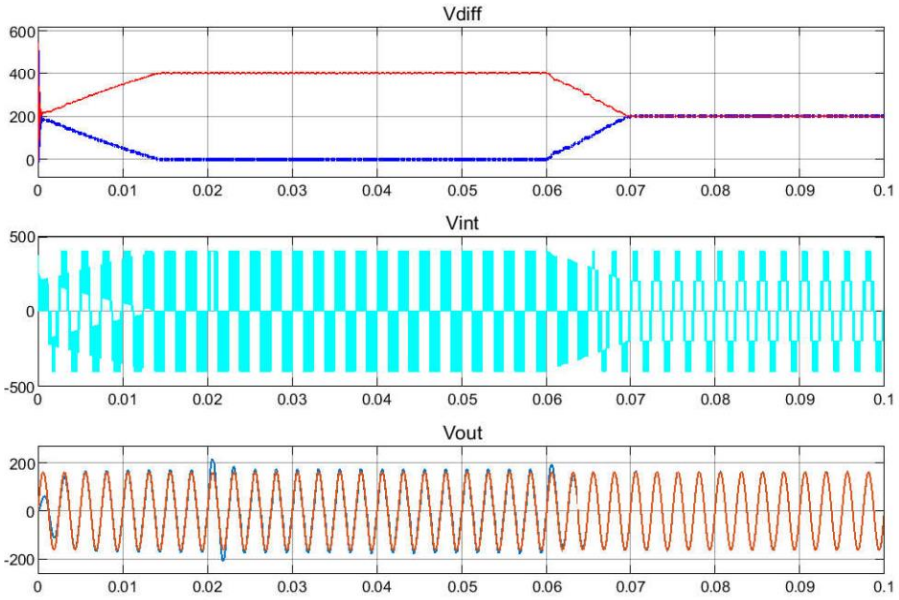


Figure 9. Simulation result of the neutral point voltage controller

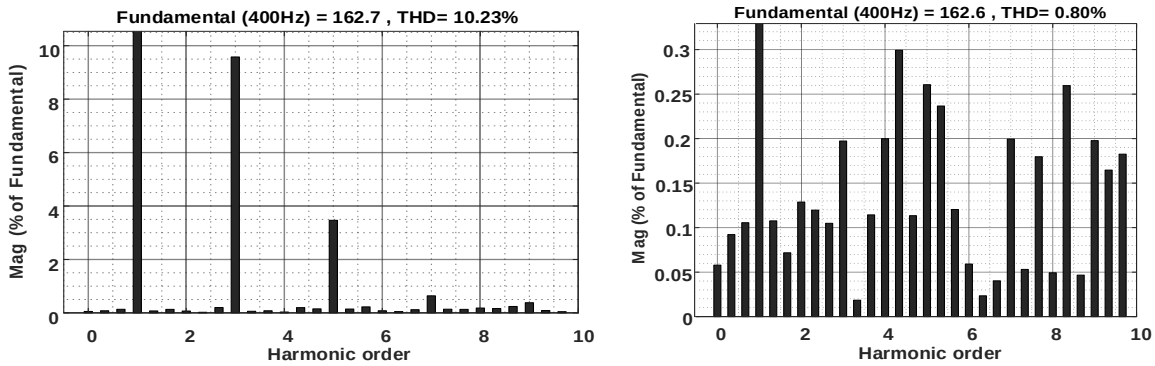


Figure 10. THD of the output voltage (a) without and (b) with neutral-point voltage controller

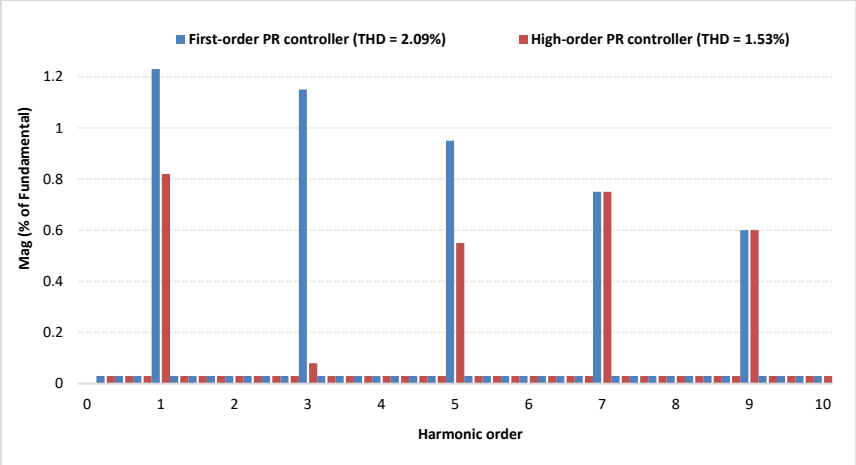
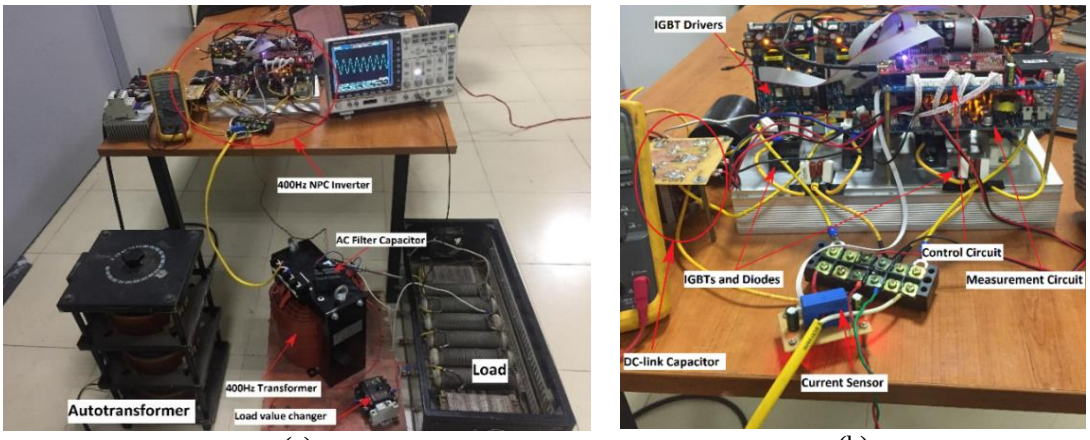


Figure 11. THD of the output voltage when first-order PR controller and high-order harmonic PR controller

5.2. Experiment results

5 kVA inverter prototype includes: capacitors link DC 2200 µF/400 V; IGBT is used as switching devices; control circuit use DSP F28379 D; 400 Hz transformer integrated filter inductor L=200µH; AC capacitor filter 400 Hz 50 µF; load resistance R = 3 Ω, as show in Figure 12 (a) and Figure 12 (b).



(a) (b)

Figure 12. 400 Hz practical inverter system, (a) system overall; (b) control circuit

In fact, experimenting with the case where the imbalance voltage across the two DC capacitors is large as in the simulation would be very dangerous. Therefore, in this test we will use the initial voltage available on the two DC capacitors. Figure 13 shows the voltage difference on the two original DC capacitors is 60 V, when using the neutral point voltage controller, after 13 ms the voltage at the neutral point has returned to the equilibrium position. The neutral point voltage balance algorithm has had many studies and many different results. Malakondareddy *et al.* [24] proposed an adaptive proportional integral (API) controller with a response time of 24 ms. In [25], [26] proposed a novel virtual space vector modulation (RCMV_VSVPWM), a set of novel virtual voltage vectors are generated to balance the neutral point voltage with a response time of 30ms. Since then, the neutral point voltage balance method in this paper has a faster response time and is suitable for 400 Hz inverters.

Figure 14 and Figure 15 show the output voltage of the NPC inverter and the voltage form, the output of the LC filter with a resistive load. NPC inverter structure works well with frequency 400 Hz. To test the responsiveness of the resonant controller, use a contactor to close the 3 Ω load. Initially, the system operates in no load condition, then the load is changed from no load to full load condition. The results are shown in Figure 16, the system has stabilized and reached the reference value in less than one cycle of 400 Hz.

To confirm the total harmonic distortion of the output voltage, the data of the output voltage from the oscilloscope will be transferred to the computer and processed by MATLAB software to get the THD value. Figure 17 (a) and Figure 17 (b) show the THD value in two cases, the first is working with the first-order PR (THD =2.97%), the second is working with the high-level PR (THD =1.46%). The results show that the high-harmonic resonator controller can eliminate the 3^{rd} and 5^{th} harmonic.

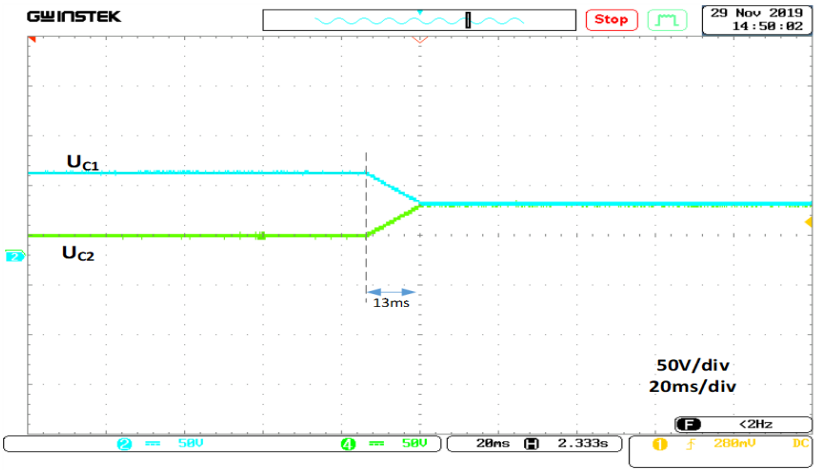


Figure 13. The point voltage controller

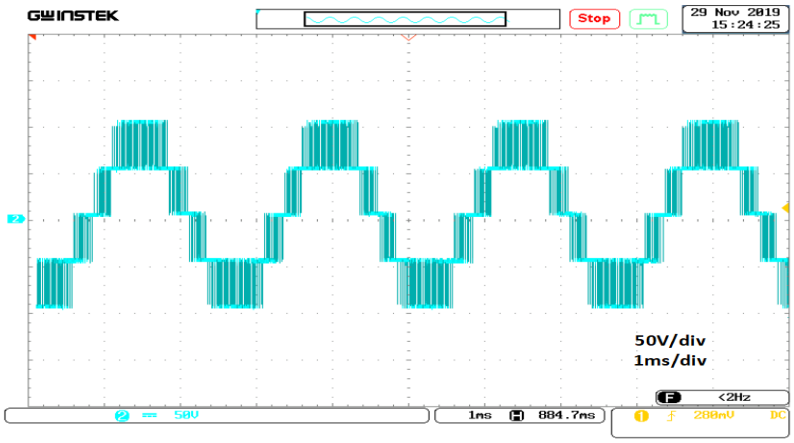


Figure 14. Inverter output voltage

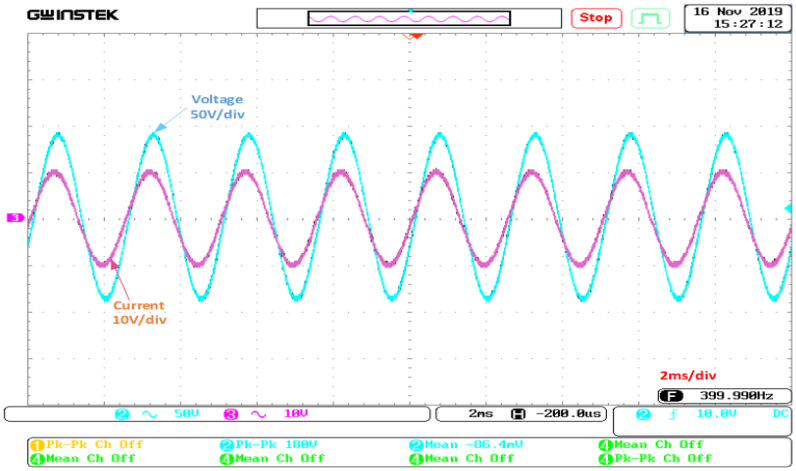


Figure 15. Output voltage after LC filter and current of inductor

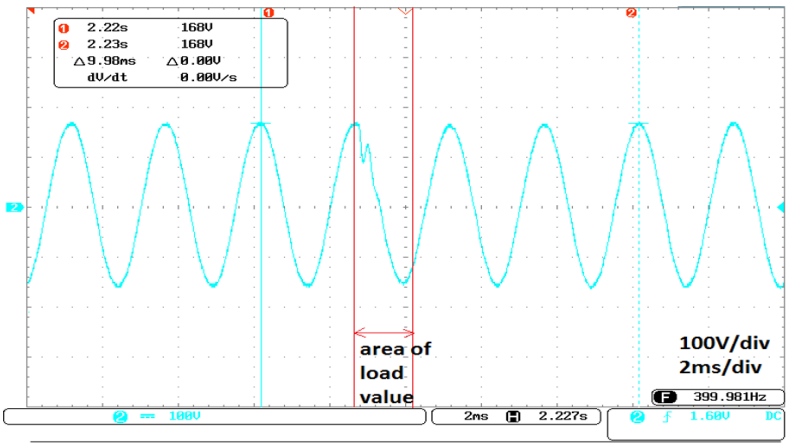
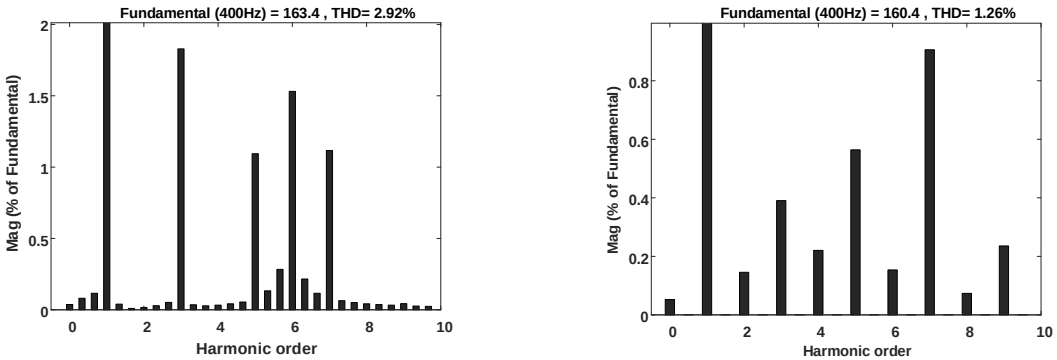


Figure 16. Response of the PR controller when changing load value



(a) (b)

Figure 17. Experimental results THD of the output voltage when using the first harmonic PR controller and high-order harmonic PR controller, (a) using the first harmonic PR controller; (b) using high-order harmonic PR controller

6. CONCLUSION

This paper presents a new approach to a three-level NPC clamping diode structure for 5 kVA 400 Hz inverters to minimize harmonics. A method of controlling the voltage balance on a DC capacitor with a fast response rate by changing the position of the pole and zero points and the static deviation is greatly reduced. The 3rd, 5th, and 7th harmonic compensated resonance controller is applied. In order to increase response to the output voltage, a current feed-forward controller with high-order harmonic filtering is used, thereby minimizing harmonics generated to the inverter. The experimental results have proved this when the obtained THD was 1.46% at 5 kVA capacity.

ACKNOWLEDGEMENTS

This research is funded by the Hanoi University of Science and Technology (HUST) under project number DTDL.CN-14/18.

REFERENCES

[1] T. S. Ferreira, L. M. F. Morais, S. I. Seleme Júnior, P. F. Donoso-Garcia, and P. C. Cortizo, "A study of HPS lamp models performance and behavior with third harmonic injection to avoid acoustic resonance," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, 2013, pp. 6040-6045, doi: 10.1109/IECON.2013.6700127.

[2] A. H. Niasar, M. Rahimi, and A. Akhbari, "Design and simulation of a single-phase 400 Hz inverter with variable input and output voltages," in *2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*, 2020, pp. 1-7, doi: 10.1109/PEDSTC49159.2020.9088484.
[3] N. T Abraham, C.A Pradeep Kumar, and S. L. Mathew, "Application of AGPU for matrix converters," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 5, no. 1, pp. 129-134, July 2014, doi: 10.11591/ijpeds.v4i1B.5340.
[4] D. Manohar, and Seema P.N, "Deadbeat controller with phase corrector for 400-Hz inverter used in ground power units of aircrafts," in *2015 International Conference on Technological Advancements in Power and Energy (TAP Energy)*, 2015, pp. 127-131, doi: 10.1109/TAPENERGY.2015.7229604.
[5] H. Khaligh, H. Torkaman, and A. Ebrahimian, "Novel algorithm for optimum output passive filter design in 400 Hz inverter," in *2018 9th Annual Power Electronics, Drives Systems and Technologies Conference (PEDSTC)*, 2018, pp. 335-340, doi: 10.1109/PEDSTC.2018.8343819.
[6] Y. Zhao, W. Dong, X. Zou, L. Tong, and G. Zhu, "Analysis and design of power hardware-in-the-loop testing for 400-Hz inverters," in *2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2017, pp. 1122-1126, doi: 10.1109/ICIEA.2017.8283008.
[7] G. Yuan, S. Luo, S. Zhou, X. Zou, and K. Zou, "Low-order harmonics analysis and suppression method for 400Hz single-phase VSI," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2341-2345, doi: 10.1109/APEC.2015.7104675.
[8] P. R. Martinez-Rodriguez, D. U. Campos-Delgado, J. F. Martinez-Garcia, J. C. Renteria-Soto, J. M. Sosa, and C. A. Limones-Pozos, "A study on the single-phase NPC multilevel power converters for active power injection," in *2017 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC)*, 2017, pp. 1-6, doi: 10.1109/ROPEC.2017.8261669.
[9] S. Brovanov, S. Kharitonov, M. Dybko and E. Grishanov, "A new approach for current calculation in a single-phase three-level NPC converter with space vector PWM," in *2010 IEEE Region 8 International Conference on Computational Technologies in Electrical and Electronics Engineering (SIBIRCON)*, 2010, pp. 639-644, doi: 10.1109/SIBIRCON.2010.5555145.
[10] D. Roy, S. Kumar, and M. Singh, "A novel region selection approach of SVPWM for a three-level NPC inverter used in electric vehicle," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol 10, no 4, p. 1705-1713, December 2019, doi: 10.11591/ijpeds.v10.i4.pp1705-1713.
[11] Z. Zhang, Y. -x. Xie, W. -p. Huang, J. -y. Le, and L. Chen, "A new SVPWM method for single-phase three-level NPC inverter and the control method of neutral point voltage balance," in *2009 International Conference on Electrical Machines and Systems*, 2009, pp. 1-4, doi: 10.1109/ICEMS.2009.5382854.
[12] R. Krishna, D. E. Soman, S. K. Kottayil, and M. Leijon, "Pulse delay control for capacitor voltage balancing in a three-level boost neutral point clamped inverter," *IET Power Electronics*, vol. 8, no. 2, pp. 268-277, 2015, doi: 10.1049/iet-pel.2014.0103.
[13] A. do E. Dutra, M. A. Vitorino, R. P. R. de Sousa, M. B. R. Corrêa, and G. G. dos Santos, "High-frequency pulsating DC-link three-phase multilevel NPC inverter without electrolytic capacitor," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1348-1355, doi: 10.1109/ECCE.2018.8558091.
[14] M. Sharifzadeh, H. Vahedi, A. Sheikholeslami, P. Labbé, and K. Al-Haddad, "Hybrid SHM–SHE modulation technique for a four-leg NPC inverter with DC capacitor self-voltage balancing," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4890-4899, Aug. 2015, doi: 10.1109/TIE.2015.2405059.
[15] A. Choudhury, P. Pillay, and S. S. Williamson, "DC-Bus voltage balancing algorithm for three-level neutral-point-clamped (NPC) traction inverter drive with modified virtual space vector," in *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 3958-3967, Sept.-Oct. 2016, doi: 10.1109/TIA.2016.2566600.
[16] F. Sebaaly, H. Vahedi, H. Y. Kanaan, N. Moubayed, and K. Al-Haddad, "Design and implementation of space vector modulation-based sliding mode control for grid-connected 3L-NPC inverter," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7854-7863, Dec. 2016, doi: 10.1109/TIE.2016.2563381.
[17] M. Rivera, D. Faundez, J. Kolar, P. Wheeler, F. Besoain, and J. A. Riveros, "A new ground power unit (GPU) supply for aircraft applications," in *2018 IEEE Biennial Congress of Argentina (ARGENCON)*, 2018, pp. 1-6, doi: 10.1109/ARGENCON.2018.8646311.
[18] S. R. Mathew, P. V. R. S. Kiran, M. Anand, and A. Rajeev, "Design and implementation of a three-level diode clamped inverter for more electric aircraft applications using hardware in the loop simulator," in *2014 International Conference on Advances in Electronics Computers and Communications*, 2014, pp. 1-6, doi: 10.1109/ICAECC.2014.7002465.
[19] M. Abarzadeh, and K. Al-Haddad, "An improved active-neutral-point-clamped converter with new modulation method for ground power unit application," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 203-214, Jan. 2019, doi: 10.1109/TIE.2018.2826484.
[20] C. Hu *et al*., "An improved virtual space vector modulation scheme for three-level active neutral-point-clamped inverter," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7419-7434, Oct. 2017, doi: 10.1109/TPEL.2016.2621776.
[21] S. Cobreces, E. J. Bueno, F. J. Rodriguez, J. Salaet, and J. Bordonau, "A new neutral-point voltage control for single-phase three-level NPC converters," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1-6, doi: 10.1109/pesc.2006.1711807.
[22] L. Cui, L. Zhenxing, C. Li, and W. Jiying, "A novel control method for single-phase power inverter systems based on Hilbert transform and DQ transform," in *2017 29th Chinese Control and Decision Conference (CCDC)*, 2017, pp. 7430-7435, doi: 10.1109/CCDC.2017.7978530.

[23] M. Nouri, O. Salari, K. Hashtrudi-Zaad, and A. Bakhshai, "A hybrid designed digital dual-loop control of high power ground power unit (GPU)," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1-P.10, doi: 10.23919/EPE17ECCEEurope.2017.8099172.
[24] B. Malakondareddy, S. Senthil Kumar, N. Ammasai Gounden, and I. Anand, "An adaptive PI control scheme to balance the neutral-point voltage in a solar PV fed grid connected neutral point clamped inverter," *International Journal of Electrical Power & Energy Systems*, vol. 110, pp. 318-331, 2019, doi: 10.1016/j.ijepes.2019.03.012.
[25] W. Jiang, X. Huang, J. Wang, J. Wang, and J. Li, "A carrier-based PWM strategy providing neutral-point voltage oscillation elimination for multi-phase neutral point clamped 3-level inverter," *IEEE Access*, vol. 7, pp. 124066-124076, 2019, doi: 10.1109/ACCESS.2019.2938623.
[26] W. Jiang *et al*., "A novel virtual space vector modulation with reduced common-mode voltage and eliminated neutral point voltage oscillation for neutral point clamped three-level inverter," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 2, pp. 884-894, Feb. 2020, doi: 10.1109/TIE.2019.2899564.

BIOGRAPHIES OF AUTHORS

Do Ngoc Quy received the B.E and M.Sc. degrees in control and automation from the Hanoi University of Science and Technology, Hanoi, Vietnam, in 2020. He is currently working at Institute for Control Engineering and Automation, Hanoi University of Science and Technology, Hanoi, Vietnam. His research interests include Power electronics, Power management for electric vehicles.

Do Ba Phu received the B.E and M.Sc. degrees in control and automation from the Hanoi University of Science and Technology, Hanoi, Vietnam, in 2020. He is currently working at Institute for Control Engineering and Automation, Hanoi University of Science and Technology, Hanoi, Vietnam. His research interests include Power electronics, Power management for electric vehicles.

Nguyen Kien Trung received the B.E. and M.Sc. degrees in control and automation from Hanoi University of Science and Technology, Vietnam in 2008 and 2011, respectively. In 2016, he received the Ph.D. degree in Functional control systems at Shibaura Institute of Technology, Japan, where he worked as a postdoctoral researcher in 2016-2017. From 2018, he works as a lecturer at Hanoi University of Science and Technology. Dr. Trung is a member of the IEEE and IEE of Japan. His research interests include high-frequency converters and wireless power transfer systems.