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Modified asymmetrical 13-level inverter topology with reduce power semiconductor devices

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ABSTRACT

This paper introduces a modified multilevel inverter topology with asymmetrical dc sources combination. The significant features of the proposed circuit are the reduced number of switches and low total standing voltage (TSV). Proposed topology utilizes ten switches to produce 13 level output with per unit $TSV_{p.u}$ of 5.33. An additional feature of the proposed topology is the inherent negative level generation as there is no requirement of an H-bridge for the polarity reversals. Nearest level control (NLC) technique is used as the modulation strategy. Performance of the proposed topology is validated through extensive analysis using Simulink and PLECS software. Detailed circuit analysis and its power loss, as well as efficiency studies, have been carried out under constant and dynamic load conditions. Results obtained shows that the proposed topology is working well, producing an output of 13-level with total harmonic distortion of 6.36% and inverter efficiency of 98.8%. The topology is extended to n-level structure, and its generalized expressions for different parameters were formulated. The comparison of the generalized structure with other existing topology is carried out, and it is found that the proposed topology outperform other topologies on many parameters.

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1. INTRODUCTION

The power generation from renewable energy sources has tremendously increased in the last few decades leading to the development of new power electronic-based converters. Multilevel inverters (MLI) have shown great promise in the area of solar energy generation, electric vehicles, HVDC systems and Flexible AC Transmission Systems (FACTS). MLIs utilize a proper combination of switches, diodes, and capacitors to generate a multilevel voltage waveform. The MLIs in comparison to conventional two-level inverter have reduced voltage stress across switches and lower total harmonic distortion (THD) in output voltage. Further, MLIs have high power handling capacity and efficiency with reduced EMI. Conventional MLI topologies include Flying capacitor (FC) type, Diode clamped type (DC) and cascaded Bridge-type (CHB). FC and DC type topologies utilize a large number of diodes and capacitors to get the staircase voltage waveform.

Moreover, the problem of capacitor voltage balancing remains a major issue in FC and DC type of topologies. The CHB topology is popular but independent dc source for each H-bridge is needed to increase

voltage level and decrease the THD in output voltage. Furthermore, no voltage boosting takes place in conventional topologies. All these problems lead to an increase in weight, cost, size and complexity of conventional MLIs.

In the last few years, to mitigate the problems associated with conventional MLIs, many new and modified structures of MLIs are reported in the literature [1]. The main focus of the researchers is to develop new MLI topologies with a reduced number of switching and passive elements and low voltage stress across switches. Moreover, low THD in voltage, inherent voltage boosting, and fault-tolerant operations are other desirable features present in new MLI topologies. Asymmetric MLIs have gained acceptance as it uses different values of input voltage sources to generate more voltage levels as compared to symmetric structures.

A comprehensive review of MLIs with generalized formulae for the number of switches, gate drivers, dc voltage levels and TSV is presented in [1]. A new multilevel inverter with bidirectional switches with symmetric and asymmetric configurations is proposed in [2]. Authors have also proposed generalized topologies of modular cascaded H-bridge MLIs which can generate a maximum number of voltage levels with lesser number of switches [3-5] and dc sources. New T-type and E-type asymmetric topologies of MLI is proposed in [6-7]. These topologies do not use any H-bridge for creating negative levels, and a smaller number of switching devices and dc sources are employed for generating more voltage levels as compared to conventional CHB structures. Some new topologies of MLIs are proposed to generate thirteen and fifteen levels of output voltage [8-9]. Nearest level control (NLC) technique is used to switch devices at fundamental frequency [8] to reduce the switching losses of converter. A new cascaded MLI for high voltage applications employing subunits with low voltage stress is proposed in [10]. Switched capacitor-based MLI with inherent boost capability is proposed by authors in [11-12].

The SCMLI topologies have gained acceptance in recent years as they use capacitors in place of dc sources. With proper charging and discharging of capacitors, the input voltage can be boosted up. However, current spikes through switching devices and capacitor voltage balance are the problems to be solved for SCMLI topology. Some other switched capacitor-based topologies which uses capacitors in place of dc sources are proposed in [13-14]. However, in [14], an additional H-bridge is required to inverse the polarity of the voltage. A cascaded H-bridge topology for the generation of the 13-level output voltage is proposed in [15]. In [16], a modified three-level NPC with boost capability and a reduced number of switches is proposed to generate seven voltage levels. A hybrid MLI employing advantages of SCMLI and conventional MLI is proposed in [17]. The topology has less peak voltage stress on devices, and simple control technique is used to balance the capacitor voltage. In [18], asymmetrical MLI producing nine output levels is presented. The topology is capable of produce all positive and negative levels but utilises cascade H-bridge for polarity changing. A latest and novel packed E-cell (PEC) MLI with the inherent boosting capability, and self-voltage balance of capacitors is proposed in [19] to generate a 9-level output voltage. The topology has six unidirectional switches, one bidirectional switch, one dc source and two capacitors. However, the dc-link voltage needs to be sensed to regulate the capacitor voltage. Hence a close loop control is required.

In this paper, a new 13-level asymmetric MLI is proposed. The proposed topology is an improved circuit of structure presented in [19]. The advantages of the proposed topology are the reduced overall components and lesser value of per unit TSV as compared to other topologies. Section I will review existing MLI topologies where their merits and limitations are highlighted. In Section II, brief descriptions on the circuit mode of operations and deployed switching strategy for the proposed MLI is described. The simulation results are discussed in section III, and section IV covers the power loss analysis of the proposed structure. A comparative analysis is presented in section V followed by a brief conclusion in the end in section VI.

2. PROPOSED TOPOLOGY

2.1. Description and operation

Figure 1 shows, the basic structure of the proposed MLI consisted of eight switches, where six are unidirectional, and the two are bidirectional switches. Each unidirectional switch is made up of an IGBT with an antiparallel diode, and a bidirectional switch is composed of two unidirectional switches. The dc source present in the left part of the circuit is V_1, whereas the right unit dc sources have the same magnitude equal to V_2 and both are in a ratio of 3:1.

Table 1 explains the various operating states of the proposed MLI. It shows the states of all the switches in a particular output state of a complete cycle. The 'ON' and 'OFF' state of the switch is denoted by 1 and 0 respectively. The different output levels which are achievable are 0, ±V/3, ±2V/3, ±V, ±4V/3, ±5V/3 and ±2V. Switches (S1, S4) and (S2, S5) operate in a complementary manner, i.e. they cannot turn on simultaneously to avoid the short circuit of the dc sources. Zero voltage can be obtained either by turning on

(S1, S2, S3) or (S4, S5, S6). First voltage level, i.e. V/3 is achieved when switch combination (S4, S5, S8) is in on state. Likewise, 2V/3, the second voltage state, is obtained by (S4, S5, S7). S6 remains completely off in the positive cycle. S2 is also in the off state in the positive voltage levels cycle except at zero voltage. However, in achieving the negative voltage levels, S2 has to remain on all the time.

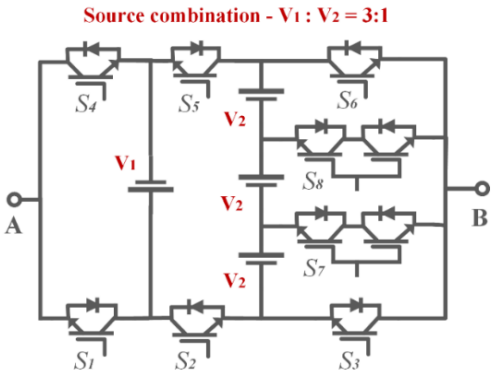


Figure 1. Proposed 13-Level topology

Table 1. Switching state for one complete cycle

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o
Zero	1	1	1	0	0	0	0	0	0
Positive States	0	0	0	1	1	0	0	1	V/3
	0	0	0	1	1	0	1	0	2V/3
	0	0	1	1	1	0	0	0	V
	1	0	0	0	1	0	0	1	4V/3
	1	0	0	0	1	0	1	0	5V/3
	1	0	1	0	1	0	0	0	2V
Zero	0	0	0	1	1	1	0	0	0
Negative States	1	1	0	0	0	0	1	0	-V/3
	1	1	0	0	0	0	0	1	-2V/3
	1	1	0	0	0	1	0	0	-V
	0	1	0	1	0	0	1	0	-4V/3
	0	1	0	1	0	0	0	1	-5V/3
	0	1	0	1	0	1	0	0	-2V

The rating of switches indirectly governs the cost of the inverter. It is considered as advantageous if low rating switches can be employed in inverter design which is only possible if the voltage to be blocked by the switch is not high. Accordingly, the voltage stress on different switches needs to be calculated. The sum of the voltage stress on all the switches can be termed as Total Standing Voltage (TSV). Lesser value of TSV is an indicator of switch ratings in a topology.

The voltage stress on different switches can be evaluated as:

$V_{S1}=V_{S4}=V_1$; $V_{S3}=V_{S6}=3V_2$; $V_{S2}=V_{S5}=(V_1+3V_2)$; $V_{S7}=V_{S8}=4V_2$

Hence, the TSV for the proposed 13 level topology can be written as

$$TSV=2\ (V_1+3V_2+(V_1+3V_2)+4V_2)$$
$$\mathbf{TSV=4V_1+20V_2=32\ V_{dc}} \quad (1)$$

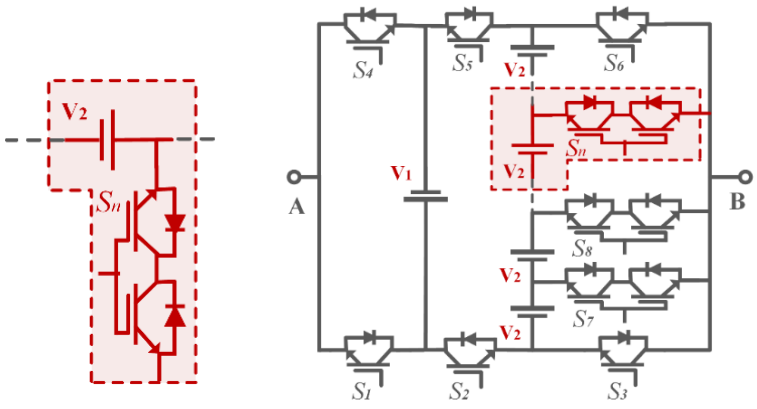
Sometimes, per-unit TSV, which is the ratio of TSV and the maximum output voltage, is also calculated. In our case, per-unit TSV,

$$\mathbf{TSV_{p.u.}=TSV/V_{o,max}=(4V_1+20V_2)/2=5.33} \quad (2)$$

2.2. Generalized circuit extension of the proposed topology

The basic structure of the proposed topology can be easily extended to an n-level structure by adding a dc source along with a bidirectional switch, as shown in Figure 2. The generalized expressions for the proposed extension have been formulated and presented by (1)–(4) below where N_{dc}, N_{sw}, N_{gd} represent the number of dc sources, switches and gate driver circuits respectively. These expressions are formulated based on the number of levels generated. For example, for a particular level, the number of dc sources required can be calculated by (4) and so on.

$$N_{dc} = \frac{N_L-5}{2} \quad (4)$$
$$N_{sw} = \frac{5(N_L-1)}{6} \quad (5)$$
$$N_{gd} = \frac{N_L+3}{2} \quad (6)$$
$$TSV = \frac{8(N_L-1)}{9} \quad (7)$$



(a) (b)

Figure 2. Extension to the n-level structure of the proposed topology, (a) Added Unit, (b) Generalized Structure

2.3. Modulation strategy

There are various techniques used for modulation in a multilevel inverter. These techniques can be classified into high frequency and low-frequency switching techniques. In [20], selective harmonics elimination using newton Rapson method is implemented. Switching control of cascaded compact modular MLI is implemented using pulse with modulation in [21]. Hybrid asymmetrical topology is proposed in [22], in this work THD is reduces using improved modulation technique. Various other methods of high frequency PWM techniques were used to improve the THD and quality of the inverter [23]. Level shifted PWM implemented on cascaded H-bridge topology has been discussed in detail in [24]. Low-frequency techniques offer the advantages of low switching loss as the number of switching in a particular cycle is less [25]. Nearest level control (NLC) is a fundamental frequency switching technique which is used in the proposed MLI to obtain the switching signals. Figure 3 show the level generation method using the NLC method.

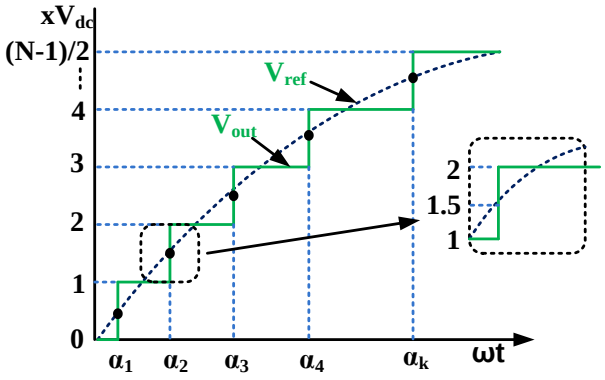


Figure 3. Level generation method using the NLC technique

The switching angle is given by (5):

$$\alpha_k = M\sin^{-1}\frac{(k-0.5)}{(N-1)/2} \quad (5)$$

where, M is the modulation index and is defined as given in (2), k=1, 2…. (N-1)/2.

$$M = \frac{V_{ref}}{V_{out}} \quad (6)$$

where, V_r and V_o is the reference and output voltage, respectively.

3. RESULTS AND DISCUSSION

Operation and the performance of the proposed circuit are validated through extensive simulation analysis under varying load conditions. DC sources value of V1=300V and V2=100V are taken in the analysis. Results obtained are discussed in detail based on the type of load used and the modulation index.

3.1. Constant R-L load

Figure 4(a) shows the switching pulses given to the power switches during one complete cycle at a modulation frequency of 50Hz. Output voltage and current waveforms are obtained using constant R-L load of Z=100+j25 Ω are shown in Figure 4(b). From the FFT analysis, it is found that the voltage THD is 6.36% and is shown in Figure 4(c). At the same time, all the individual harmonic components have less than 5% contribution to the total THD. Voltage waveform shows that the topology successfully achieves 13 level output having all the positive and negative levels, and the load current waveform shows that the topology works well the inductive load.

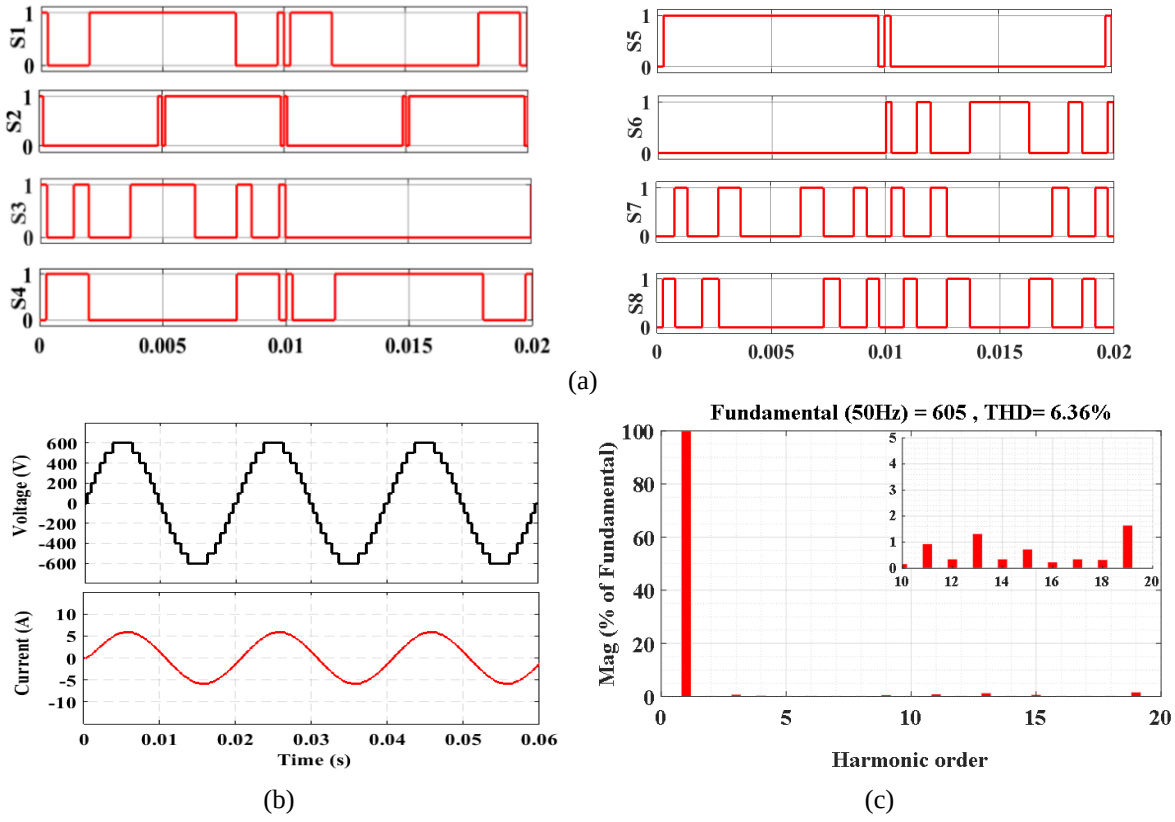


Figure 4. Results obtained using constant RL load, (a) Pulses to the power switches, (b) Voltage and load current waveform, (c) FFT analysis of the output voltage

3.2. Varying R and RL load

To assess the dynamic performance of proposed inverter structure performance is evaluated for varying R and RL load. Figure 5 shows a resistive load change condition in which there is a load variation from open circuit condition to Z=100 Ω to Z=50 Ω. As the resistance is decreased, therefore an increase in current magnitude can be seen. RL load variation is shown in Figure 6 comprising a change from open circuit condition to Z=100+j25 Ω to Z=50 +j12.5 Ω. And the value of the load current changes from zero to 6A to 12A. All the voltage levels are visible with a sinusoidal current having smooth transaction from a step change in load.

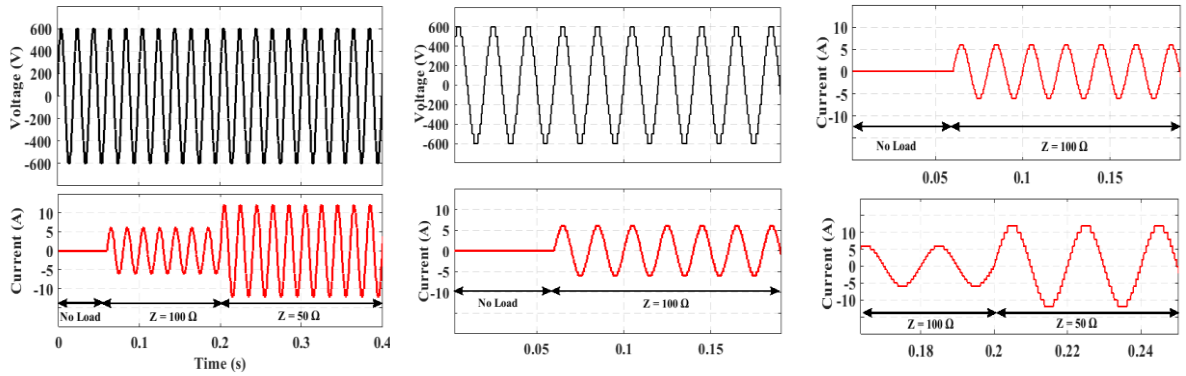


Figure 5. Voltage and load current waveform with varying R load condition, (a) Voltage and load current waveform with varying R load, (b) Magnified waveform during the first step, (c) Magnified waveform during step-change in load

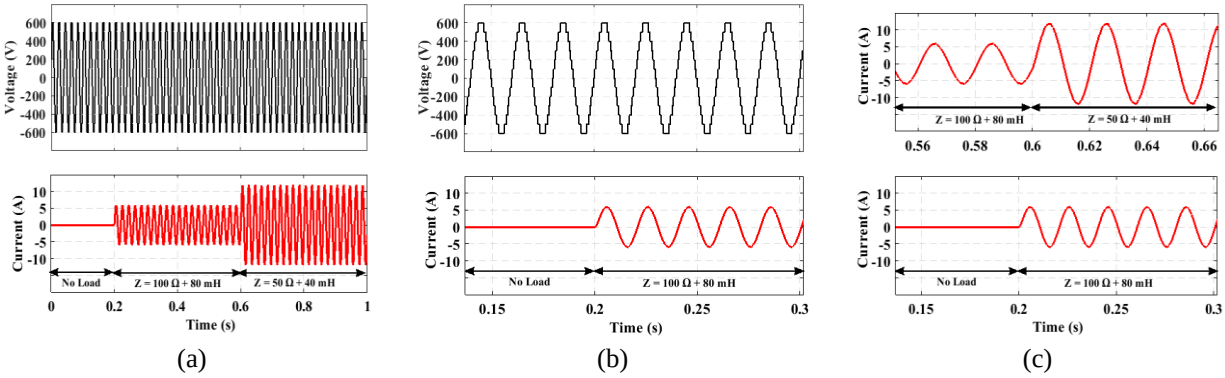


Figure 6. Voltage and load current waveform with varying RL load condition, (a) Voltage and load current waveform, (b) Magnified waveform during the first step, (c) Magnified waveform during step-change in load

3.3. Varying Load Power Factor

In Figure 7, the effect of change in load power factor on the output voltage and current is presented. The power factor of the load varies from unity to lagging power factor by providing a step-change in the load from Z=100 Ω to Z=100+j25 Ω which is evident by the current waveform as the current becomes sinusoidal after the instant of load change.

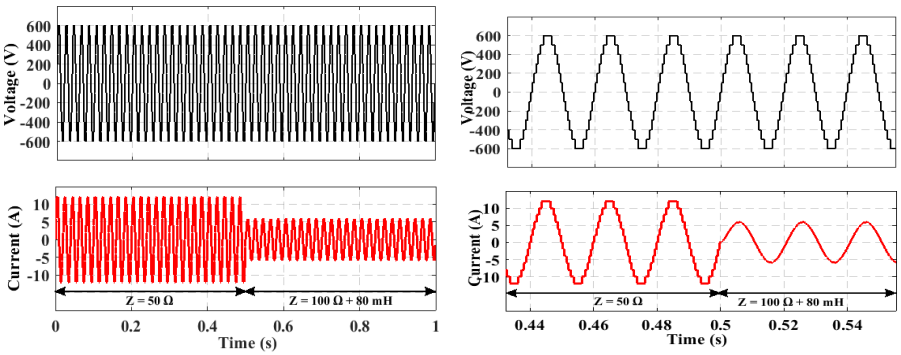


Figure 7. Voltage and load current waveform with varying load power factor condition, (a) Voltage and load current waveform, (b) Magnified waveform

3.4. Varying Modulation Index

The step-change in modulation index is also considered to evaluate the performance of the inverter. Figure 8 depicts the result for varying modulation index (M) from M=1 to M=0.8 to M=0.8. The effect of decreasing the value of M is visible as the number of levels gets reduced from 13 levels to 11 levels, and it further gets reduced to 9 levels.

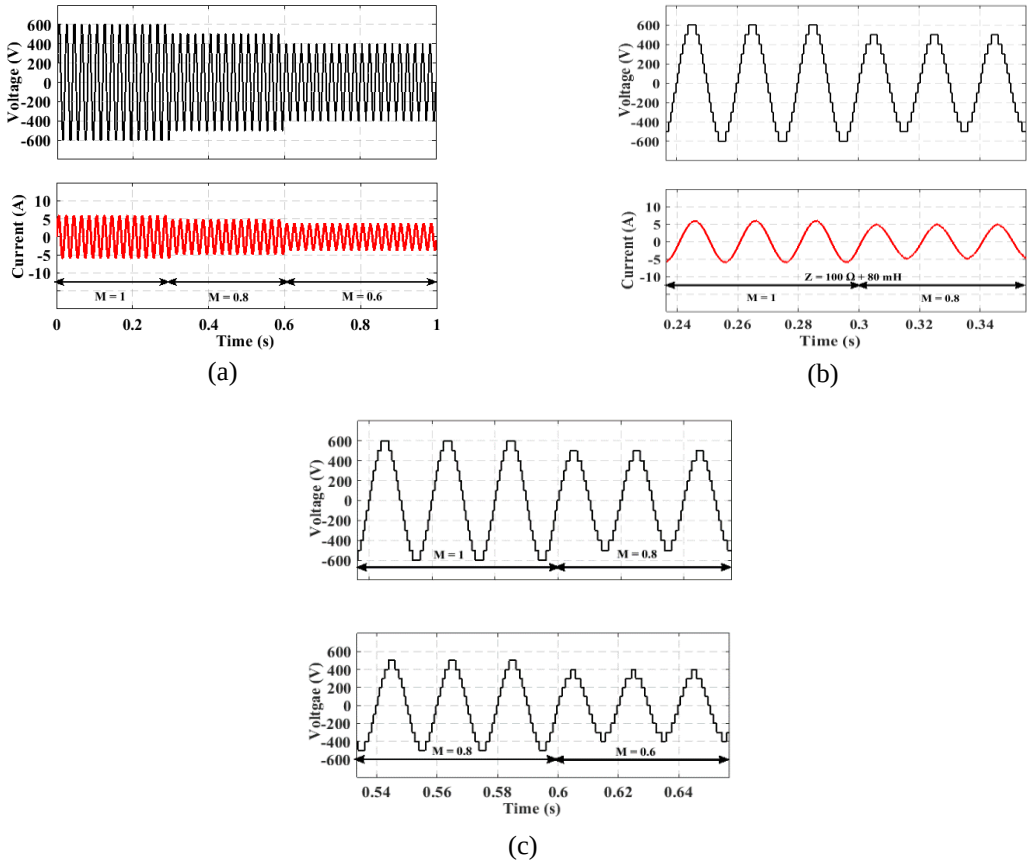


Figure 8. Voltage and load current waveform with varying Modulation index, (a) Voltage and load current waveform, (b) Magnified waveform, (c) Magnified voltage waveform

4. POWER LOSS ANALYSIS

The switches in multilevel inverter need to switch on and off frequently in a complete cycle. These switching operations result in power loss which affects the efficiency of the topology. These losses include conduction loss and switching loss. Therefore, the power loss analysis of the proposed topology is done with the help of PLECS software. Figure 9(a) and 9(b) represent the conduction and switching loss respectively for different loads. The three different loads are Z1=50 Ω, Z2=100+j12.5 Ω and Z3=100+j25 Ω. Figure 9(c) depicts the total loss and efficiency at the three mentioned loads. The voltage stresses on different switches, in terms of Vdc, is shown in Figure 9(d). Maximum voltage stress is experienced by switches S2 and S5 as both the switches block the voltages during complete half cycle alternatively. The efficiency of the proposed structure is compared with the other 13 levels topologies presented in [7] and [8]. From Figure 9(e) it can be seen that the proposed topology has better efficiency when compared to other topologies.

5. COMPARISON WITH OTHER TOPOLOGIES

The proposed structure is compared with some other inverter topologies in order to validate the claim. Table 2 presents a comparison study of different topologies. The parameters taken for comparison are the number of switches (Nsw), gate drivers (Ngd), dc links (Ndc), per-unit TSV. As there are topologies involving a different number of levels (NL), therefore one more parameter (NL/Nsw) is added in the

table. [2, 16] and [17] are 7-level topologies having TSV 6, 7.3 and 6.3, respectively, which is more than the proposed topology. The number of switches used in the topologies of [9] and [12], having 9-levels, are 11 and 17, respectively. Moreover, the TSV value is 6.75 and 5.83, respectively. At the same time, the factor NL/Nsw for these topologies is also lower than the proposed topology. Per-unit TSV is also on the higher side as compared to the topology presented in this paper. The comparison table also shows the topologies having 13 levels. By looking at the table, we can see that all these 13-levels structures contain either an equal or greater number of switches than the proposed topology. The per-unit TSV of the proposed structure is also lower than these topologies. Similarly, other structures can also be compared with the proposed topology. A quick look at the comparison table shows the superiority of the proposed inverter topology in terms of lesser number of switches and lower voltage stress value. A higher value of NL/Nsw and lesser value of TSVp.u. shows that the proposed topology is better than the other discussed structures in terms of the number of components and reduced voltage stresses.

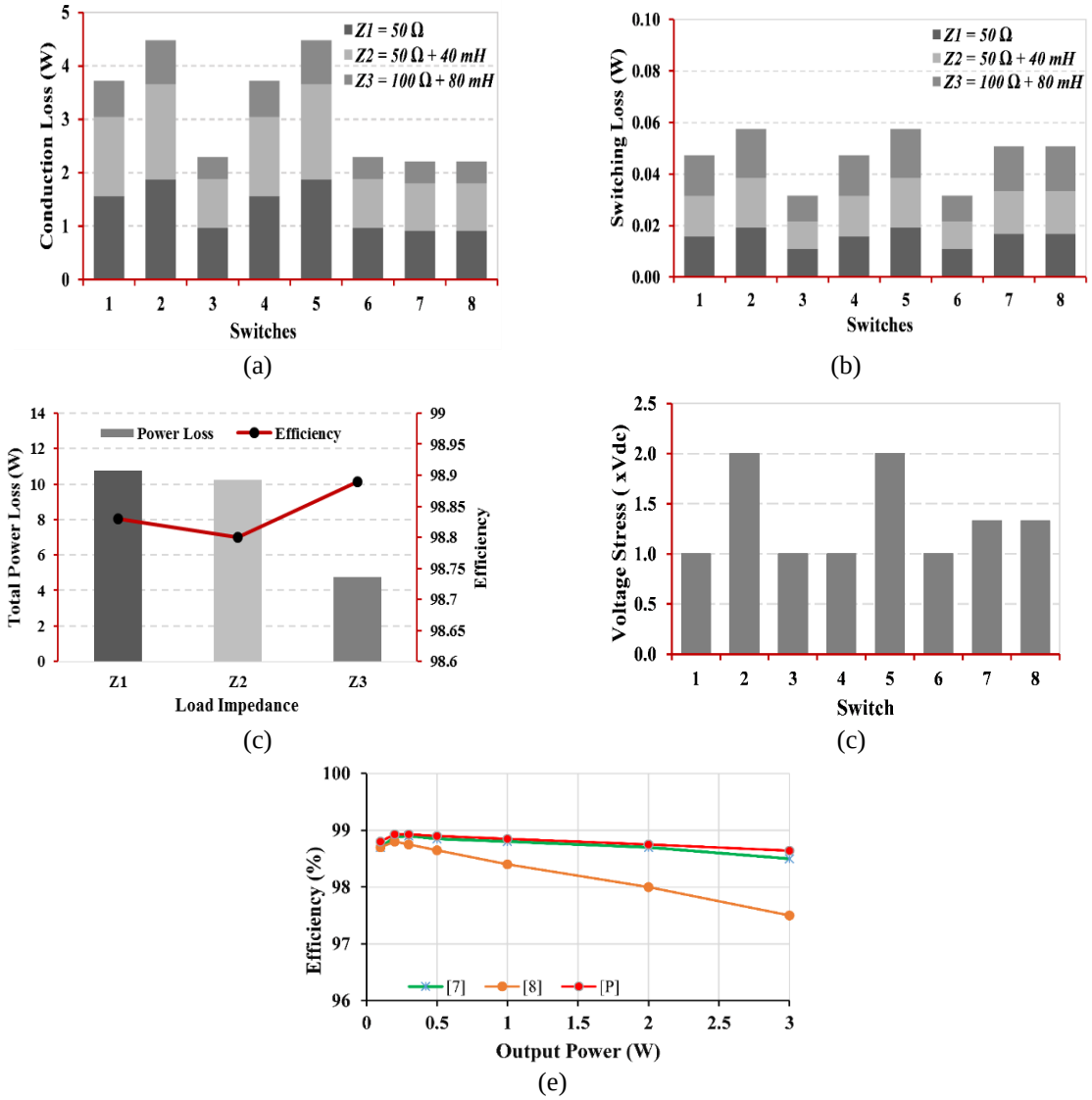


Figure 9. Results obtained from the Power Loss Analysis of the proposed topology, (a) Conduction losses, (b) Switching Losses, (c) Efficiency and Total power loss, (c) Total Standing Voltage (TSV), (e) Variation in Efficiency with output power

Table 2. Comparison of various topologies

Topology	N_L	N_{sw}	N_L/N_{sw}	N_{gd}	N_{dc}	$TSV_{p.u.}$
[2]	7	8	0.875	7	3	6
[6]	17	12	1.42	10	4	6
[9]	9	11	0.82	11	4	6.75
[10]	17	12	1.42	10	4	5.5
[12]	9	17	0.53	17	5	5.83
[13]	13	14	0.93	11	4	5.33
[14]	13	18	0.72	18	6	5
[15]	13	12	1.08	12	3	24
[16]	7	10	0.7	8	5	7.3
[17]	7	9	0.78	8	4	6.3
Proposed	13	10	1.3	8	4	5.33

6. CONCLUSION

This paper presents an improved multilevel inverter topology having low total standing voltage and utilized a reduced number of switches to produce a 13-level output voltage. Topology is extended to the n-level generalized structure by adding extra units consist of 2 switches and dc source to the basic structure. Analysis of constant and dynamic load conditions as well as varying load power factor are also presented and discussed in detail. For constant RL load, the THDv and the value of per unit total standing voltage (TSV) are found to be 6.36% and 5.33, respectively with an efficiency of around 98.8%. Under varying load condition; change in current from zero to 6A and then to 12A with resistive load and from zero to 5.8 to 11.6 A with inductive RL load is attained. As the modulation index changes from 1 to 0.6 output levels reduce from 13 levels to 9 levels. The comparison of the proposed structure with other existing topologies is also provided, and it is noted that the proposed topology outperformed others topologies on many parameters.

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